A linearity improvement method for CIS column-parallel SAR ADC using two-step conversion

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ESSCIRC 2023- IEEE 49th European Solid State Circuits Conference (ESSCIRC) | 979-8-3503-0420-6/23/$31.00 ©2023 IEEE | DOI: 10.1109/ESSCIRC59616.2023.10268814

***Abstract*— This paper presents a new 2-step SAR ADC architecture for image sensors in machine vision applications. This structure effectively improves the structural problems of the image sensor caused by the area occupied by the ADC, such as linearity and temporal noise performance. In this work, we designed a two-step SAR ADC using a 6-bit SAR ADC and a PGA generating residue and offset. Since the number of unit capacitors is reduced, the common centroid method is applied in the capacitor layout to improve the linearity. As a result, the capacitor mismatch characteristic is improved, and the differential nonlinearity (DNL) obtained is +0.36/ −0.28LSB. In addition, the temporal noise is about 530μV_{rms} due to the small bandwidth of the column-parallel structure in an image sensor. The implemented ADC achieves 250kS/s as a maximum speed. The maximum frame rate of the sensor is 2500 fps. The power consumption of the sensor, except for the LVDS interface, is 37.5mW. This sensor is designed in TowerJazz CIS 180nm process with one poly and four metal layers. The supply voltage of the analog and digital domains are 3.3V and 1.8V, respectively.**

Keywords—CMOS Image Sensor, SAR ADC, Linearity, Column-parallel structure

I. INTRODUCTION

Machine vision systems using image sensors have changed our lives. But applications such as autonomous driving assistant systems (ADAS), can have better work efficiency when the image sensor has a higher frame rate. The SAR ADC is an appropriate solution to improve the frame rate of the image sensor. This ADC has a better performance in the range from 100kS/s to 10MS/s. As introduced in previous work [1], the SAR ADC has the best figure-of-merit (FOM) and requires a slow clock which can improve the system power efficiency.

However, designing a SAR ADC in an image sensor brings structural limitations originating from the area occupied by the SAR ADC. First, the sensor has a worse temporal noise performance due to the increased bandwidth of the ADC. As previous research [2-5] described, a SAR ADC is shared within multiple columns. For this reason, the required bandwidth of the SAR ADC also increases proportionally to the area occupied. Second, the mismatch from column to column inherently degrades the fixed pattern noise (FPN) performance and the linearity of the ADC. It takes a lot of effort to improve the mismatch issue after designing an ADC within the narrow space of 1-pixel pitch. Therefore, this inevitable mismatch has been studied. The layout needs to follow the algorithm [7] to enhance the linearity. However, the number of switches and control lines complicates the space, leading to a degraded linearity [3-4].

In this work, we present a two-step SAR ADC in a column-parallel structure to solve the area issue. Since this ADC only uses a 6-bit SAR ADC, the number of switches and the control lines are reduced. Therefore, this ADC occupies a smaller area enough to design a column-parallel structure, and the capacitor DAC array layout is improved sufficiently to enhance the linearity. This paper reviews the sensor structure and timing in section 2. In section 3, the PGA supporting residue generation and the redundancy are discussed in detail. Finally, this paper discusses the measurement results in section 4.

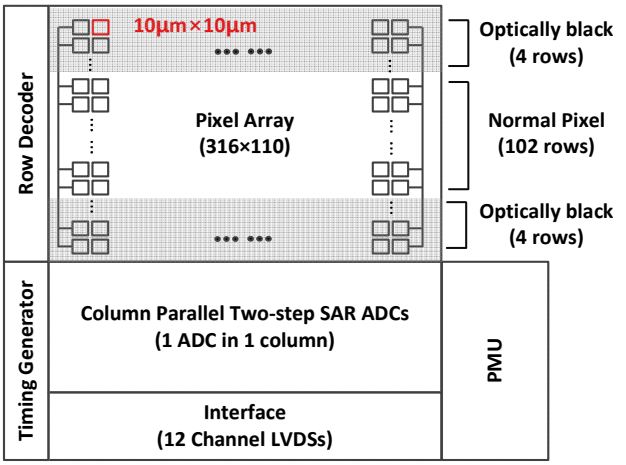

Fig. 1. Sensor block diagram

II. SENSOR ARCHITECUTRE

A. Sensor structure overview and timing

Fig. 1 shows the block diagram of this image sensor. It has a 316×110 pixel array, and the pixel employs the same structure as the previous work [6]. This sensor uses the top 4 lines and bottom 4 lines as optically black (OB) pixels. This sensor uses 316 two-step SAR ADCs in a column-parallel structure, and this two-step SAR ADC consists of a programmable gain amplifier (PGA) and a 6-bit SAR ADC. The PGA provides analog gain up to ×8. To transmit the data to the outside world, 12 channel LVDS interface transmits the data at 1.5Gb/s speed. The power management unit (PMU) provides the reference voltage and the current for the in-pixel source follower, PGA, and LVDS interface, respectively. The row decoder on the left side of the pixel controls the pixels selected by the vertical domain address (VDA).

Fig. 2 shows the timing diagram for the pixel readout. When the sensor starts reading the pixels, the sensor reads the OB pixel first. The sensor uses the data after readout 2 lines of 4 at the top and bottom, respectively. In particular, the integration time is set to a minimum during the readout OB pixel, and this data is used to compensate for the FPN of

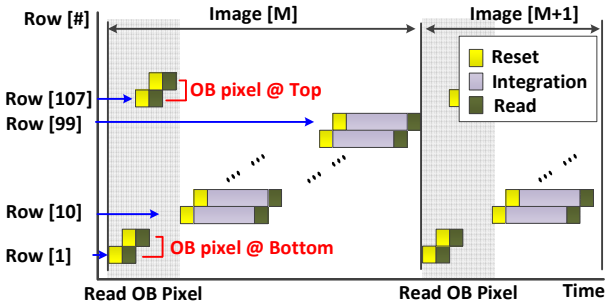

Fig. 2. Pixel readout timing diagram

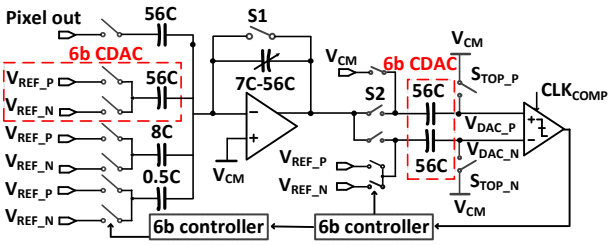

Fig. 3. Two-step SAR ADC circuit block diagram

the image sensor. When the sensor completes reading the OB pixels, the sensor starts readout the active pixel for actual data.

B. ADC structure overview and timing

Fig. 3 is a circuit block diagram of the two-step SAR ADC. The ADC has a capacitor DAC array consisting of 56-unit capacitors at the PGA and the 6-bit SAR ADC, respectively. Considering the dark level, the ADC outputs digital code up to 1792. The additional 8-unit capacitors and 0.5-unit capacitors are used for generating offset for the dark levels and the over-range at PGA. In addition, the feedback capacitor consisting of 56-unit capacitors controls the analog gain, and the other 56-unit capacitors are used in parallel with the capacitor DAC for sampling.

In this ADC structure, the number of control lines and switches is reduced due to the ADC resolution. Therefore, the unit capacitors are equally distributed within the entire capacitor DAC area, as shown in Fig. 5(a). In addition, any adjacent capacitor doesn't share the same node at its bottom plate. This layout can improve the linearity of the ADC. As depicted in Fig. 5(b), metal-insulator-metal (MIM) capacitors using metal 4 and metal 3 are used, and the mismatch caused by the parasitic capacitor between the control line and the bottom plate of the capacitor is prevented by placing the metal 2 in between.

Fig. 4 is a timing diagram explaining the operation of ADC and pixel in a single horizontal line time. When the horizontal line time starts after VDA is transmitted, the pixel outputs the reset level, V_{PIX_RST}, and the ADC starts sampling. Therefore, the PGA samples the pixel output, V_{PIX_RST}, and resets itself by simultaneously turning on the switch S_1. In addition, The ADC starts sampling the output of the PGA, V_{PGA_RST}, by turning on S_2, S_{TOP_N} and S_{TOP_P}. When the reset level sampling is completed, switch S_1 and S_{TOP_N} is sequentially turned off, and the pixel output its integrated signal, V_{PIX_SIG}. After signal level sampling, the ADC turns off the switch S_{TOP_P} and S_2 and starts the 6-bit coarse conversion. After 6 cycles, the PGA controls the

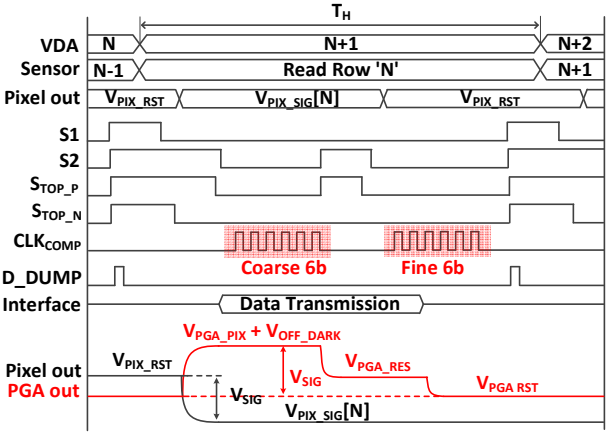

Fig. 4. ADC timing diagram in 1 horizontal line time

capacitor DAC to generate the residue. The ADC turns on switch S_2 and S_{TOP_P} to sample the residue, V_{ADC_RES}, at the positive part of the capacitor DAC. When sampling is completed, the ADC turns off the S_{TOP_P} and S_2 switches sequentially and starts a 6-bit fine conversion. After the 6-bit fine conversion is completed, the 12-bit digital code is generated by the ADC. This final 12-bit digital code is transmitted to the interface at the rising edge of D_DUMP.

III. REDUNDANCY CONTROLLED BY THE PGA

In this work, the PGA performs a critical operation by controlling the connection between the bottom plate of the capacitor DAC array and the ADC reference. For instance, as shown in Fig. 7(a), 8-unit capacitors are controlled to generate the offset, V_{OFF_DARK}, for the dark level of 256. As a result, this offset is added to the actual pixel output signal at T_{OFFSET_1} in Fig. 6, when the ADC completes reset level sampling.

In addition, the PGA supports generating a residue for the 6-bit fine conversion. After 6 cycles of coarse conversion, the control logic for PGA captures the coarse conversion result, D_{COARSE}, at T_{OFFSET_2} in Fig. 6. The capacitor DAC array of the PGA is controlled by following

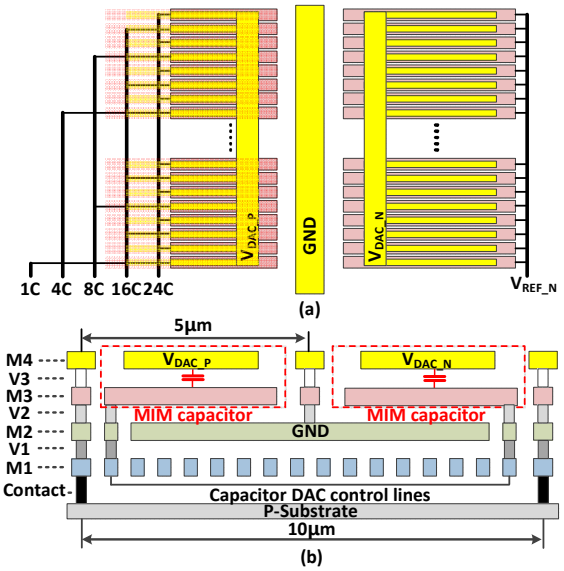

Fig. 5. The layout of the capacitor DAC array: (a) top view, (b) cross-sectional view

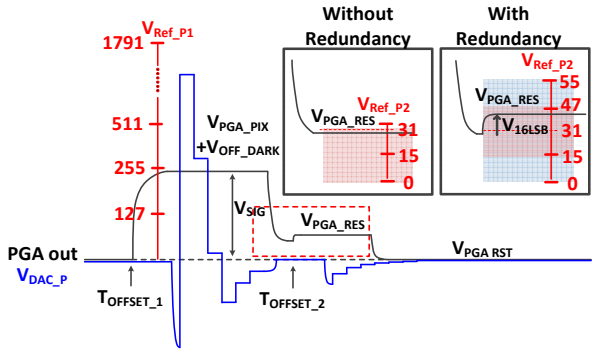

Fig. 6. The timing diagram of the output of PGA and the positive input of the comparator

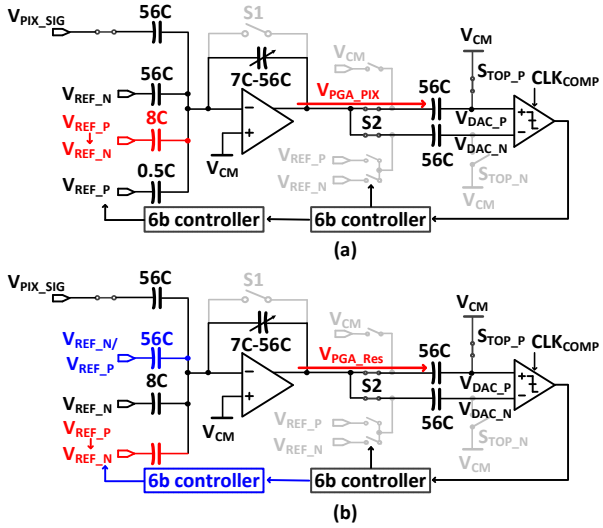

Fig. 7. The capacitor DAC control for generating (a) the offset and (b) the residue

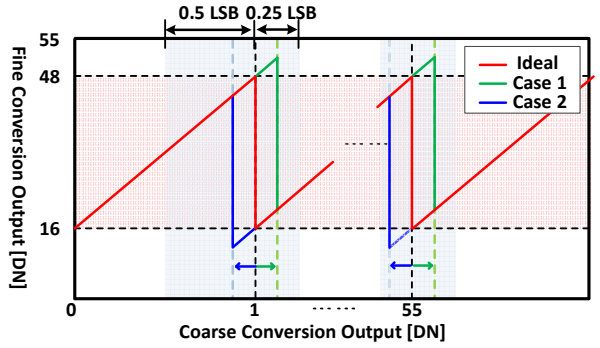

Fig. 8. The transfer curve of two-step SAR ADC

the captured digital code. However, the final output can be distorted when the coarse conversion is wrong. For this reason, this work extends the ADC cover range by adding 1 bit of redundancy, as shown in Fig. 6. To include the redundancy, the PGA generates the 16LSB offset, V_{16LSB}, by controlling the 0.5-unit capacitor as described in Fig. 7(b). The offset shifts the original region by 16LSB, as depicted in Fig. 6. The generated residue has a redundant area of 8LSB above and 16LSB below the original area. One can calculate the output of the PGA, including all offsets generated, as follows :

$$V_{PGA\_out} = V_{PGA\_PIX} + V_{OFF\_DARK} - (V_{REF\_P} - V_{REF\_N}) \times \frac{D_{COARSE} \times C_U}{C_{FB}} + V_{16LSB}$$

In this equation, C_{FB} and C_U are the feedback capacitor and the unit capacitor, respectively. The two-step SAR ADC has the transfer curve of the red line in Fig. 8 without distortion at coarse conversion. The minimum output code at fine conversion is 16 due to the offset, V_{16LSB}. However, if the coarse decision is wrong, the generated residue deviates from the red area in Fig. 6. Nevertheless, if the error is within the over-range marked in blue, it is possible to compensate for it during the fine conversion. For example, if the coarse conversion is wrong due to a lack of the PGA bandwidth, the transfer curve deviates from the red area, and this curve follows the transfer curve of case 2 in Fig. 8. Though the coarse conversion result is lower than expected, accurate conversion is available because the actual signal V_{PGA_PIX} is preserved. Therefore, the 1-bit redundancy covers this deviation and finally leads to the correct result. In addition, the over-range corresponds to 0.25LSB and 0.5LSB, respectively, in the case of coarse conversion. In the opposite case, the transfer curve follows the transfer curve of case 2 in Fig. 8.

IV. Measurement Result

The fabricated CMOS image sensor is designed in a TowerJazz 0.18μm CIS process technology, and the chip size is 5.0mm×5.0mm. As shown in Fig. 9, the FPGA uses a 60MHz clock from the oscillator and generates appropriate clocks to manage each block, including the image sensor. The image sensor receives a maximum 64MHz clock from the FPGA, and the FPGA captures the data from the image sensor at the receiver using a 128MHz clock. In addition, the camera-link protocol manages the communication protocol between FPGA and the computer, and the maximum data transmission speed is 1.5Gb/s.

Fig. 10 shows differential nonlinearity (DNL), integral nonlinearity (INL), and transfer curves of the readout chain designed for this sensor. In particular, the readout chain includes pixels and two source followers. In this measurement, 100 images are taken by adjusting the integration time. In the meantime, the intensity of the light source is set to 0.2 lux.

As described in Fig. 10, The DNL is +0.36/ −0.28LSB, and the INL is +0/ −12.46LSB. Table 1 compares the performance of the sensor designed in this study and previous studies. The linearity measurement result shows that the DNL result is improved compared to previous research [3-5]. However, the INL performance is not optimum. Especially the amount of current consumed inside the pixel is varied up to 2.5% depending on the signal scale output from the pixel. The deviation of the load current leads to worse linearity performance of the source follower and affects the linearity performance of the readout chain. Including the nonlinearity, the measured transfer curve is compared with the ideal one in Fig. 10(c). The graph shows that the transfer curve gradually deviates from the ideal line as the code increase. As a result, the deviation is about 1.02% at the mid code, but this deviation increases to 1.91% and 3.22% until it reaches the maximum code.

The RMS value of the measured temporal noise under dark conditions is 530μV_{rms}. The RMS value of the temporal

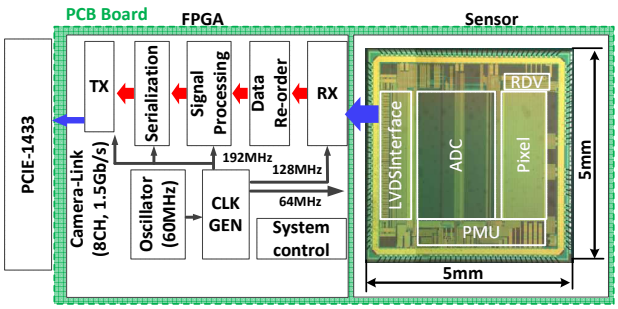

Fig. 9. The block diagram of the measurement set-up

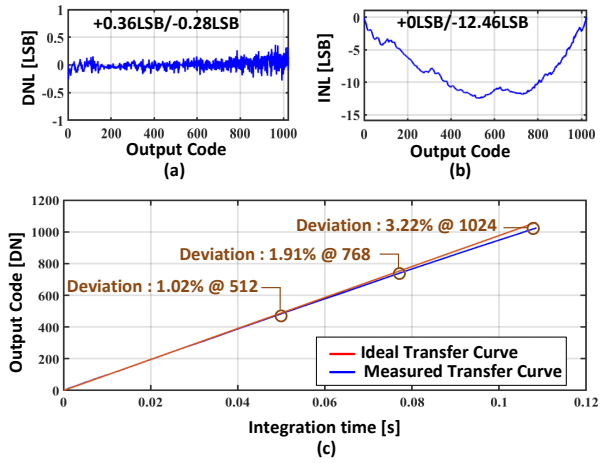

Fig. 10. Linearity measurement result: (a) DNL, (b) INL and (c) transfer curve

noise originating from the ADC, including the PGA, is about 260.1μV. These measurement results shows that the performance has been improved compared to [6]. Table 1 shows a performance comparison of image sensors designed using SAR ADCs. As shown in Table 1, [3] has a SAR ADC structure with the 4T-type pixel. Though the 4T-type pixel theoretically contributes less to the temporal noise than the 3T-type pixel, this design has a similar temporal noise level as [3]. The main reason is that the ADC design in [3] has a more than 70 times faster sampling rate. In addition, [5] designed SAR ADC with noise shaping technique. However, the comparator decision of [5] is about 10 times faster than this design, and the temporal noise level is similar to the temporal noise of this design without pixels.

V. Conclusion

An image sensor using a two-step SAR ADC has been implemented as a solution to improve the linearity. This structure effectively reduces the area occupied by the ADC and the number of switches and control lines that control the capacitor DAC. To implement this ADC, the PGA supports the generating residue. As a result, the ADC is implemented in a column-parallel structure, and the layout of the capacitor DAC array is improved by following [7] to effectively solve the systematic error. Therefore, the RMS value of the temporal noise performance is measured at about 530μV_{rms}, and the measured DNL is +0.36/ −0.28LSB.

TABLE I. Performance Summary and Comparison

Year	2023	2015	2012	2018	2022
Ref	This work	[3]	[4]	[5]	[6]
Technology	180nm 1P4M	180nm 1P4M	180nm 1P6M	90nm 1P5M	180nm 1P4M
Pixel array	316×110	15488×8776	920×256	1920×1440	316×110
Pixel type	3T	4T	4T	4T	3T
Frame rate	2500fps	60fps	9fps	50fps	3000fps
Power consumption	37.5mW	11W	-	64mW	78.5mW
Conversion gain	46.4μV/e-	58.24μV/e-	52μV/e-	-	58.24μV/e-
Full well capacity	14008e-	10005e-	4994e-	N/A	8042e-
Analog gain	×1-×8	×1-×18	-	-	×1-×8
Temporal noise	530μV_{rms} (=11.4e-)	614.4μV_{rms} (=7.68e-)	5300μV_{rms} (=61.5e-)	273.6μV_{rms}	712.8μV_{rms} (=12.2e-)
VFPN	0.036%		0.5%	0.23%	0.03%
ADC Saturation level	0.65V	0.8V	0.26V	0.7V	0.5V
Dynamic range	61.7dB	62.3dB	73dB	66.5dB	56.3dB
ADC resolution	10	12	9	10	10
ADC Sampling rate	0.25MS/s	17.95MS/s	33.3kS/s	12MS/s	0.5MS/s
DNL [LSB]	+0.36/ -0.28	+6/ -1	+1.2/ -1.2	+0.77/ -0.54	-
INL [LSB]	+0/ -12.46	-	+4/ -4	+0.81/ -0.5	-

Acknowledgment

This work was supported by the Mantis project, sponsored by the Dutch government and the EU. The authors would like to thank TowerJazz for their support in fabricating the silicon dies.

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