Multiple-Ramp Column-Parallel ADC Architectures for CMOS Image Sensors

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***Abstract*—This paper presents a CMOS imager with a column-parallel ADC architecture based on a multiple-ramp single-slope (MRSS) ADC. Like the well-known column-level single-slope ADC, an MRSS ADC uses a very simple analog column circuit, which mainly consists of an analog comparator and some switches. A prototype imager using the MRSS ADC architecture was realized in a 0.25 μm CMOS process. Measurements demonstrate that the conversion speed of an MRSS ADC is 3.3$\times$ higher than a single-slope ADC while dissipating only 16% more power. Furthermore, the MRSS ADC can be easily adapted to exhibit a companding characteristic, which exploits the amplitude-dependent nature of the photon shot noise present in imager signals. Measurements show that the resulting multiple-ramp multiple-slope ADC is 25% faster than an MRSS ADC while dissipating the same amount of power.**

***Index Terms*—A/D conversion, CMOS image sensors, column-level ADC, multiple-ramp single-slope (MRSS) ADC, photon shot noise, single-slope ADC.**

I. Introduction

THE consumer demand for imagers with more and more pixels has had a profound influence on their design. The main consequence is a marked trend towards smaller and smaller pixels, since this allows for an increase in the number of pixels without increasing die size and optical format and thus, the cost of the sensor. For instance, the smallest reported pixel size has more than halved in the last four years [1], [2]. A second consequence of an increased pixel count is that the bandwidth of the readout circuitry needs to be significantly increased in order to read out all pixels within the same frame time. As a result, column-parallel ADC architectures have become increasingly popular [3]–[8]. This is because they employ a large number of parallel ADC channels and therefore facilitate the high-speed readout of large pixel arrays.

While several types of ADCs have been used in column-parallel ADC architectures, such as the successive approximation (SAR) [3] or cyclic ADC [4], the single-slope ADC [5]–[8] is clearly the most often used. This is because a single-slope ADC can be implemented using a very simple column circuit, which mainly consists of a single comparator. As a result, a single-slope ADC will typically require much less chip area than a cyclic or SAR-based ADC. Moreover, this simple column circuit also makes it relatively easy to ensure uniformity between columns and thus minimizes the amount of column fixed-pattern noise (FPN). To a first approximation, the only analog circuit parameter that causes nonuniformity is the comparator's offset, and this can be relatively easily reduced by auto-zeroing.

However, a disadvantage of a single-slope ADC is its relatively slow conversion speed. Each n-bit A/D conversion requires 2^n clock periods, compared with only n clock cycles for both SAR and cyclic ADCs. This can limit the readout speed of the imager, particularly at higher (>10 bit) ADC resolutions, and means that, in some cases, ADC resolution must be traded in for speed [8]. While SAR and cyclic ADCs are much faster, these all require much more column-level circuitry, which significantly increases chip area and increases column uniformity problems.

To solve this speed problem, a new column-parallel ADC architecture based on a multiple-ramp single-slope (MRSS) ADC has been proposed [9], [10]. An MRSS ADC offers significantly increased readout speed, while still preserving the main advantage of the single-slope ADC: its simple column circuit. Compared with a single-slope ADC, the column circuit of an MRSS ADC only requires a number of additional switches and some digital circuitry.

An additional increase in conversion speed can be made by combining the MRSS ADC architecture with the concept of exploiting the amplitude-dependent characteristic of photon shot noise present in imager signals. This can be done by adapting the MRSS ADC such that it exhibits a companding quantization characteristic. While this concept has been suggested earlier [11], [15], few practical implementations have been reported in literature, which seems to suggest that it is relatively difficult to implement. In an MRSS architecture, a companding characteristic can be relatively easily obtained by using ramps with *different* slopes. This results in a multiple-ramp multiple-slope (MRMS) ADC, which can be faster than an MRSS ADC, without increasing power consumption or decreasing image quality. In this paper, the first measurement results of a prototype imager using a MRMS ADC will be presented.

This paper is organized as follows. In Section II, the MRSS architecture will be described. Section III discusses the implementation details of the silicon prototype. This is followed, in Section IV by measurement results. Section V describes the concept of photon shot-noise exploitation and

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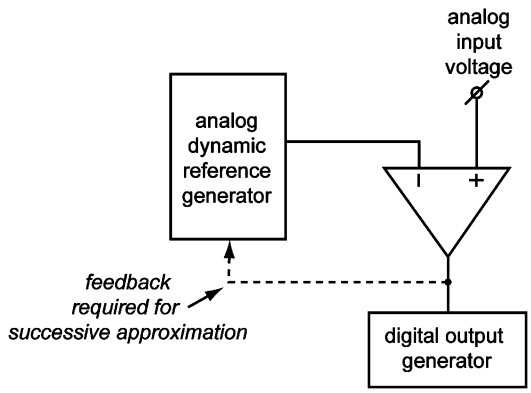


Fig. 1. Common principle of the single-slope and successive approximation ADC architecture.

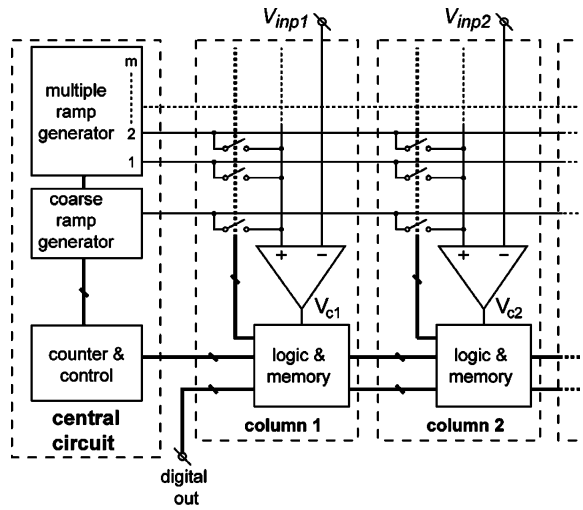
discusses how the resulting MRMS architecture can be implemented using the same silicon prototype. In Section VI, measurement results with the MRMS architecture are described. Finally, conclusions are presented in Section VII.

II. MRSS ADC Architecture

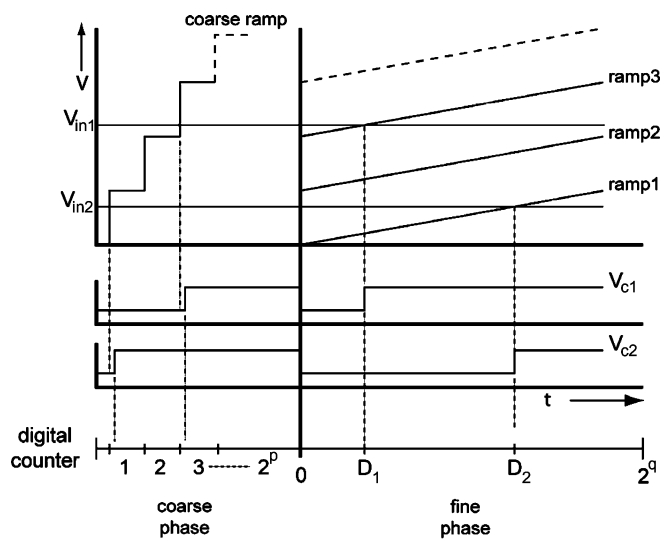
The MRSS ADC can best be regarded as a cross between a single-slope and a SAR ADC. In both cases, as illustrated in Fig. 1, the A/D conversion is performed by means of a number of comparisons between a dynamic reference signal and the analog input voltage. In the case of a single-slope ADC, the dynamic reference generator outputs a ramp voltage. While this approach is simple and robust, it requires 2^n comparisons for an n-bit conversion and is therefore slow. By using a dynamic reference generator whose output depends on the result of previous comparisons, the successive approximation ADC requires only n comparisons,. The drawback of this approach in a column-parallel ADC architecture is that it requires feedback between the comparator and the reference generator and, therefore, that the reference voltage is dependent on the input signal. In a column-parallel structure with several hundreds of comparators, this necessitates the implementation of a reference generator in each column, instead of the single, centrally implemented dynamic reference generator of a column-parallel single-slope ADC. This significantly increases chip area and makes it more difficult to ensure uniformity between columns.

The MRSS ADC has a faster conversion speed than the single-slope ADC, without requiring a reference generator in each column. The basic concept of an MRSS ADC is that the ramp voltage, which spans the entire input voltage range in a single-slope architecture, is divided into m ramps, which each span $1/m$ of the input range. If each column comparator can be connected to the correct ramp (i.e., whose span contains the input signal), all m ramps can be output concurrently, resulting in a shorter conversion time compared with a single-slope ADC.

In Fig. 2(a), a block diagram of an MRSS ADC is shown. The dynamic reference generator outputs m different ramp voltages. Each column circuit has a set of switches that connects one of the m ramps to the input of the comparator. Compared with the single-slope architecture, the MRSS architecture only requires the addition of some analog switches, as well as some extra digital memory and logic in each column.



(a)



(b)

Fig. 2. (a) Block diagram of the MRSS ADC architecture. (b) Corresponding timing diagram.

In Fig. 2(b), the operation of the MRSS architecture is further illustrated with a timing diagram. The A/D conversion is subdivided into coarse and fine phases. In the coarse phase, all comparators are connected to a single coarse ramp voltage, and a single-slope A/D conversion is performed. The results of this coarse conversion are stored in the memory in each column. Next, the coarse conversion result is fed back into the analog switches, which connect the correct ramp to each comparator. The fine conversion phase is then performed while all m ramps are concurrently output. The fine conversion is essentially a single-slope conversion, but since each comparator is connected to a ramp corresponding to the level of its input signal, each ramp only has to span $1/m$ times the ADC input range, and therefore, the conversion can be much faster. The result of the fine conversion is stored in the column memory. The final digital output is a combination of the results of the coarse and fine conversion phases.

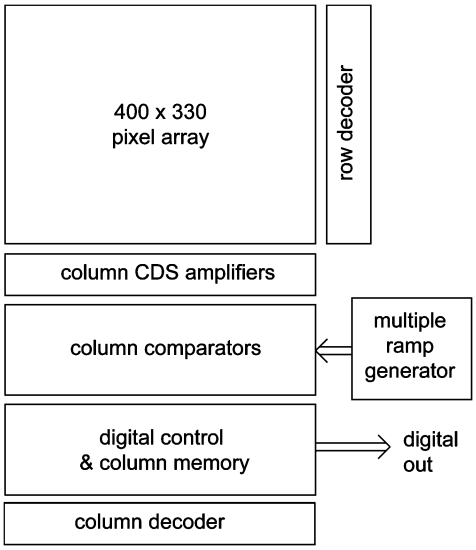


Fig. 3. Block diagram of the realized prototype imager.

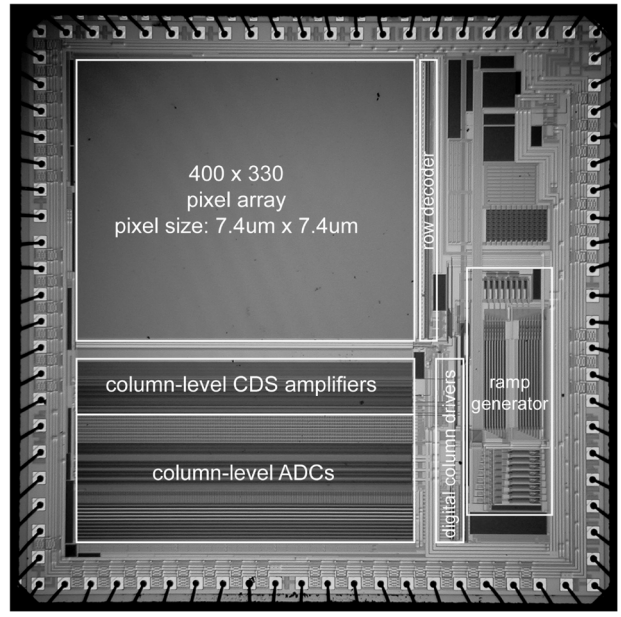


Fig. 4. Chip micrograph of the realized prototype imager. The die size is 5 mm × 5 mm.

TABLE I
SPECIFICATIONS OF THE PROTOTYPE

Technology	1P3M 0.25μm CMOS
Die Size	5mm x 5mm
Supply Voltage	2.5V (digital/analog) / 3.3V (I/O)
Pixel Pitch	7.4μm
Number of Pixels	400 x 330
Pixel Type	3T, n-well photodiodes
Column ADC pitch	7.4μm
Number of ramps	8
ADC input voltage range	1V
ADC clock frequency	20MHz
ADC resolution	10b

If the number of ramps m is equal to a power of two, i.e., $m = 2^p$, then the total A/D conversion time $T_{\rm conv}$ can be expressed as

$$T_{\rm conv} = \frac{2^p - 1}{f_{\rm ck}} + \frac{2^q - 1}{f_{\rm ck}} \quad (1)$$

where $f_{\rm ck}$ the clock frequency of the counter, p and q are integers, $p + q = n$, and n is the resolution of the conversion. The choice for p and q and, thus, the number of ramps in the ADC involves a tradeoff between conversion speed and power consumption. In Section III, this tradeoff will be further discussed as a part of the prototype implementation.

III. Implementation

A. Sensor Overview

A prototype imager with an MRSS ADC architecture was implemented in a single-poly triple-metal 0.25 μm CMOS process. The die size is 5 mm × 5 mm. The prototype has a resolution of 400 × 330 pixels and a pixel pitch of 7.4 μm. The imaging array consists of standard 3T pixels with n-well photodiodes. In Fig. 3, a block diagram of the prototype imager is depicted. Each column circuit has a separate correlated double-sampling (CDS) amplifier that drives the column comparator. Both of these circuits are reused from an existing design, as is the row decoder. The column ADC has the same layout pitch as the pixels, i.e., 7.4 μm. The ADC clock frequency is 20 MHz. The ADC resolution (limited by the noise of the comparators) is 10 bits. Most of the digital timing and control is performed off-chip by a field-programmable gate array (FPGA). This enables flexible ADC operation and timing; in particular, it is possible to operate the ADC in single-slope mode for comparison purposes. The supply voltage is 2.5 V for analog and digital circuitry and 3.3 V for digital I/O. Fig. 4 shows a chip micrograph, and Table I summarizes the prototype specifications.

B. System-Level ADC Design Considerations

As mentioned in the previous section, the main system-level design choice involves the number of parallel ramps in the MRSS ADC. According to (1), the minimum conversion time occurs for $p = q$, which would result in a conversion time of 62 clock periods for a 10-bit resolution. However, such a choice for p and q would imply that 32 ramps would be required. Two practical problems make it difficult to implement such a large number of ramps. First, each output of the ramp generator must be buffered in order to drive the capacitive load presented by a large number of comparators. Since the number of comparators connected to each ramp is signal-dependent, each buffer has to be dimensioned for the worst case situation, where it has to drive all of the comparators. Therefore, there is a tradeoff between the increased speed obtained by using a large number of ramps and the increased power dissipation of using many ramp buffers.

A second limitation stems from the fact that, if each of the m ramps only spans $1/m$ of the input range, errors in the coarse conversion phase may result in the comparator being connected to the wrong ramp during the fine conversion phase, resulting in dead bands in the final digital output. This problem can be solved by creating some overlap between the different ramps. Subsequently, the digital outputs stored in the coarse and fine memory can be correctly combined with some simple digital processing. The amount of overlap required between successive ramps is fixed and depends on the expected magnitude of the errors made in the coarse conversion phase. As a result, increasing

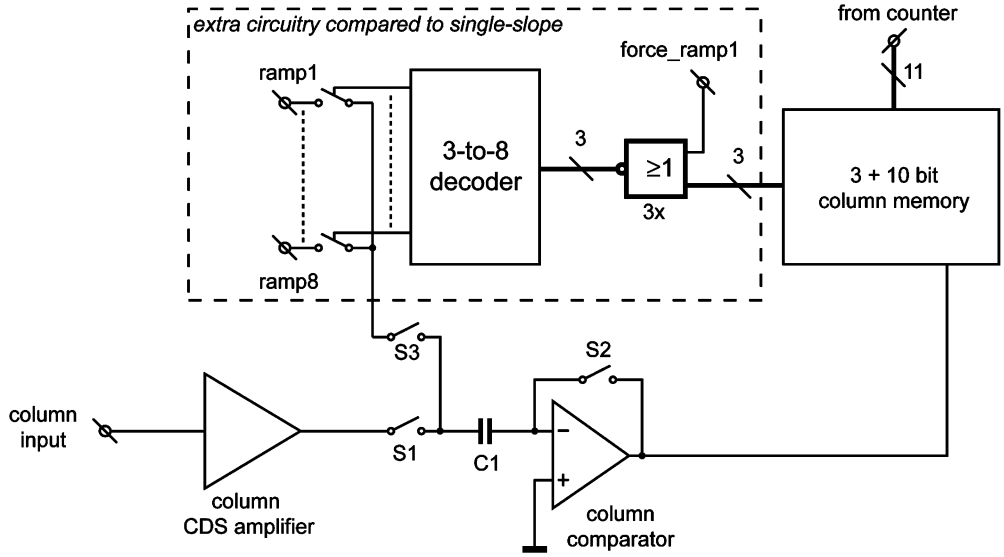


Fig. 5. Simplified block diagram of the column-level circuitry.

the number of ramps will increase the portion of each ramp that is repeated in an overlap.

Based on the above-mentioned limitations, eight ramps were used in the silicon prototype.

C. Column-Level ADC Circuitry

In Fig. 5, a simplified block diagram of the column-level circuitry is depicted. An input amplifier reads out the pixel output voltages and performs the required CDS operation. After this, the column comparator is auto-zeroed using capacitor C1 and switch S2 [6], [8]. During this auto-zero phase, the output of the column-level CDS amplifier is also sampled on C1. Next, the comparator is connected to a ramp voltage via S3. In this MRSS design, eight ramp voltages $ramp1$ through $ramp8$ can be connected to the comparator via a 3-to-8 decoder. The output of the comparator is connected to a digital memory. For clarity, the figure depicts a single memory, although two memory banks were actually implemented. This allows for simultaneous A/D conversion and digital readout of the column circuitry.

The coarse A/D conversion is performed by connecting each comparator to the same ramp voltage and performing a normal single-slope A/D conversion. Although a separate coarse ramp voltage is theoretically required during the first A/D conversion phase, in this design, the coarse voltage is supplied by the first ramp generator ($ramp1$). This is done by making the $force_ramp1$ signal high, which feeds address 0 into the 3-to-8 decoder. As a result, ramp voltage $ramp1$ is connected to the column comparator. The results of the coarse A/D conversion are stored in the column memory and are subsequently used to connect each comparator to the correct ramp, i.e., the ramp in whose range the input signal is in. This is done by making the $force_ramp1$ signal low, which connects the outputs of the digital memory to the 3-to-8 decoder, and thus connects the correct ramp voltage to the comparator. Since there are eight ramp voltages in this design, 3 bits of digital memory are required to store the result of the coarse conversion.

Next, the fine A/D conversion is performed, during which all eight ramps are operated concurrently. The results of this conversion are also stored in the digital memory. The fine A/D conversion theoretically yields 7 bits of resolution, and an extra bit is required to encode the overlap between the ramps that is required for robustness. As a result, 8 bits of digital memory are required for the fine conversion phase; however, 10 bits of memory were implemented in the prototype to allow the column circuit to operate as a 10-bit single-slope ADC for comparison purposes. This can easily be done by making $force_ramp1$ high and feeding a ramp voltage via $ramp1$. Some simple digital hardware is required to reconstruct a 10-bit integral digital code from the overlapping $3 + 8$-bit raw digital output. This is done in the off-chip FPGA.

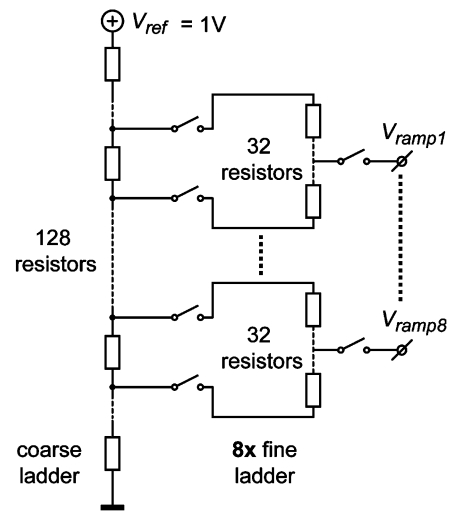


Fig. 6. Resistor ladder DAC concept used for the multiple-ramp generator.

As can be seen from Fig. 5, compared with the classical single-slope ADC, the only additional column-level circuitry required to implement an MRSS ADC consists of eight analog switches, a 3-to-8 decoder and three NOR gates. This underlines the advantage of the MRSS architecture, as it offers significantly higher conversion speed while retaining a simple column circuit.

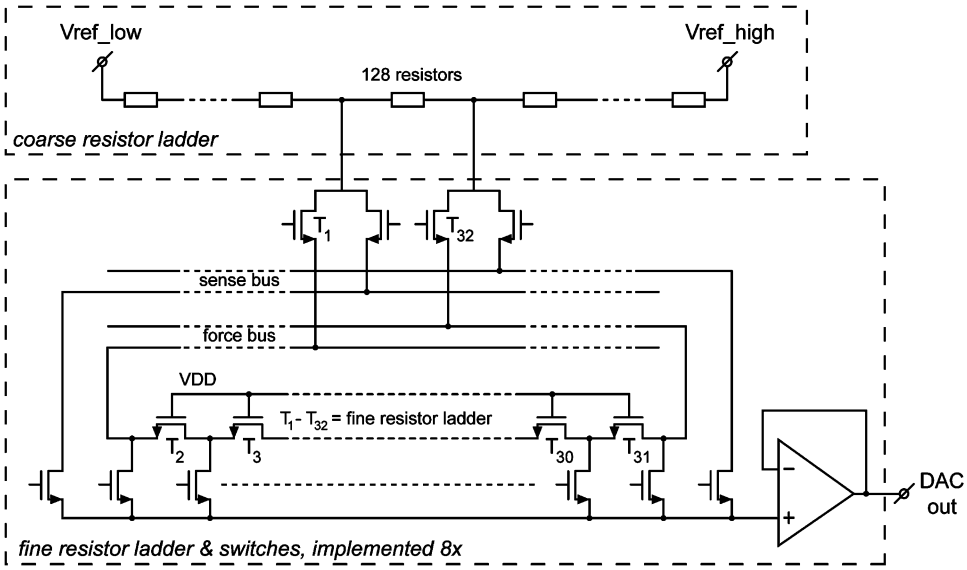


Fig. 7. Circuit diagram of the multiple-ramp generator.

D. Multiple-Ramp Generator

In order for an MRSS ADC to have a linear response, it is imperative that the multiple ramps are well matched, i.e., their slopes are equal and their offsets are well defined. In order to achieve this matching, the multiple ramp generator was implemented as a set of eight matched DACs with 12-bit resolution. This allows for a lot of flexibility in the prototype, as each ramp voltage is fully programmable via a digital interface to the aforementioned off-chip FPGA.

The DAC architecture used for the multiple-ramp generator is based on a resistor ladder DAC first published in [12] and is illustrated in Fig. 6. A single coarse resistor ladder, consisting of 128 resistors, is connected to a reference voltage of 1 V. To this coarse resistor ladder, eight fine ladders, each consisting of 32 resistors, are connected as shown. In the implementation, a full set of switches and digital decoders is available for each of the fine resistor ladders, resulting in eight output voltages that are fully programmable. At the same time, the uniformity between the output voltages depends mostly on the matching of the resistors in the coarse ladder. These resistors should match within 0.8% in order to get 10-bit precision, which can be achieved by careful layout.

A major source of error in the DAC is the fact that the fine ladders load the coarse ladder. Each fine resistor ladder thus reduces the effective resistance of the unit coarse resistor to which it is connected. A second source of error is due to the fact that the switches connecting the fine ladder to the coarse ladder have a certain on-resistance, which is in series with the outer unit resistors of the fine ladders. In [12], both of these problems were solved by placing unity-gain buffers between the coarse and fine ladders. However, this would require 16 additional amplifiers in this design, which would considerably increase chip area and power consumption. Therefore, a direct, passive connection between coarse and fine resistor ladders was used, and the resulting voltage errors were minimized as follows. First, the error caused by the resistive loading of the coarse ladder by the fine error can be minimized by a proper choice of unit resistor values. Based on ladder biasing current and thermal noise considerations, the unit resistors were chosen to be 29 Ω and 1.6 kΩ for the coarse and fine ladders, respectively. With these choices, the total resistance of the fine ladder is 51 kΩ, and this total resistance is switched in parallel with a coarse unit resistance of 29 Ω. It is clear that the resulting errors are much less than 0.5 LSB.

In order to keep the voltage error caused by the on-resistance of the switches below 0.5 LSB, the on-resistance should be less than 0.25 times the fine resistance, or 400 Ω. This leads to large switches and thus results in an intolerable amount of charge injection at the required switching speed of 20 MHz. To reduce this, the resistors of the fine ladder were implemented with nMOS transistors, with the outer transistors of the fine ladder functioning as both switches and resistors, as is illustrated in Fig. 7. Since the switches' on-resistance can now be 4× higher, a considerable reduction in their size, and hence, their charge injection can be achieved. In order to output the voltage at the coarse resistor ladder nodes, a separate set of sense switches is implemented, since the switches T_1 and T_{32} conduct current and thus have a voltage drop across their channels.

The outputs of the fine resistor ladders are buffered by folded-cascode opamps, which drive the column circuits. The offset of these buffers will give rise to offset between the ramps. This is corrected by the following auto-calibration algorithm. One of the 400 column comparators is disconnected from its CDS amplifier and is instead directly connected to $ramp1$, as illustrated in Fig. 8(a). This test column circuit samples a test voltage V_{testk} output by $ramp1$ at the same time that the other column comparators sample the outputs of the column CDS amplifiers [Fig. 8(b)]. Since the test voltage V_{testk} corresponds to the middle of $rampk$ ($k = 2 \ldots 8$), the test column circuit will certainly select $rampk$ during the coarse conversion phase. The subsequent fine conversion phase now becomes a comparison between V_{testk} that is output by $ramp1$, and $rampk$. If there is no offset between these ramps, this should result in a digital output that corresponds exactly to the middle of

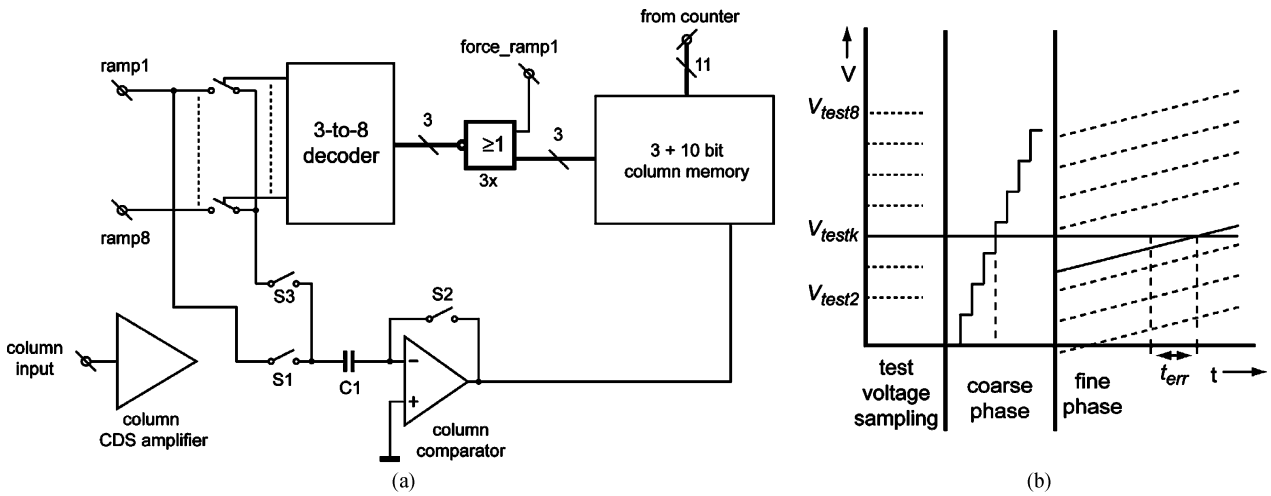


Fig. 8. (a) Circuit diagram of the test column used for auto-calibration. (b) Corresponding timing diagram.

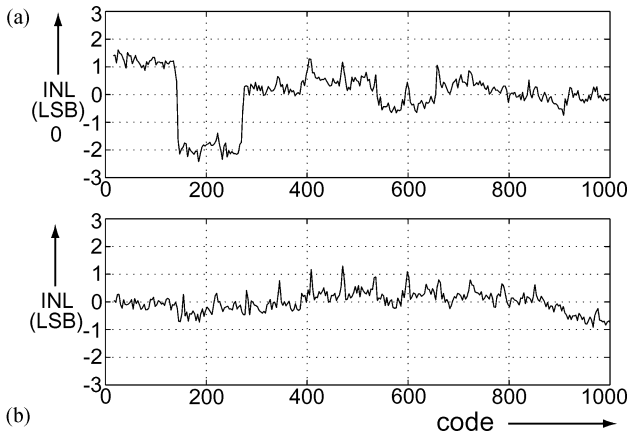


Fig. 9. Measured averaged INL at 1 MHz. (a) Without auto-calibration. (b) With auto-calibration.

Fig. 10. Image captured with the column ADC in single-slope mode at 50 fps.

Fig. 11. Image captured with the column ADC in MRSS mode at 142 fps.

$rampk$. However, due to offset between $ramp1$ and $rampk$, a certain error t_{err} will exist in the fine conversion. This error is now available in the digital domain, where it is averaged and subsequently used to correct $rampk$, which can easily be done by changing the code assigned to the initial voltage of $rampk$. Finally, by repeating this auto-calibration procedure for $k = 2$ through $k = 8$, all offsets between the ramps are removed.

IV. MRSS ADC Measurement Results

In order to separately evaluate the performance of the ADC, the prototype imager was equipped with a test input through which a common input voltage could be fed to all columns. Using this test input, INL measurements were performed at a clock frequency of 1 MHz (Fig. 9). In Fig. 9(a), the INL is shown without auto-calibration. Offset between the ramps leads to significant nonlinearity, which are visible as discrete "jumps" in the INL graph. Fig. 9(b) shows the INL with the auto-calibration algorithm applied. It clearly demonstrates the effectiveness of the auto-calibration scheme.

Fig. 10 shows a measured image at 50 fps with the column ADC in 10-bit single-slope mode. At a clock frequency of 20 MHz, the line time is 58 μs, of which 53 μs is used for the A/D conversion. Fig. 11 shows a measured image at 142 fps with the column ADC in 10-bit MRSS mode. The A/D conversion is now performed in 16 μs, reducing the line time to

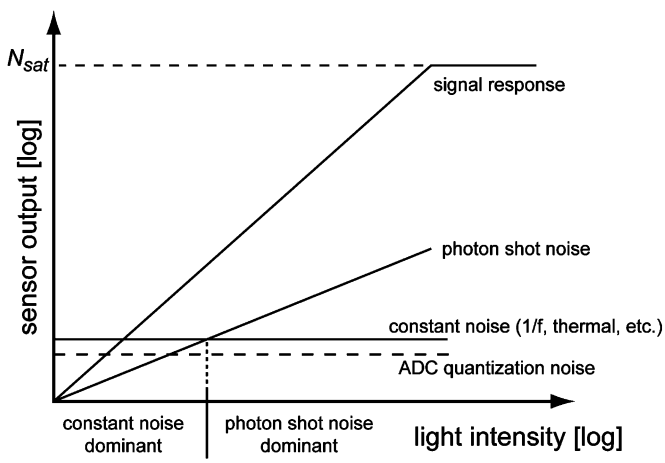


Fig. 12. Conceptual logarithmic plot of the sensor's response to light and corresponding noise sources.

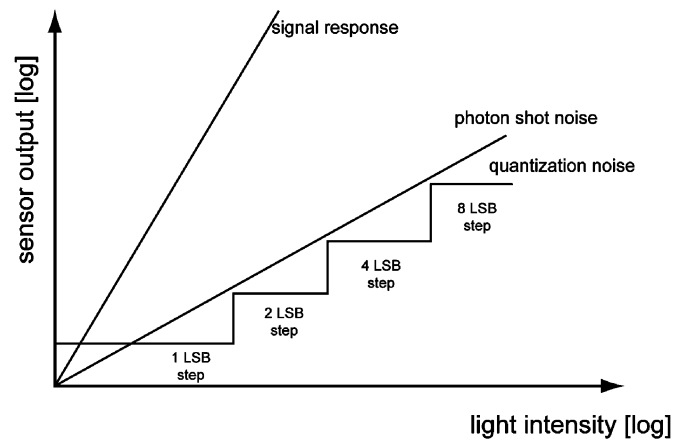


Fig. 13. Exploitation of photon shot noise in an imager ADC by increasing the quantization step in binary fashion.

21 μs. The power consumption of the prototype is 52 mW, of which 30 mW is used by the column CDS amplifiers and comparators, 8 mW by the ramp generator, and 14 mW by the digital and I/O circuitry. Therefore, the MRSS ADC achieves a 3.3$\times$ decrease in conversion time compared to a single-slope ADC. This is a significant improvement, which underlines the potential of the MRSS ADC architecture. The increased speed does require some additional power consumption, since the MRSS ADC requires eight ramp generators instead of only one. Since each ramp generator requires 1 mW, the increase in power consumption is 7 mW or 16%.

V. Exploiting Photon Shot Noise: MRMS ADC

A. Photon Shot-Noise Exploitation in Imager ADCs

In Fig. 12, the response of an imager pixel is plotted on a logarithmic graph along with the various noise sources. The sensor's output increases linearly with light intensity until its output saturates at a level $N_{\rm sat}$, which is usually expressed in electrons of charge that can be stored on the capacitive node of the sensor. Most of the noise sources are independent of light intensity, and therefore form a constant "noise floor," which limits the dynamic range of the imager. Imager ADCs are usually designed such that their quantization noise level is lower than this noise floor.

However, an imager output signal also contains photon shot noise, which can be expressed as follows:

$$e_{\rm phs}(N_{\rm sig}) = \sqrt{N_{\rm sig}}. \tag{2}$$

Here, $e_{\rm phs}(N_{\rm sig})$ is the photon shot noise, which depends on the signal level $N_{\rm sig}$ (both expressed in electrons of charge). Because photon shot noise is dependent on the input signal, it becomes the dominant noise source at higher light intensities. In this part of the input range, the ADC has a better noise performance than is required, i.e., its quantization noise can be increased without decreasing the overall noise performance. This is equivalent to increasing the quantization step size in the ADC and therefore reducing the total number of quantization levels of the ADC. This leads to an ADC with a companding characteristic [13], in which the reduced number of quantization steps can be exploited to yield lower ADC power consumption or higher conversion speed.

While several companding characteristics exists, such as the logarithmic μ-law [13] or A-law [14], several digital postprocessing steps commonly performed in CMOS imagers, such as white-balancing or gamma correction, require digitized sensor outputs that are linearly dependent on the input light level. Therefore, to facilitate the reconstruction of a linear output code in the digital domain, it is preferable to use integer multiples of the quantization step size used for the smallest input signal. An example of such a scheme is illustrated in Fig. 13. Here, the quantization step size is doubled several times with increasing light intensity. In applying such a *binary* increase of the quantization-step size, it is necessary to calculate at which input levels the quantization step size, and therefore the quantization noise, can be doubled, without increasing the overall noise too much. In order to quantify this allowable noise increase, a quality parameter r is defined as follows:

$$r = \frac{e_{\rm qns}(k)}{e_{\rm phs}(N_{\rm sig})}. \tag{3}$$

Here, $e_{\rm qns}(k)$ is the quantization noise of the ADC depending on the step size k ($k = 1, 2, 4, 8, \ldots$). As is well known, the quantization noise can be expressed in terms of the quantization step size as follows:

$$e_{\rm qns}(k) = k \cdot \frac{e_{\rm lsb}}{\sqrt{12}}. \tag{4}$$

Here, $e_{\rm lsb}$ is the quantization step size. For an optimal ADC design, the input range of the ADC should be matched to the maximum output swing of the sensor, i.e., the saturation level of the sensor. This can be expressed as follows:

$$N_{\rm sat} = 2^n \cdot e_{\rm lsb}. \tag{5}$$

Here, n is the (linear) resolution of the ADC in bits. Combining expressions (2) through (5) yields the following expression:

$$N_{\rm sig} = \left(\frac{N_{\rm sat} \cdot k}{2^n \cdot \sqrt{12} \cdot r}\right)^2 \tag{6}$$

TABLE II
EXAMPLE OF A BINARY QUANTIZATION STEP INCREASE SCHEME

Step size (LSBs)	1x	2x	4x	8x	***Total:***
Nr. of steps:	204	305	611	105	***1225***

where N_{sig} is the input signal level at which the ADC can double the quantization step size, while still maintaining the required ratio between quantization noise and photon shot noise, as defined by the quality factor r in (3).

By evaluating (6) for increasing k, all of the points at which the quantization noise can be doubled are obtained. Using this result, the total amount of quantization steps can be computed. An example of such a calculation is given in Table II. For this computation, N_{sat} was chosen to be 25 000 electrons, the initial resolution n was 12 bit, and the quality parameter r was set to 0.1. The latter is a conservative setting, ensuring that the quantization noise increase will not be visible in the image. As can be seen in Table II, 1225 quantization steps are required for an effective resolution of 12 bit. This is a considerable reduction over normal linear quantization, where 4096 steps would be required.

The main challenge in the design of such a companding ADC is to actually translate the reduced number of quantization levels into increased conversion speed or reduced power consumption. So far, it seems that the only companding ADC implementations for CMOS imagers have been based on a column-parallel single-slope ADC [11], [15]. As will be shown in the next section, however, the MRSS ADC can be advantageously modified to create a companding characteristic.

B. A Multiple-Ramp Multiple-Slope (MRMS) ADC

In order to implement a companding characteristic in an ADC, the quantization step must be varied along the input range. In an MRSS ADC, the quantization step size is equal to the increase in the ramp voltage during one clock period of the system-level counter. Therefore, the quantization step size can be doubled by doubling the slope of the ramp. As there are several ramps in the ADC, the input level at which the quantization step size increases can be chosen such that it coincides with the transition point between the ramps. This results in the timing diagram depicted in Fig. 14. As can be seen in the figure, the ramps have different slopes; however, unlike an implementation of companding in a single-slope ADC, the slope of the ramps is not changed during an A/D conversion, which reduces the potential for glitches and nonlinearity of the ADC. Because the ramps now operate at different slopes, the combination of an MRSS architecture and companding is called a *multiple-ramp multiple-slope* (MRMS) ADC.

Since the prototype chip described in Section III uses programmable DACs as a multiple-ramp generator, the MRMS ADC can be realized in this prototype without any hardware changes. The prototype ADC has an initial resolution of 10 bit. When operating in MRSS mode, the fine conversion phase takes 128 clock periods. In MRMS mode, this phase can be reduced to 64 clock periods by reducing the number of quantization levels, as is detailed in Table III. A key requirement for this MRMS mode is that the slopes of the various ramps have an exact integer relationship. The resistor-ladder DAC

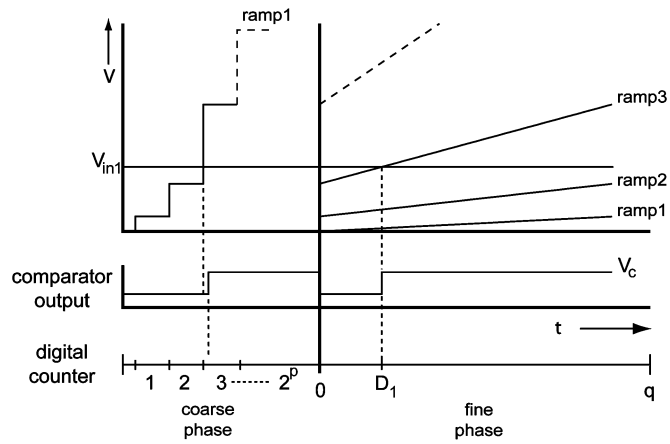


Fig. 14. Timing diagram of an MRMS ADC.

TABLE III
COMPANDING SCHEME USED IN THE PROTOTYPE MRMS ADC

Ramp nr.	***Slope***	***Nr. of LSBS***
1	1x	64
2	1x	64
3	2x	128
4	2x	128
5	2x	128
6	2x	128
7	2x	128
8	4x	256

structure is very well suited for this, since it not only ensures a well-matching voltage offset between the ramps, but also ensures matching of the LSB voltages, and thus the slopes will have an integer relationship. Like in MRSS mode, the residual offset of the DAC output buffers is reduced by using the auto-calibration algorithm described in Section III.

VI. MRMS ADC MEASUREMENT RESULTS

In order to verify that the ADC has a linear response in MRMS mode, an INL measurement similar to that of Fig. 9 can be performed by applying an appropriate test voltage to the ADC test input. This results in the INL graph of Fig. 15. It clearly shows that the MRMS ADC exhibits the same level of linearity as the MRSS ADC.

Figs. 16 and 17 show a measured image in MRSS and MRMS modes, respectively.[1] As can be seen from these figures, the application of companding does not lead to visible artefacts in the image. In the prototype, the MRMS mode conversion time is 12.8 μs, compared with 16 μs in MRSS mode or 53 μs in single-slope mode. While the 25% reduction compared with the MRSS mode might not seem significant, it is important to note that, for ADCs with more than 10-bit resolution, i.e., whose (initial) quantization noise is smaller, companding will lead to even larger reductions in conversion time. Both images were captured at 142 fps; although the lower conversion time in the MRMS mode should enable a higher frame rate, this was limited by the maximum readout speed of the digital column memory.

[1]Although the MRSS image of Fig. 16 is taken with exactly the same sensor settings as that of Fig. 11, it is nonetheless included as a reference, since the measurement setup was moved between the MRSS and MRMS measurements, resulting in a slight change in scenery and lighting conditions.

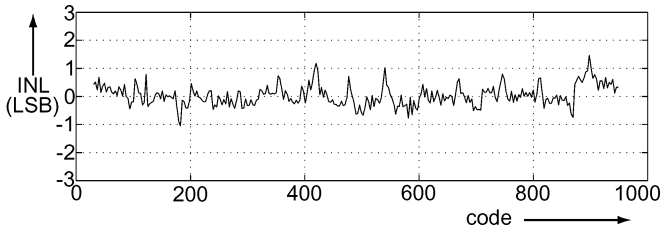


Fig. 15. Averaged INL measurement of the MRMS ADC at 1 MHz.

Fig. 16. Captured image with the column ADC in MRSS mode at 142 fps.

Fig. 17. Captured image with the column ADC in MRMS mode at 142 fps.

VII. Conclusion

A CMOS image sensor with a column-parallel ADC architecture using an MRSS ADC has been described. This new type of ADC achieves significantly higher conversion speeds than the often-used column-level single-slope ADC, while retaining a simple column circuit. A prototype imager with an MRSS ADC was implemented in a 0.25 μm CMOS process. The column-level ADC circuit only requires a comparator, eight switches, and some digital logic. Compared with a single-slope ADC, the prototype achieves a 3.3$\times$ reduction in A/D conversion time at a power increase of about 16% and thus shows the potential of this new ADC architecture to increase power efficiency, speed, and chip area of column-level ADCs.

The MRSS ADC can be combined with the known concept of exploiting photon shot noise in imager signals to reduce A/D conversion time, resulting in an MRMS ADC. Due to its flexible design, the above-mentioned MRSS prototype can also be used in MRMS mode. Measurement results show a 25% reduction in conversion time compared to a MRSS ADC. Moreover, this reduction will be larger for ADCs with more than 10 bit resolution.

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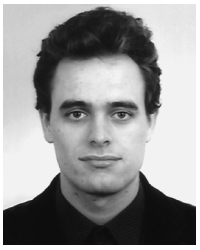

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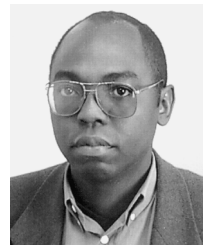

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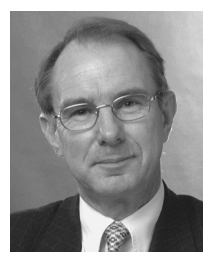

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