The Hole Role in Solid-State Imagers

Albert J. P. Theuwissen, *Fellow, IEEE*

***Abstract*—The importance of holes present in the pixels of solid-state image sensors is described by Theuwissen *et al.* (*IEDM Tech. Dig.* 2005, p. 817). Today's success of digital imaging is based on the positive effect of an accumulation layer that reduces the interface-related dark current and dark current fixed-pattern noise. This superb imaging feature is applied in charge-coupled devices as well as in complementary metal–oxide–semiconductor devices, in consumer as well as in professional equipment. Holes are not only used to improve the dark performance of imagers; other examples of efficient use of holes are fixing electrostatic potentials, creating gate structures, draining photon-generated charges, and constructing antiblooming means.**

***Index Terms*—Charge-coupled device (CCD) image sensors, CMOS image sensors, pinned photodiodes (PPDs).**

I. Introduction

HOLES PLAY a very important role in determining the quality of images obtained by solid-state image sensors. First, holes can be used to fix the electrostatic potential in the charge-coupled device (CCD) and CMOS pixels. Second, holes can be seen as a kind of by-product in the generation process of the video signal: Absorbed photons in the silicon result in the generation of electron–hole pairs. It seems to be quite straightforward, but one needs to get rid of these holes in a proper way; otherwise, they can drastically hamper the intended functionality of the imager.

Once the excess holes are drained, the next step can be taken, and that is to make use of the holes to improve the quality of the imager. The pinned photodiode (PPD) [2] is probably the best example of the latter statement and is a well-known and popular element used in CCD and CMOS image sensors. Through the presence of the holes at the $Si-SiO_2$ interface, the surface contribution to dark current is drastically reduced. However, holes do play a much broader role in improving the imaging function than just reducing the dark current. They are key in the functionality of clocked antiblooming [3], in noise reduction, and in the definition of clock phases. Examples of the latter are the open-phase pinning [4], multiphase pinning (MPP) [5], and the virtual phase clocking [6].

This paper will give an overview of the role that holes can play in today's pixels of imaging systems. It will show a historical overview as well as state-of-the-art work in the field of CCDs as well as CMOS imagers.

Manuscript received May 1, 2006; revised August 17, 2006. The review of this paper was arranged by Editor J. Hynecek.

The author is with DALSA Semiconductors, 5656AE Eindhoven, The Netherlands (e-mail: albert.theuwissen@dalsa.com).

Color versions of all figures are available online at http://ieeexplore.ieee.org.
Digital Object Identifier 10.1109/TED.2006.885545

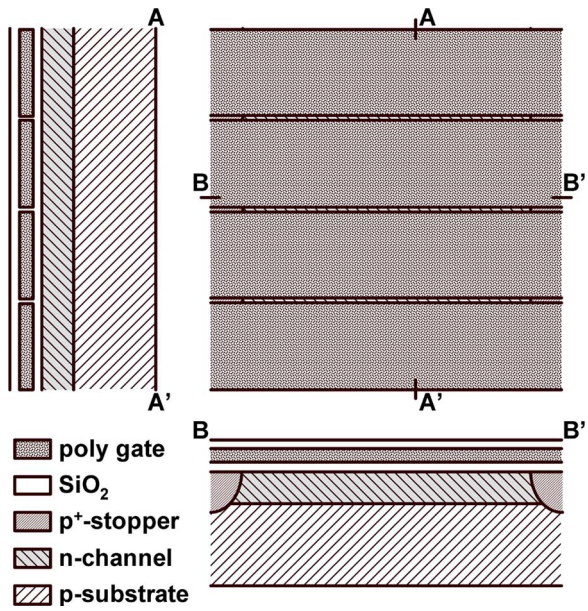

Fig. 1. Top view and cross sections of a four-phase CCD with polysilicon gates fabricated on a p-type Si substrate.

II. Holes Used to Fix Potentials in the Pixels

A crucial part of a properly functioning pixel of an image sensor is well-defined electrostatic potential at any point or region within and between pixels. If there exists an area or region (n-type or p-type) within a pixel without an appropriately defined voltage, the pixel might lose part of its functionality. The simplest example is the separation of pixels by means of p^+-channel stopper implants in CCDs or p^+ isolation regions between CMOS pixels. The CCD channel separation is illustrated with an example shown in Fig. 1: A top view and cross sections are shown of an n-type CCD channel sandwiched between two p^+-channel stopper regions [7]. From the top view and the cross section $A-A'$, it can be seen that the pixel is defined by means of four polysilicon CCD gates. In the cross section $B-B'$, the n-type CCD channel can be recognized as being built between two p^+-channel stopper regions on a p^--type substrate. The channel stoppers and the nondepleted p^--substrate form a huge and rigid structure in which the n-channels are imbedded. The p^--substrate acts as a backplane to which all the individual channel stopper regions are electrically connected. By definition, the channel stopper has the same electrostatic potential as the substrate.

Notice that impinging photons will generate electron–hole pairs in the silicon. The electrons will get collected in the CCD channel. The holes will flow to the lowest potential in the structure, the p-type substrate, and the channel stopper regions. The latter acts as a low-resistivity interconnect toward the electrical contact of the p-type substrate.

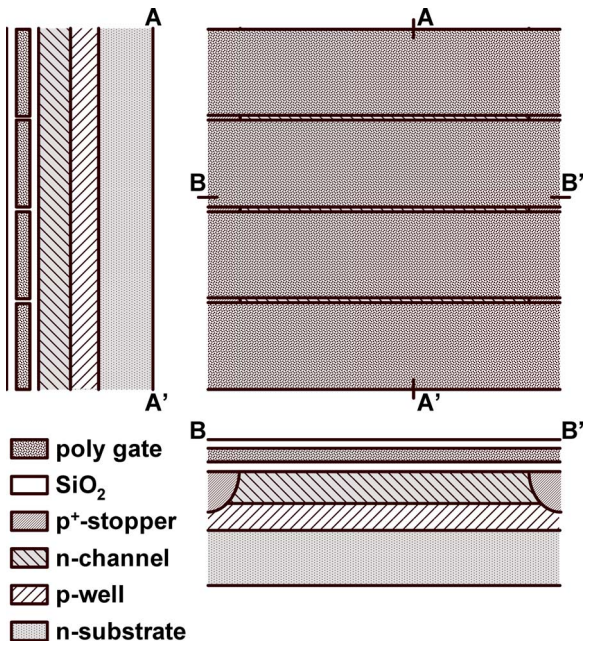

Fig. 2. Top view and cross sections of a four-phase CCD with polysilicon gates fabricated in a p-well on an n-type Si substrate.

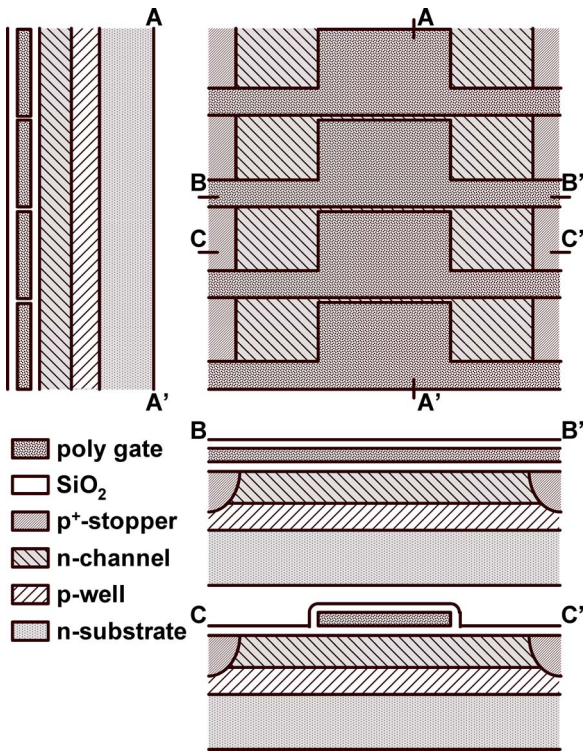

Fig. 3. Top view and cross sections of a four-phase CCD with polysilicon gates fabricated in a p-well on an n-type Si substrate. The polysilicon CCD gates are provided with holes to create a two-phase architecture underneath every single gate and/or to create windows to enhance the light sensitivity.

The situation changes when the imager is built on a depleted p-well in a nondepleted n-substrate as shown in Fig. 2. This illustration again shows cross sections and a top view. This architecture is very popular for devices that make use of vertical antiblooming. The vertical n (CCD channel) –p (well) – n^- (substrate) acts as a bipolar transistor in punchthrough at the moment the CCD channel is filled with electrons [7]. This is made possible through an appropriate biasing of the structure with a low voltage on the fully depleted p-well and a high voltage on the n-substrate. With respect to the hole role, the concentration of holes in the channel stoppers now becomes very important, because the channel stopper regions are no longer backed up by means of the large nondepleted p-well! Photon-generated holes have to find their way out of the pixel through the channel stopper finger structure. This aspect will be further highlighted in Section IV.

A relatively old technique to create a two-phase clocking system [8] and/or to increase the blue sensitivity of the imager [3] can be found in the so-called light windows cut in the polysilicon gates. The result is shown in Fig. 3. The open areas in the CCD gates are clearly visible in the top view as well as in the cross section C−C′. "Blue" photons can be absorbed in the polysilicon CCD gates that cover the substrate. However, in the case of open areas in the CCD gates, considerably more "blue" photons will reach the substrate of the imager and will drastically increase the blue sensitivity. On the other hand, the width of the gate that is covering the silicon in region C−C′ is much smaller than the width of the gate that is covering the silicon in region B−B′. This results in a lower channel potential at the cross section C−C′ in comparison to the channel potential at cross section B−B′, with the same electrostatic potential applied to the gates. In this way, a two-phase transporting CCD can be created in which the transport and storage part can be formed underneath a single poly-Si gate.

Despite these advantages, notice that parts of the depleted n-type CCD channels are not covered by gate material. In this way, their electrostatic potential is not defined! Such a structure will suffer from serious charge transport issues during its operation, because charge can and will be trapped in local potential pockets. The effect can simply be solved by defining the potential in the open areas through an extension of the p^+-channel stopper. A simple self-aligned p-implant of $2 \cdot 10^{13}/\text{cm}^2$ B-ions after the gate construction is sufficient to extend the channel stop area to the gate edge and, consequently, fix the potential in the open areas. The result after this self-aligned implant is shown in Fig. 4. The presence of enough holes plays a crucial role in fixing the potential for the regions normally "beyond control" of the gates. [Is this structure the mother of the PPD or buried diode or hole-accumulation device (HAD)?]

III. Holes Used to Create Gates

In the examples shown in Figs. 1–4, the holes are used to fix the potential in the part of the structure where no electrons are transported. In all these figures, the CCD channel runs from top to bottom in the top view, and electrons are stored and transferred underneath the gates. These gates are oriented perpendicularly to the channel. In classical CCD structures, this transport of electrons is guided by means of digital pulses supplied to the CCD gates. In principle, not all the gates of a pixel need to be clocked, some gates might also be fixed at a certain potential, and in this way, they create a potential barrier

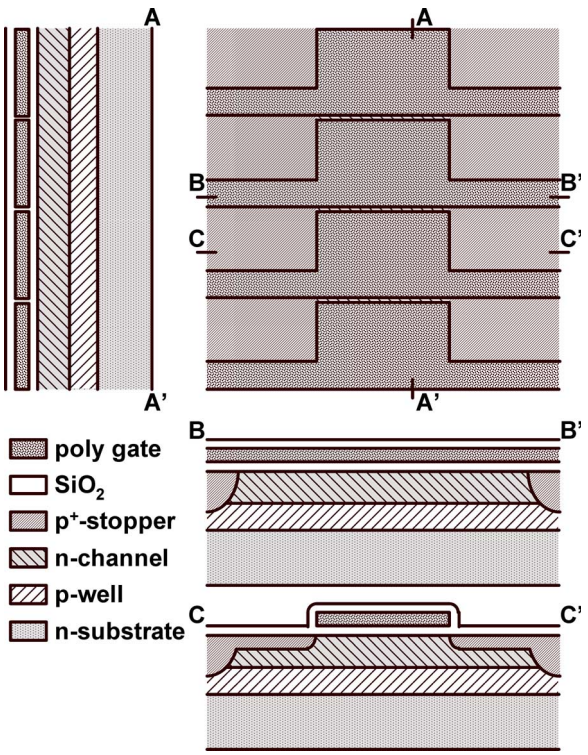

Fig. 4. Same structures are given as shown in Fig. 3, but with an additional self-aligned p^+-implant to extend the stopper region.

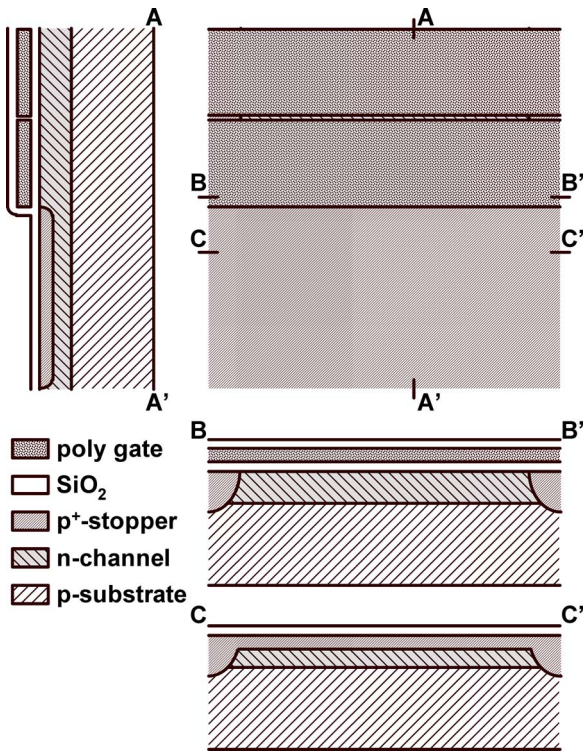

Fig. 5. Top view and cross sections of a three-phase CCD with two polysilicon gates in combination with one phase pinned at the substrate potential fabricated on a p-type Si substrate.

in the silicon. A typical example is, for instance, the output gate located between the last clocking gate of a CCD and the floating diffusion. A similar structure exists in CMOS pixels, especially in the active pixel sensor (APS) photogate structure: The gate used to separate the floating diffusion from the photogate is also a dc-biased gate. The latter is set to a well-defined potential by means of an (adjustable) dc voltage. However, a simple p^+-layer at the $Si-SiO_2$ interface above the n-buried CCD channel can substitute such a nonclocking or dc-biased gate, resulting in a local potential barrier in the silicon. The limitation of such a "p^+-layer dc gate" is the fact that the p^+-layer is internally biased to the p-substrate or p-well potential and is no longer separately adjustable.

A structure making use of a p^+-layer to construct a potential barrier in every pixel is known as an open-pinned phase (OPP) CCD and is illustrated in Fig. 5 [4]. The illustration is based on Fig. 1, in which two gates are replaced by a shallow p^+-implant. In this way, the interface potential is fixed or pinned to the potential of the p-substrate and p^+-channel stops. The channel potential underneath these open gates is fully determined by the doping levels in the fully depleted n-channel and the nondepleted p-substrate.

The open-pinned phase is, in principle, a similar application of holes as mentioned before: A p^+-layer is used to locally fix the electrostatic potential at the $Si-SiO_2$ interface. A further extension of the idea to create equivalent gate structures by means of a pinning layer can be found in the virtual phase CCD (although discussed here after the OPP, the VP-CCD was invented before the development of the OPP). A top view and the cross-sections are shown in Fig. 6 [9]. Each pixel consists of a clocked CCD gate ($B-B'$) and a fixed virtual gate ($C-C'$, made by means of the p^+ top implant). To provide the CCD with a well-defined transport direction, extra n^--regions are defined underneath the clocked CCD gate as well as underneath the virtual phase. The regions underneath the extra n^--implants act as storage areas for the charge packets, the regions without the n^--implants are used as potential barriers to define the charge-transport direction. Despite some drawbacks, the virtual-phase CCD has some interesting advantages, i.e., the device is characterized by an increased light sensitivity (especially in the blue), low surface dark-current component, a relatively simple clocking sequence, and high yield. These benefits are only applicable due to the presence of holes at the interface!

IV. Holes Used to Drain Photon-Generated Charges

Photons that are absorbed in the silicon create electron–hole pairs. Many engineers focus on electrons during imager design. However, one has to keep in mind that generated holes need to be handled by the imager as well. If this drainage or removal is not done properly, the holes can drastically hamper the proper function of the imager. To make sure that this is not the case, the photon-generated holes need a low-resistivity path to a ground connection or to another low voltage.

For devices that are built on nondepleted p-type substrates (see Fig. 1), the drainage of the holes is straightforward. In these cases, the holes can flow in vertical direction (third dimension) to the p-type substrate and can be drained through the ground or low-voltage connection of the p-type substrate. The p-type

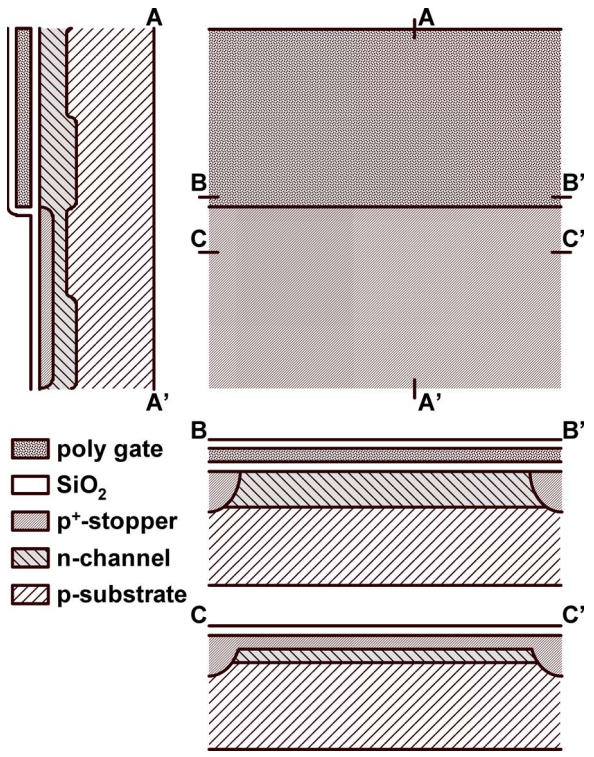

Fig. 6. Top view and cross sections of a virtual-phase CCD with one polysilicon gate in combination with one phase pinned at the substrate potential fabricated on a p-type Si substrate. Both phases have an extra n-type implant to create a deep potential well under each phase.

substrate is located underneath the complete sensor surface, is quite large in area, and has a low electrical resistivity. The situation described is typical for CMOS imagers and CCD imagers fabricated on standard p-type substrates. However, it is important to notice that the "connection" between the sensor surface and the p-type substrate (e.g., photodiodes and photogates) needs to be made by nondepleted p-regions. In many cases, the substrate is composed of p^+ material with a p^- epitaxial layer on top. The latter needs to be nondepleted; otherwise, the holes will not find their way to the p^+ substrate material.

This situation is typically the case in front-side illuminated CCDs that are built in a p-well on top of an n-type substrate. The holes need to be drained through the p-well. However, in the case that the p-well is part of a vertical antiblooming structure, it needs to be completely depleted, and successful drainage of the holes by means of only the p-well is no longer possible! This effect is shown in Fig. 4. A similar situation is present in devices built on silicon-on-insulator (SOI) in which the complete (thin) backing silicon layer is depleted. In the case of such an SOI pixel, electron–hole pairs will be generated, and the electrons will be collected in the pixels. What happens to the holes then? If not every pixel is provided with a dedicated hole drain, the pixel will not function.

To maintain a proper functionality of the imager built on an n-type substrate and in the case that the p-well is fully depleted, the device needs to be provided with p^+-channel stopper regions that have an extra function next to the separation of the CCD channels: the drainage of the photon-generated holes. Notice that:

1) the amount of holes to be drained can be very large (e.g., 100 000 times of overexposure in a 9 μm $\times$ 9 μm pixel that has a saturation level of 100 000 e^- results in a total drainage of 10^{10} holes per pixel), and;
2) the length of the channel stoppers can be very large as well (e.g., worst case 12 mm in a device of 36 $\times$ 24 mm, 1 μm in width, or a total of 12 000 squares).

A significant voltage drop can be generated by means of the hole drainage through the long channel stopper lines. These voltage drops can result in local nonuniformities and artifacts in the center of a highlight ("black smear") if the doping level of the channels stoppers is too low. If the proper operation of the sensor asks for voltage drops less than 1 V, the overall doping level of the channel stoppers needs to be high enough to allow the excess hole current to flow, e.g., $5 \cdot 10^{13}/\text{cm}^2$ [10].

V. Holes Used to Shield the Interface States

The most widely used form of applying holes to the benefit of image quality is the pixels that use holes to fill up the interface states. It is well known in the industry that the presence of interface states results in a drastically increased dark current and dark fixed-pattern noise. In many image sensor applications, the dark fixed-pattern noise is the limiting factor in sensor and camera performance. For instance, the longest exposure time in digital still applications is determined by the amount of dark fixed-pattern noise. Reducing the effects generated by dark fixed-pattern noise is of crucial importance. This can be realized by filling the interface states by means of holes [9]. Interface states that are filled with charge carriers no longer generate any dark current [11]. The filling by the holes can be done temporarily or permanently. Both options will be described in the following sections.

A. Temporary Fill of the Interface States

Pulsing the gate of a MOS structure into accumulation can relatively easily fill the interface states by means of holes. For instance, pulsing the CCD gates of a pixel one after another into accumulation and back into deep depletion can attract enough holes to fill up all interface states while the interface is biased in the accumulation mode. In this way, the surface generation part of the dark current will be completely eliminated [12]. This effect is known as the reduction of dark current by means of charge pumping, and it is illustrated in Fig. 7: A similar structure as already shown in Fig. 1 is used. The third gate is biased to a voltage, which is low enough to push the structure into accumulation mode. The interface will attract holes, and they will fill up the interface states and remain trapped even if the structure is forced into deep depletion again. This process is repeated gate after gate.

It looks as though it is a very attractive and simple way of operating the device; but to apply it successfully, the following boundary conditions need to be fulfilled [13], [14].

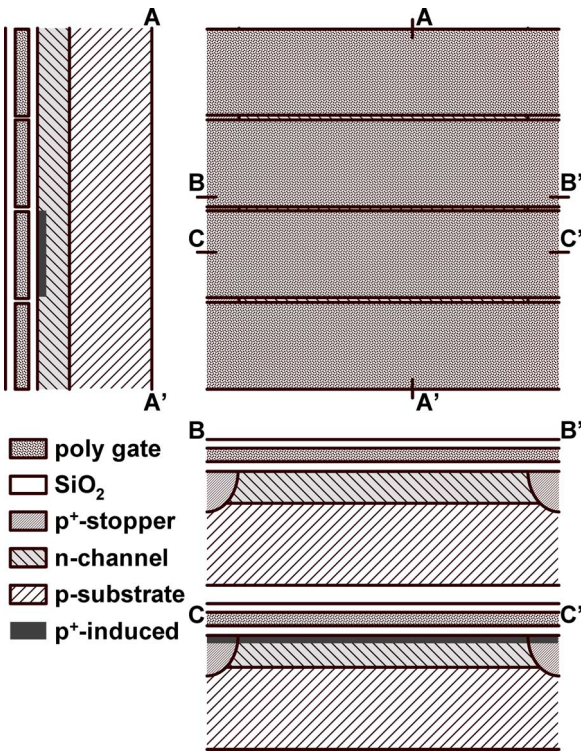

Fig. 7. Top view and cross sections of a four-phase CCD with polysilicon gates fabricated on a p-type Si substrate. One of the gates is pulsed to a low voltage to introduce a hole-accumulation layer at the interface.

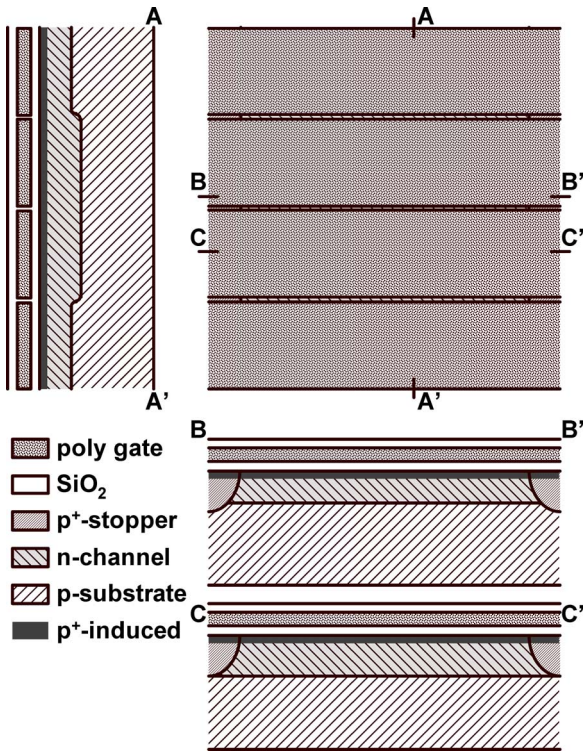

Fig. 8. Same structures as shown in Fig. 7, but in this case with a permanent hole-accumulation layer at the interface. An extra n-type implant is introduced to create a deep potential in the CCD channel.

1) There needs to be a source of holes available in the structure to supply the holes that are used to fill up the interface states. In large area sensors built on depleted p-wells, this can be an issue. The problem can be solved by the introduction of low-resistivity channel stopper regions.
2) After filling the interface states with holes, the gates of the MOS structures are rebiased into deep depletion, and the excess holes underneath the gates need to be able to escape quickly.
3) The filling action needs to be repeated frequently! Once the interface states are filled with holes and once the MOS structures are pulsed into deep depletion again, the interface states tend to release the holes, become empty, and start generating dark current again. This relaxation process depends very much on temperature as well.

Obeying these design and operating conditions, a spectacular reduction in dark current and in dark current nonuniformities can be obtained!

An interesting side effect of having all interface states filled with holes can be found in clocked antiblooming. After pulsing the gates negatively, the interface states are filled with holes. In the case of strong illumination, the charge packet in the sensor will fill up with electrons, and if the device is correctly designed, one can allow the collected electrons in the charge packets that are almost completely filled to reach the $Si-SiO_2$ interface. These electrons will interact and recombine with the holes in the interface states, and the recombined electrons will no longer contribute to any video signal. It looks like the holes have skimmed part of the electrons from the charge packet. In this way, the overflow or blooming of excessively generated electrons can be prevented. This technique is also known as clocked antiblooming or antiblooming by charge pumping [3].

The technique of clocked antiblooming has the following disadvantages: First, one needs to have "enough" interface states to act as an effective antiblooming drain. However, on the other hand, interface states that are emptied through an electron–hole recombination can start generating dark current again.

A major limitation of the charge pumping to reduce dark current effects is its dependence on time and temperature. As already mentioned, the interface states release their holes and start generating dark current again after a short period of time. An answer to this issue can be found in the MPP [15] and all-gates pinning (AGP) [16] CCD structures. By means of a clever design, layout, and processing, a structure can be made that can be forced into accumulation mode for its full integration period, without any refreshing cycle needed. As long as the CCD is operated in the integration or exposure mode, all clocks remain biased to a low voltage, and all interface states are filled with holes. Charges are collected in the potential pockets created by an extra n^--implant within each pixel (see Fig. 8): During the integration period, all CCD gates are biased low, and holes are attracted to the $Si-SiO_2$ interface and eliminate the generation of dark current due to the unfilled interface states. An extra potential pocket is created in the structure to store the collected charges and to form a barrier between the various charge packets in the structure. Only during the transport of the charge packets that the CCD gates are biased to higher voltages. Because the transport of the CCDs is done much faster than the

relaxation time of the interface states, dark current can be kept low during the complete operation of the sensors.

Furthermore, in these CCDs, the following boundary conditions need to be fulfilled.

1) There needs to be a low-resistivity path to allow enough hole flow underneath the gates biased into accumulation.
2) There needs to be a low-resistivity path to allow the holes to be drained away from the interface when the gates are biased again into deep depletion.

The AGP variant has a few extra features over the MPP version (e.g., charge reset and vertical antiblooming), but the basic concept of shielding the dark current generation by the interface states is the same. For the device with the MPP option: In the non-MPP mode, it shows a dark current of 0.5 $\mathrm{nA/cm^2}$ at room temperature; in the MPP mode, this value is reduced to 0.01 $\mathrm{nA/cm^2}$ [15] and even lower. Similar to the MPP sensor is the AGP version, a reduction in dark current by a factor of 25 is observed when the AGP mode is switched on: 0.3 $\mathrm{pA/cm^2}$ at room temperature and 3 $\mathrm{pA/cm^2}$ at 60 °C. Furthermore, the nonuniformity of dark fixed-pattern noise is reduced by a factor of 3–10, resulting in 4.5 $\mathrm{pA/cm^2}$ at room temperature and 16 $\mathrm{pA/cm^2}$ at 60 °C [16].

B. Permanent Fill of the Interface States

A permanent fill of the interface states would solve once and for all the issue of the dark current generation through these interface states! Such a permanent fill can be realized by means of a shallow p^+-implantation at the $Si-SiO_2$ interface. Unfortunately, such a shallow implant does not allow any longer control of the potential underneath the structure. The accumulation layer composed of holes will electrically shield the influence of the gate voltage above it as well. This is exactly the same situation present in the OPP-CCD and the VP-CCD, where the gates are even omitted above the p^+-implanted regions. The latter effect is no issue. Photodiodes do not have a gate above the structure to control the potentials. This is the "secret" behind the so-called PPD, buried photodiode, or HAD: the classical n-p photodiode is provided with an extra shallow p^+-layer (i.e., $1 \cdot 10^{13}/\mathrm{cm^2}$, B, 30 keV on top of $5 \cdot 10^{12}/\mathrm{cm^2}$, P, 200 keV) at the $Si-SiO_2$ interface to fill the interface states with holes and to pin the voltage at the interface to a fixed potential. In this way, a relatively simple structure is produced with an exceptionally good dark performance.

The construction of an interline-transfer CCD with a PPD is shown in Fig. 9. From the top view, the CCD register with four gates can be recognized, next to two photodiodes. Cross section $A-A'$ is very similar to earlier cross sections shown, because of the classical 4-phase CCD structure. Cross section $B-B'$ highlights the PPD: the complete structure is built in a p-well on an n-type substrate. The photodiode is made from an n-implantation in the p-well. The p^+-pinning layer is shielding the photodiode from the $Si-SiO_2$ interface, and is electrically connected to the channel stopper regions and to the p-well. In this way the interface is pinned to the potential applied to the p-well/channel stoppers.

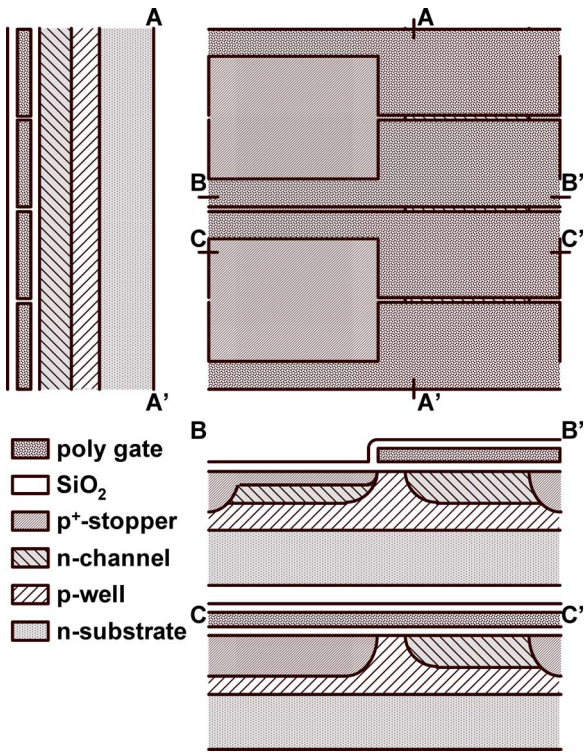

Fig. 9. Top view and cross sections of a four-phase interline-transfer CCD with PPDs and fabricated on an n-type Si substrate.

The very first publications on PPDs describe the presence of the p^+-layer to pin the interface to a fixed voltage, and to allow a complete read-out or reset of the photodiode without any image lag [2]. Later the positive effects on the dark current performance were recognized [17], [18].

PPDs were and still are very efficient in increasing the performance of the interline-transfer CCDs. As a kind of spinoff of the vertical p^+-n-p-n structure, the interline-transfer CCDs can apply a charge reset (electronic shuttering) by applying a positive pulse on the substrate of the imager [19]. The top part of the PPD is pinned to the surface potential by means of the p^+-layer, and the bottom part of the PPD is tied to a high potential. This way of working resets the photodiode completely.

VI. Hole Role in CMOS Image Sensors

As can be learned, history is repeating itself. The ideas explored in CCD technology are also successfully introduced in the CMOS technology as it comes to the development of image sensors.

A. Three-Transistor APS Pixel (3T-APS)

These days, APSs are almost exclusively used to construct CMOS pixels. APSs are characterized by the presence within each pixel of not only the photodiode but also a minimum of three transistors in the form of a source-follower amplifier. An example of such a 3T cell is shown in Fig. 10. At the left side, the photodiode can be seen (see also cross section $A-A'$), and at the right side and top to bottom, the selection transistor,

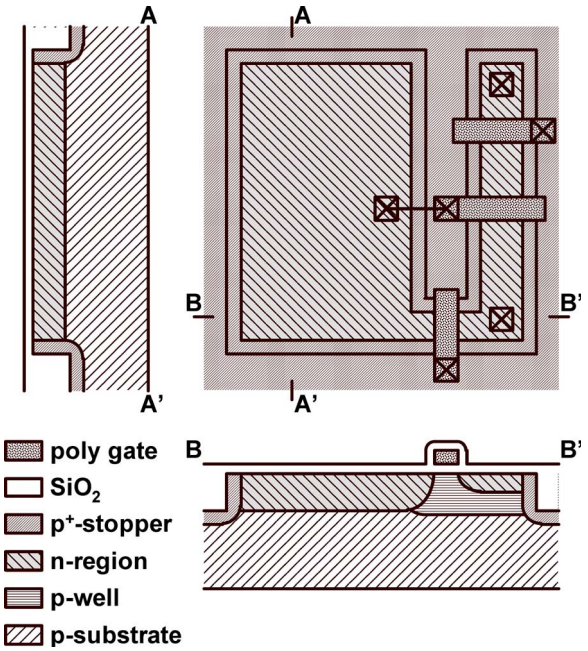

Fig. 10. Top view and cross sections of a 3T CMOS pixel fabricated on a p-type Si substrate.

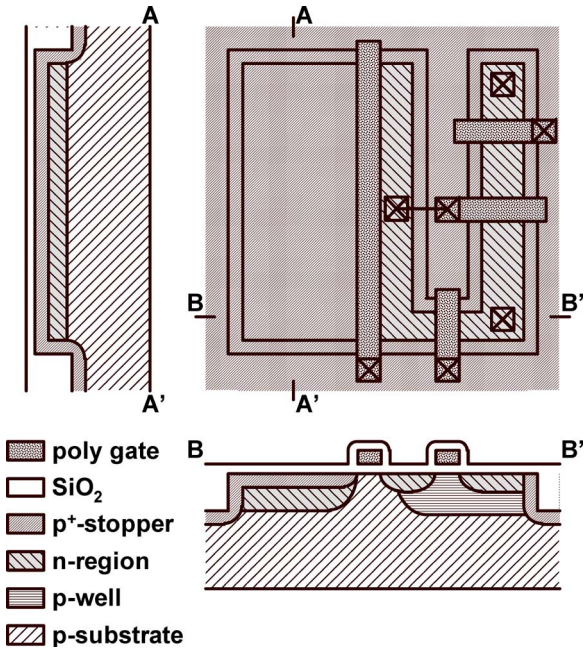

Fig. 11. Top view and cross sections of a 4T CMOS pixel based on a PPD and fabricated on a p-type Si substrate.

the source follower, and the reset transistor can be recognized. Cross section B−B′ highlights the photodiode and the reset transistor.

Notice again the following effects in which the holes play an important role.

1) Electron–hole pairs are being generated in the photodiode, and in this case, both electrons as well as holes are stored in the photodiode.
2) In the case of overexposure, the excess electrons will be drained by the reset transistor, but the excess holes need to be drained by the p^+-stopper regions as well as by the p-type backing substrate.
3) Of great importance in this structure is the encapsulation of the shallow-trench isolation (STI) by means of the p^+-implant. The STI construction introduces mechanical stress as well as high electrical fields into the pixels, resulting in high dark current and dark FPN values. However, in the case that the STI interfaces are put into accumulation, all defects are shielded from the photodiodes and will not influence the dark performance of the imager.

B. Four-Transistor APS Pixel (4T-APS)

Based on the success of PPDs or buried photodiodes in CCD technology, they were also introduced in CMOS image sensors that rely on four-transistor-cell active pixels [20].

The 4T pixel is illustrated in Fig. 11. In comparison with Fig. 10, the 4T has an extra transfer gate inserted between the photodiode and the three transistors already present in the 3T pixel. At the left side of this transfer gate, the photodiode with a pinning layer on top can be recognized. At the right side of the transfer gate, a (floating) diffusion is defined to perform the charge-to-voltage conversion.

As could be expected, the permanent fill of the interface in CMOS imagers resulted again in a drastic reduction in dark current and dark current fixed-pattern noise. The dark current was reduced from 6 to 0.15 nA/cm^2 by means of the PPD (numbers quoted are measured at room temperature) [21].

The application of PPD in CMOS sensors creates the following interesting spinoff benefits.

1) The PPD in a 4T cell allows correlated double sampling (CDS), and in this way, the effect of pixel reset or kTC noise is substantially reduced [22].
2) It allows the construction of shared pixels, in which the readout part of a pixel is shared between two, four, or even eight pixels. In this way, the fill factor of the pixels can be increased dramatically or the pixels can be made considerably smaller while preserving fill factor [23].

C. Switched Biasing

The charge pump mechanism to reduce the surface generation effects described earlier in this paper was only applied to CCD pixels. However, recently, a similar technique is introduced in CMOS sensors as well. One of the biggest concerns in CMOS imagers is the presence of 1/f noise of the in-pixel source-follower transistor. Although the exact mechanism of 1/f noise generation is not known, it is believed that 1/f noise is related to the presence of interface states. The charge carriers present in the channel of the MOS transistor have the possibility of being trapped and reemitted by these interface states. This action modulates the number of carriers present in the conduction channel, resulting in the 1/f noise behavior of the device. By biasing the gate of the source follower (together with the floating diffusion) into accumulation at the time when the source follower is not active, the interface states will be filled with holes. Once the pixel becomes active during the readout

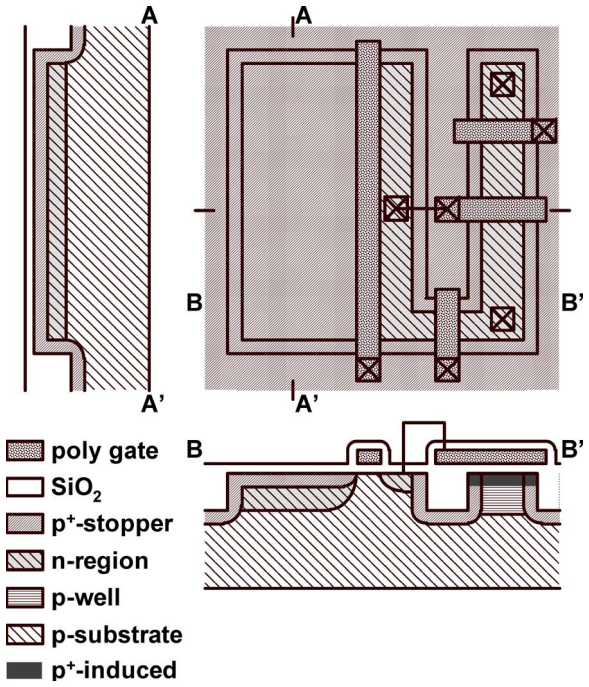

Fig. 12. Top view and cross sections of a 4T CMOS pixel, the $Si-SiO_2$ interface of the source-follower transistor is filled with holes to lower the 1/f noise contribution of this transistor.

cycle, the video signal is transferred onto the floating diffusion. Then, the source follower becomes active, and the structure is released from its accumulation state. The interface states remain filled with holes and are inactive (for a short period of time); consequently, the 1/f noise is reduced. This technique is also known as switched biasing [24] and is schematically illustrated in Fig. 12. The same pixel as shown in Fig. 10 is used, but in this case, the cross section $B-B'$ indicates the situation in the source-follower transistor. An appropriate biasing of the source-follower gate to a low voltage will attract holes under the gate to invert the channel of the MOS transistor. A similar effect can be obtained by switching the source and the drain of the MOS transistor to a high potential. Once an accumulation layer of holes is present under the gate, the surface states will fill up with holes, and they will become inactive.

VII. Conclusion

Holes play a very important role in the performance of image sensors. The presence of holes in today's imaging products cannot be overestimated! The first concern is to get rid of the excess of holes, but once this has been taken care of, the next step can be to use the holes to the benefit of the image quality! The acceptance and introduction of solid-state imaging applications was boosted once the positive effect of an accumulation layer composed of holes was discovered. Such an accumulation layer can reduce the generation of interface-related dark current and dark current fixed-pattern noise. This superb imaging characteristic holds for consumer as well as for professional products for CCDs as well as for CMOS. If these days the CMOS image sensors are challenging the CCDs when it comes to image quality, it is fully based on the ability to copy features and tricks into the CMOS technology that were originally developed in CCD technology and that rely on the exploration of the hole role. This is not really surprising, because after all, it is all silicon!

Acknowledgment

The author would like to thank all his colleagues of the last 30 years at the Catholic University of Leuven, Philips Research, Philips Semiconductors, DALSA and Delft University of Technology, as well as his competitors in the imaging field, who contributed in one way or another to the exciting R&D in the area of CCD and CMOS image sensors. The author would also like to thank D. Litwiller for editing the manuscript of this paper.

References

[1] A. Theuwissen, J. Bosiers, and E. Roks, "The hole role," in *IEDM Tech. Dig.*, 2005, pp. 817–820.
[2] N. Teranishi, A. Kohono, Y. Ishihara, E. Oda, and K. Arai, "No image lag photodiode structure in the interline CCD image sensor," in *IEDM Tech. Dig.*, 1982, pp. 324–327.
[3] G. Beck, M. Collet, J. van Gils, A. Klinkhamer, H. Peek, W. Ruis, J. van Santen, T. Smit, and G. Vandormael, "High density frame transfer image sensor," in *Proc. 14th Conf. Solid-State Devices*, Tokyo, Japan, 1982, pp. 109–112.
[4] J. Janesick, "Open pinned-phase CCD technology," *Proc. SPIE*, vol. 1159, 1989. San Diego.
[5] ——, "Multi-pinned phase charge-coupled device," *NASA Tech. Briefs*, vol. 14, no. 8, p. 22, 1990.
[6] J. Hynecek, "Virtual phase CCD technology," in *IEDM Tech. Dig.*, 1979, pp. 611–614.
[7] A. Theuwissen, *Solid-State Imaging With Charge-Coupled Devices*. Norwell, MA: Kluwer, 1995.
[8] Y. Hagiwara, M. Abe, and C. Okada, "A 380H $\times$ 488V CCD imager with narrow channel transfer gates," in *Proc. 10th Conf. Solid-State Devices*, Tokyo, Japan, 1978, pp. 335–340.
[9] J. Hynecek, "Virtual phase technology: A new approach to fabrication of large-area CCDs," *IEEE Trans. Electron Devices*, vol. ED-28, no. 5, pp. 483–489, May 1981.
[10] M. van de Steeg, H. Peek, J. Bakker, J. Pals, B. Dillen, and J. Oppers, "A frame-transfer CCD color imager with vertical antiblooming," *IEEE Trans. Electron Devices*, vol. ED-32, no. 8, pp. 1430–1438, Aug. 1985.
[11] A. S. Grove, *Physics and Technology of Semiconductors*. Hoboken, NJ: Wiley, 1967.
[12] N. S. Saks, "A technique for suppressing dark current generated by interface states in buried channel CCD imagers," *IEEE Electron Device Lett.*, vol. EDL-1, no. 7, pp. 131–133, Jul. 1980.
[13] G. Putman, S. Kelly, S. Wang, W. Davis, E. Nelson, and D. Carpenter, "Photography with an 11-megapixel 35-mm format CCD," *Proc. SPIE*, vol. 5017, pp. 371–384, 2003.
[14] I. Peters, A. Kleimann, F. Polderdijk, W. Klaassens, R. Frost, and J. Bosiers, "Dark current reduction in very-large area CCD imagers for professional DSC applications," in *IEDM Tech. Dig.*, 2004, pp. 993–996.
[15] T. H. Lee, B. Burkey, and R. Khosla, "A 4 million pixel CCD image sensor," in *Proc. ESSDERC*, Nottingham, U.K., 1990, pp. 599–602.
[16] I. Peters, A. Kleimann, W. Klaassens, F. Polderdijk, and J. Bosiers, "Dark current reduction in FT-CCDs," in *Proc. IEEE Workshop CCDs & AIS*, Karuizawa, Japan, 2005, pp. 141–144.
[17] Y. Matsunaga and N. Suzuki, "An interline transfer CCD imager," in *Proc. ISSCC Tech. Dig.*, 1984, pp. 32–33.
[18] B. Burkey, W. Chang, J. Littlehale, T. Lee, T. Tredwell, J. Lavine, and E. Trabka, "The pinned photodiode for an interline-transfer CCD image sensor," in *IEDM Tech. Dig.*, 1984, pp. 28–31.
[19] T. Kuriyama, H. Kodama, T. Kozono, Y. Kitahama, Y. Morita, and Y. Hiroshima, "A 1/3-in 270 000 pixel CCD image sensor," *IEEE Trans. Electron Devices*, vol. 38, no. 5, pp. 949–953, May 1991.
[20] R. Guidash, T. Lee, P. Lee, and D. Sackett, "A 0.6 μm CMOS pinned photodiode color imager technology," in *IEDM Tech. Dig.*, 1997, pp. 927–929.

[21] K. Yonomoto and H. Sumi, "A CMOS image sensor with a simple fixed-pattern-noise-reduction technology and a hole accumulation diode," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 2038–2042, Dec. 2000.
[22] M. White, D. Lampe, F. Blaha, and I. Mack, "Characterization of surface channel CCD image arrays at low light levels," *IEEE J. Solid-State Circuits*, vol. SC-9, no. 1, pp. 1–13, Feb. 1974.
[23] H. Takahashi, M. Kinoshita, K. Morita, T. Shirai, T. Sato, T. Kimura, H. Yuzurihara, and S. Inoue, "A 3.9 μm pixel pitch VGA format 10b digital image sensor with 1.5-transistor/pixel," in *Proc. ISSCC Dig. Tech. Papers*, 2004, pp. 108–109.
[24] M. Snoeij, A. van der Wel, A. Theuwissen, and J. Huijsing, "The effect of switched biasing on 1/f noise in CMOS imager front-ends," in *Proc. IEEE Workshop CCDs & AIS*, Karuizawa, Japan, 2005, pp. 68–71.

Albert J. P. Theuwissen (S'83–M'83–SM'95–F'02) was born in Maaseik, Belgium, on December 20, 1954. He received the M.Sc. degree in electrical engineering and the Ph.D. degree in electrical engineering from the Catholic University of Leuven, Leuven, Belgium, in 1977 and 1983, respectively. His thesis work was based on the development of supporting hardware around a linear CCD image sensor. His dissertation was on the implementation of transparent conductive layers as gate material in the CCD technology.

From 1977 to 1983, his work at the Department Electrical Engineering (ESAT) Laboratory, Catholic University of Leuven, focused on semiconductor technology for linear CCD image sensors. In 1983, he joined the Micro-Circuits Division, Philips Research Laboratories, Eindhoven, The Netherlands, as Member of the Scientific Staff. Since that time, he was involved in research in the field of solid-state image sensing, which resulted in the project leadership of SDTV and HDTV imagers. In 1991, he became the Department Head of the Imaging Devices Division, focused on CCD as well as CMOS solid-state imaging activities. He is the author or coauthor of many technical papers in the solid-state imaging field and is the holder of several patents. In 1995, he authored the textbook titled *Solid-State Imaging With Charge-Coupled Devices*. In 1998, he became an IEEE Distinguished Lecturer. In March 2001, he became a part-time Professor at the Delft University of Technology, Delft, The Netherlands. At this university, he teaches courses in solid-state imaging and coaches Ph.D. students in their research on CMOS image sensors. In April 2002, he joined DALSA Corporation to act as the company's Chief Technology Officer (CTO). In September 2004, he retired as CTO and became the Chief Scientist of DALSA Semiconductors. This shift allows him to focus more on the field of training and teaching solid-state image sensor technology. In 2005, he founded the European Technical Expert Team on Image Sensors (ETETIS), a nonprofit organization to promote European R&D activities in the field of solid-state image sensors. He is a Member of the editorial board of the magazine *Photonics Spectra*.

Dr. Theuwissen is a member of the International Society for Optical Engineering (SPIE). In 1988, 1989, 1995, and 1996, he was a Member of the International Electron Devices Meeting Paper Selection Committee. He was Co-Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES special issues on *Solid-State Image Sensors* in May 1991, October 1997, and January 2003 and the *IEEE Micro* special issue on digital imaging in November/December 1998. He acted as the General Chairman of the IEEE International Workshop on Charge-Coupled Devices and Advanced Image Sensors in 1997 and 2003. He is a Member of the Steering Committee of the aforementioned workshop and the founder of the Walter Kosonocky Award, which highlights the best paper in the field of solid-state image sensors. For several years, he was a Member of the Technical Committee of the European Solid-State Device Research Conference and the European Solid-State Circuits Conference. Since 1999, he has been a Member of the Technical Committee of the International Solid-State Circuits Conference (ISSCC). For the same conference, he acted as Secretary, Vice-Chair, and Chair in the European ISSCC Committee. He is also a member of the overall ISSCC Executive Committee.