The Hole Role

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Abstract

The importance of holes in solid-state image sensors is described. Today's success of digital imaging is based on the positive effect of an accumulation layer that reduces the interface-related dark current and dark current fixed-pattern noise. This superb imaging feature is applied in CCD as well as in CMOS devices, in consumer as well as in professional equipment. Holes are not only used to improve the dark performance of imagers, other examples are fixing electrostatic potentials, creating gate structures, draining photon-generated charges and constructing output-amplifier stages.

Introduction

Holes play an important role in the quality of images obtained by solid-state image sensors. In the first place, holes can be used to fix the electrostatic potential in pixel. Secondly, holes can be seen as a by-product in the generation of the video signal : absorbed photons in the silicon result in electron-holes pairs. In the past there were some trials to use both electrons and holes for "mapping" the image. But this appeared not to be successful. The only solution left is then to discard the holes in an efficient and proper way, without hampering the electron-picture.
Once excess holes are drained, a next step can be taken and that is to make use of holes to improve the quality of the imager. The pinned-photo diode is probably the best example of the latter statement and is a popular element used in CCD and CMOS image sensors. But, holes play a much broader role in improving the imaging function than just reducing the dark current. They are key in the functionality of clocked anti-blooming, in noise reduction as well as in the definition of clock phases, and can benefit output amplifiers as well. This paper will give an overview of the role that holes play in today's imaging system.

Holes used to fix the potentials in the pixels

A crucial part of a properly functioning pixel of an image sensor is a well-defined electrostatic potential at any point or region within and between pixels ! If there exists an area within a pixel without an appropriately defined voltage applied to it, the pixel can partly lose functionality. The simplest example is the separation of pixels by means of p^+ stopper implants in CCD or p^+ isolation regions between CMOS pixels.

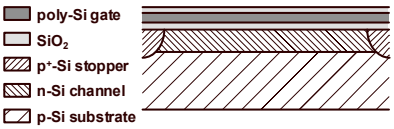

Figure 1. Cross section of a buried-channel CCD on p-Si substrate (the cross section is made perpendicular to the CCD channel) .

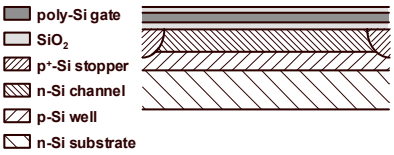

Figure 2. Cross section of a buried-channel CCD on n-Si substrate (the cross section is made perpendicular to the CCD channel).

A CCD channel stopper example is illustrated in Figure 1 : a cross section is shown of an n-type buried channel CCD sandwiched between two p^+ channel stopper regions. The CCD is built on a p-type substrate [1]. The p-substrate acts as a "low resistivity" backplane for all the individual channel stop regions. This situation changes when the imager is built on a depleted p-well in a non-depleted n-substrate as shown in Figure 2.

This architecture is popular for devices that use vertical anti-blooming. The vertical n(CCD channel)-p(well)-n(substrate) acts as a bipolar transistor in punchthrough at the moment the CCD channel is filled with electrons [1]. The concentration of holes in the channel stoppers becomes important, because the channel stopper regions are no longer backed-up by the large p-well ! Without doping changes, the resistivity of the p^+ network becomes larger and more susceptible to cross-talk.

A relatively old technique to create a two-phase clocking system [2] and/or increase the blue sensitivity of the imager [3], is to cut so-called light windows in the gates. But in the case that parts of the depleted n-type CCD channels are not covered by gate material, their surface potential is undefined ! Such a structure will suffer from charge transport issues during operation, because charge can be trapped in local potential pockets. The effect can be solved by defining the potential in the open areas through an extension of the p^+ channel stopper. A simple self-aligned implant of $2x10^{13}$ /cm^2 boron ions is sufficient to extend the channel stop areas to the gate edge and consequently fix the potential in the open areas [2]. The result

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after this self-aligned implant is shown in Figure 3. The presence of enough holes plays a crucial role in fixing the potential for the regions "beyond control" of the gates. (Is this structure the mother of the pinned-photodiode or buried diode or hole-accumulation device ?)

Holes used to create gates

In classical CCD structures the transport of electrons is guided by means of digital pulses supplied to the CCD gates. In principle not all the gates of a pixel need to be clocked, some gates might also be fixed at a certain potential and in this way they create a potential barrier in the silicon. A typical example is the output gate located between the last clocking gate of a CCD and the floating diffusion. A similar structure exists in CMOS pixels, especially in the APS photogate structure. A p^+ layer at the Si-SiO_2 interface above the n-buried CCD channel can substitute a non-clocking or DC-biased gate, resulting in a local potential barrier. Structures making use of this construction in every pixel are known as Virtual Phase (VP) and Open Pinned-Phase (OPP) CCD. In the latter, two gates of the classical CCD structure are replaced by means of a shallow implant [4]. A cross section of an OPP-CCD is shown in Figure 4. The interface potential in the open area is pinned to the potential of the p-substrate. The channel potential underneath the open gates is determined by the doping levels in the fully depleted n-channel and the non-depleted p-substrate.

A further extension of the idea to create equivalent gate structures by means of a pinning layer can be found in the Virtual Phase CCD [5]. A cross-section is shown in Figure 5 : each pixel consists of one clocked CCD gate and one fixed virtual gate (made by means of the p^+ top implant). To provide the CCD with a well-defined transport direction, extra n^- regions are defined underneath the clocked CCD gate as well as underneath the virtual phase. Despite some drawbacks, the virtual phase CCD has interesting advantages : the device is characterized by increased light sensitivity (especially in blue), low surface dark-current component and a relatively simple clocking sequence.

Holes used to drain photon-generated charges

Photons absorbed in the silicon create electron-hole pairs. Most designers focus on the signal electrons during the imager design, but the generated holes need to get handled by the device as well. If this is not done properly, the holes can drastically hamper the imager's proper functioning. To make sure that this is not the case, the photon-generated holes need to find a low-resistivity path towards a ground connection or another low voltage.
For devices that are built on non-depleted p-type substrates (see Figure 1), the holes can flow vertically (third dimension) to the p-type substrate and can be easily drained by the p-type substrate. But in the case that the p-well is part of a vertical anti-blooming structure, it will be fully depleted and a success-

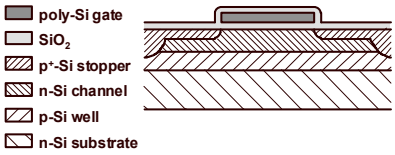

Figure 3. Cross section of a buried-channel CCD on n-Si substrate including light windows and pinned interface potential in the non-covered CCD channels (the cross section is made perpendicular to the CCD channel).

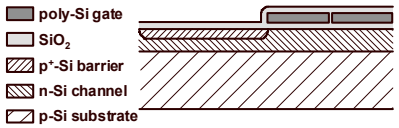

Figure 4. Cross section of an Open Pinned-Phase CCD in which holes are used to create a fixed barrier gate (the cross section is made along the CCD channel).

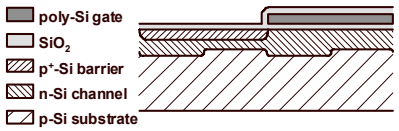

Figure 5. Cross section of a Virtual Phase CCD in which holes are used to create a fixed barrier gate (the cross section is made along the CCD channel).

full drainage of the holes by means of only the p-well is no longer possible [6] ! This effect is shown in Figure 3. A similar situation is present in devices built on SOI in which the complete (thin) backing silicon layer is depleted. To maintain a proper functionality of the imager in the case that the p-well is fully depleted, the device needs to be provided with p^+ channel stopper regions that have a sufficiently high doping level to drain photon-generated holes. Be aware that :

- the amount of holes to be drained can be large (e.g. 100,000 times over-exposure in a 9 µm x 9 µm pixel that has a saturation level of 100,000 e^-, results in total drainage of 10^{10} holes per pixel),
- the channel stoppers can be long (e.g. worst case 12 mm in a device of 36 x 24 mm, 1 µm in width, or a total of 12,000 squares).

So, a serious voltage drop can be generated by hole drainage through the channel stopper lines. These voltage drops can result in local non-uniformities and artifacts in the center of a highlight ("black smear") if the doping level of the channel stoppers is too low. If the proper operation of the sensor asks for voltage drops less than 1 V, the overall doping level of the channel stoppers needs to be high enough to allow the excess hole current to flow, e.g. $5x10^{13}$ /cm^2 [6].

Holes used to shield the interface states

The most widely used form of applying holes to improve image quality, is the pixels that use holes to fill up the interface-states. It is well known that the presence of interface-states results in a sharp increase in dark current and in dark fixed-pattern noise.

In many image sensor applications the dark fixed-pattern noise is the limiting factor in sensor and camera performance. For instance, the longest exposure time in digital still applications is governed by the amount of dark fixed-pattern noise. Reducing the effects generated by dark fixed-pattern noise is crucially important. This can be realized by filling the interface states by means of holes [5][7]. Interface states that are filled with charge carriers no longer generate dark current. Filling interface states with the holes can be done temporarily or permanently. Both options will be described :

Temporarily filling the interface states

Pulsing the gate of a MOS structure into accumulation can fill the interface states with holes. For instance, pulsing the CCD gates of a pixel one after another into accumulation can attract enough holes to fill up all interface states and to eliminate surface generation of dark current [7].

This effect is known as the reduction of dark current by means of charge pumping, see Figure 6. It looks an attractive and simple way of operating the device, but to apply it successfully, a few boundary conditions need to be fulfilled [8]:

- a source in the structure to supply large amount of holes to fill up the interface states. In large area sensors built on depleted p-wells this can be an issue. This problem can be solved by the introduction of low-resistivity channel stopper regions,
- after filling the interface states with holes, the gates of the MOS structures are re-biased into deep depletion, and the excess holes underneath the gates need to have the possibility to escape through a low-resistivity path,
- the filling action needs to be repeated frequently !

An interesting side effect of having all interface states filled with holes can be found in clocked anti-blooming. After pulsing the gates negatively, the interface states become filled with holes. In the case of strong illumination, the charge packets in the sensor will fill up, and with an optimized design, one can allow the electrons of the charge packets that are almost completely filled to reach the Si-SiO_2 interface. These electrons will interact and recombine with the holes in the interface states, no longer contributing to the video signal, with the appearance of the holes skimming part of the electrons from the charge packet. In this way the overflow of excessively generated electrons can be prevented. This technique is also known as clocked anti-blooming or anti-blooming by charge pumping [3].

The charge pump mechanism to reduce the surface generation effects described here was only applied to CCD pixels, but recently a few publications have introduced a similar technique in CMOS sensors as well [10]. One of the biggest concerns in CMOS imagers is the presence of 1/f noise in the in-pixel source-follower transistor. By biasing the gate of the source follower FET into accumulation when the structure is inactive, the interface states become filled with holes. Once the pixel goes active during the read-out the interface states remain filled with holes for a short period of time and 1/f noise reduces. This technique is known as Switched Biasing.

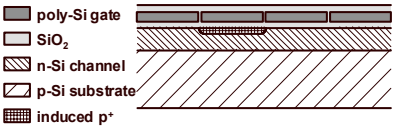

Figure 6. Inducing an accumulation layer underneath one CCD gate in order to reduce the dark current or to create an anti-blooming structure (the cross section is made along the CCD channel).

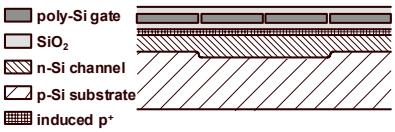

Figure 7. Inducing an accumulation layer underneath all CCD gates in order to reduce the dark current and operate the device in MPP or AGP mode (the cross section is made along the CCD channel).

A major limitation of charge pumping to reduce dark current is its dependence on timing and especially on temperature. An answer to this issue can be found in the multi-phase pinning (MPP) [11] and all-gates pinning (AGP) [12] CCD structures. By means of a clever design, lay-out and processing, a structure can be made that can be forced into accumulation mode without a refresh cycle. Charge is collected in the potential pockets created by an extra n^- implant within each pixel, see Figure 7. Only during transport of the charge packets are the CCD gates biased to higher voltages. Also in these CCDs a few boundary conditions need to be fulfilled :

- a low resistivity path to allow hole flow underneath the gates biased into accumulation,
- a low resistivity path allowing holes to be drained from the interface when the gates are biased again into deep depletion.

The AGP variant has a few extra features over the MPP version (e.g. charge reset and vertical anti-blooming), but the basic concept of shielding the dark current generation by the interface states is the same. For the device with the MPP option : in the non-MPP it shows a dark current of 0.5 nA/cm^2 at room temperature, with the MMP mode, this value is reduced to 0.01 nA/cm^2 [11]. Similar to the MPP sensor is the AGP version, a reduction in dark current by a factor of 25 is observed when the AGP mode is switched on : 0.3 pA/cm^2 at room temperature and 3 pA/cm^2 at 60°C. Also the non-uniformity or dark fixed-pattern noise is reduced by a factor of 3 to 10, resulting in 4.5 pA/cm^2 at room temperature and 16 pA/cm^2 at 60°C [12].

Permanently filling the interface states

A permanent fill of the interface states would solve once and forever the issue of the dark current generation through these interface states ! A permanent fill can be realized by means of a shallow implantation at the Si-SiO_2 interface. This is the

"secret" behind the so-called Pinned-PhotoDiode (PPD), buried photodiode or Hole-Accumulation Device (HAD) : the classical pn-photodiode is provided with an extra, shallow p^+ layer ($1x10^{13}$ /cm^2, B, 30 keV on top of $5x10^{12}$ /cm^2, 200 keV, P) at the Si-SiO_2 interface to fill the interface states with holes and to pin the interface voltage to a fixed potential. In this way a relatively simple structure is implemented with exceptional dark performance.

However, it is questionable whether the pinned-photodiode was invented for this reason. First publications describe the presence of the p^+ layer to pin the interface to a fixed voltage, and to allow a complete read-out or reset of the photodiode without any image lag [13]. Later the effects on dark performance were recognized [14][15].
Pinned photodiodes were and still are very efficient in increasing the performance of interline-transfer CCDs. As a derivative of the vertical p^+np structure (see Figure 8), the interline-transfer CCDs can apply a charge reset (electronic shutter) by applying a positive pulse on the substrate on the imager [16].

Based on the success of the pinned or buried photodiodes, they were also introduced in CMOS imagers that rely on 4 transistor-cell active pixels [17]. As could be expected, the permanent fill of the interface in CMOS imagers resulted again in a large reduction in dark current and dark-current fixed-pattern noise. The dark current was reduced from 6 nA/cm^2 to 0.15 nA/cm^2 by means of the PPD (figures quoted are measured at room temperature) [18]. The application of PPD in CMOS sensors created an extra, interesting spin-off : the PPD in a 4 T cell allows Correlated-Double-Sampling (CDS) and in this way the effect of pixel-reset or kTC noise is reduced.

Holes used in the output amplifier

New low-noise output architectures were launched in which the driver of the source-follower stage is replaced by a JFET. The charge packet generated in each pixel, is transferred to the gate of the JFET, modulating a hole current through the transistor. An alternative can be found in a MOSFET in which the charge packet is stored in the bulk of the device. Also here a hole current is modulated by the video signal [19]. Because the sensing capacitance is limited, the new output configurations have an optimized noise performance.

Conclusion

Holes play an important role in the performance of image sensors. The presence of holes in today's imaging products can not be overestimated ! The first concern is to remove excess holes, but once this has been taken care of, the next step can be to use holes to benefit image quality. Acceptance and introduction of solid-state imaging applications was boosted

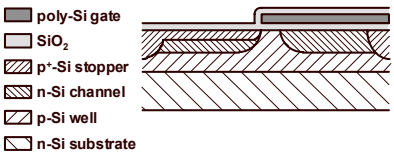

Figure 8. Cross section of an interline-transfer CCD with a pinned-photodiode (left) next to the CCD register (right), cross section is taken perpendicular to the CCD channel.

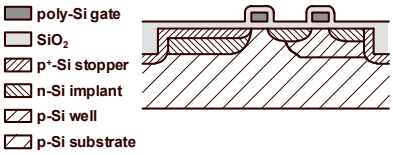

Figure 9. Cross section of a 4T-APS CMOS pixel with a pinned-photodiode (left) next to the transfer gate and the reset transistor (right).

upon discovery of the positive effect of an accumulation layer composed of holes. Such an accumulation layer can reduce the generation of interface-related dark current and dark current fixed-pattern noise. This superb imaging feature holds for consumer as well as for professional products, for CCDs as well as for CMOS. After all, it is all silicon !

Acknowledgement

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References

[1] A. Theuwissen : "Solid-State Imaging with Charge-Coupled Devices", Kluwer Academic, ISBN 0-7923-3456-6, 1995,
[2] Y. Daimon-Hagiwara et.al., Proc. 10th Conf. on Solid-State Devices, Tokyo, 1978, pp.335-340,
[3] G.A. Beck et.al., Proc. 14th Conf. on Solid-State Devices, Tokyo, 1982, pp. 109-112,
[4] J. Janesick, SPIE Proceedings, Vol. 1159, San Diego, 1989,
[5] J. Hynecek, IEEE Transac. Electr. Dev., Vol. ED-28, 1981, pp. 483-489,
[6] M.J.H. van de Steeg et.al., IEEE Transac. Electr. Dev., Vol. ED-32, 1985, pp. 1430-1438,
[7] N.S. Saks, IEEE Electr. Dev. Letters, Vol. EDL-1, 1980, pp. 131-133,
[8] G. Putman et.al., SPIE Proceedings, Vol. 5017, 2003, pp. 371-384,
[9] I. Peters et.al., IEDM Technical Digest, 2004, pp. 993-996,
[10] M.F. Snoeij et.al., IEEE Workshop on CCDs & AIS, Karuizawa, 2005,
[11] T.H. Lee et.al., Proceedings ESSDERC, Nottingham, 1990, pp.599-602,
[12] I. Peters et.al., IEEE Workshop on CCDs & AIS, Karuizawa, 2005,
[13] N. Teranishi et.al., IEDM Technical Digest, 1982, pp. 324-327,
[14] Y. Matsunaga et.al., ISSCC Technical Digest, 1984, pp. 32-33,
[15] B.C. Burkey et.al., IEDM Technical Digest, 1984, pp. 28-31,
[16] T. Kuriyama et.al. , IEEE Transac. Electr. Dev., Vol. 38, 1991, pp. 949-953,
[17] M. Guidash et.al., IEDM Technical Digest, 1996, pp. 927-929,
[18] K. Yonomoto et.al., IEEE Transac. Electr. Dev., Vol. 35, 2000, pp. 2038-2042,
[19] E. Roks : "Advanced CCD Imaging by Opposite Carrier Interaction", PhD Dissertation, Twente University, 1994, ISBN 90-74445-13-6.