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CONSUMER CCDS: MASTERPIECES OF 3-D INTEGRATION

Snapshot: The development of CCDs for consumer applications is driven by cost reduction considerations. In this very competitive, high-volume market (over 10 million CCDs per year) the drive is toward an ever lower cost for a CCD camera while maintaining (or even improving) performance and adding extra features.

Over the past decade, the optical format of the CCD imagers used in such consumer CCDs as camcorders, observation cameras, and home security systems, has decreased. Since the mid-1980s, 1/2-in. sensors (imaging area 6.4 (H) × 4.8 (V) mm^2) have been commercially available. In the late 1980s and early 1990s, 1/3-in. imagers (4.8 × 3.6 mm^2) took over the main market share, and today 1/4-in. CCDs (3.6 × 2.7 mm^2) dominate the camcorder business. The decrease in optical format has all to do with imager cost. Within the CCD business, the price of the imagers is mainly determined by the cost of processing semiconductor wafers. The smaller the chip size of the imager, the more devices can be put on a single wafer, and the lower the price of each individual device. This trend of going to smaller devices will probably continue as long as the optical and electrical performance of the imagers do not change when switching to the next generation of CCD imagers.

CCD architecture

Four basic types of CCD architectures for area imagers can be distinguished (see Table 1).

A full-frame imager (FF-CCD)[1] consists of a matrix of image pixels and one or two serial readout registers (Fig. 1). After integration, the image pixels are read out line per line into the serial register, and measured at the output node. During readout, the sensor has to be shielded from light to avoid a spurious smear signal (for a definition of this and other terms see p. 34), *e.g.*, by means of a mechanical shutter; or the integration time has to be significantly larger than the readout time (*e.g.*, in astronomical observations). Real-time video is not possible.

Type	FF	FT	FIT	IL
Application areas	scientific astronomy	broadcast scientific consumer observation	broadcast	consumer observation
Pixel size	≥ 12 × 12 μm^2	5 × 5..10 × 10 μm^2	7 × 7..10 × 10 μm^2	5 × 5..7 × 7 μm^2
Readout Frequency	5 images/sec	PAL, NTSC, HDTV	PAL, NTSC, HDTV	PAL, NTSC

Table 1. Basic types of CCD imagers.

A frame-transfer imager (FT-CCD)[2] consists of two almost identical arrays, one of image pixels and one of storage cells (Fig. 2). After the integration cycle, charge is transferred as fast as possible from the light-sensitive pixels to the storage cells, covered with a metal light shield. This limits the time in which smear is generated to the frame shift time, which is considerably shorter than the readout time. A mechanical shutter is only used in broadcast applications. For the same image format, the FT-CCD is almost twice as large as the FF-CCD, and thus is more expensive.

An interline transfer sensor (IL-CCD)[3] consists of an array of photodiodes and vertical CCD registers (Fig. 3). After the integration cycle, the charge from the photodiodes is transferred to the vertical CCD registers, covered with a metal light shield, and then read out line per line. Only a small fraction of the light can penetrate sideways into these registers, hence the smear is limited. The chip size is about half of that of a FT-CCD, but due to the more complicated technology (photodiode and vertical register cell per pixel), the cost is about the same for equal image formats.

For broadcast applications, the frame-interline transfer imager[4] (FIT-CCD) was developed to achieve even lower smear values as with the IL-CCD, by adding a storage section under the IL-CCD (Fig. 4). Smear is now generated only during the short frame shift time, instead of during the whole readout time. The larger chip size and the more complicated technology make this an expensive CCD, suitable only for high-quality broadcast applications.

Real-time video (PAL, NTSC, VGA) is possible with FT-, IL-, and FIT-CCDs, since a new integration cycle can be started as soon as the previous image has been transferred into the storage matrix (FT-CD) or in the vertical registers (IL- and FIT-CCD).

Only the FT-CCD and the IL-CCD can fulfill the needs for consumer applications. The FF-CCD does not allow real-time video and the FIT-CCD is too expensive.

Essential requirements for consumer CCD camera systems include: inexpensive CCD; low-cost, low-power camera module; real-time video; low smear without shutter; overexposure protection by means of anti-blooming structure (often called vertical overflow drain, or VOD)[5]; electronic shutter function by means of charge dump to the overflow drain; and, since many applications require color imaging, a sufficient sensitivity for wavelengths from 400-700 nm. A complementary mosaic color filter pattern using cyan, green, yellow, and magenta colors is most frequently applied.[6,7] For low-light level imaging ('candlelight camcorders'), CCDs with a high quantum efficiency and low noise (both from image dark current and from the output amplifier) are required.[7,8]

The CCD pixel

Each individual pixel of a CCD imager is a masterpiece of device physics and semiconductor technology. As will be seen, the pixels have a dedicated two-dimensional construction within the focal plane, but have also an appropriate architecture in the third dimension with different functions at different levels.

Basement level

Within the silicon substrate, the various functions of a semiconducting device can be constructed by different implantations. This applies also to a CCD imager: starting from an n-type silicon substrate, the entire CCD is built in a p-type well that is implanted in the silicon substrate. All individual pixels are defined by an extra n-type implant. This n-p-n- structure—about 3 μm deep in the third dimension—plays an important role during overexposure handling.

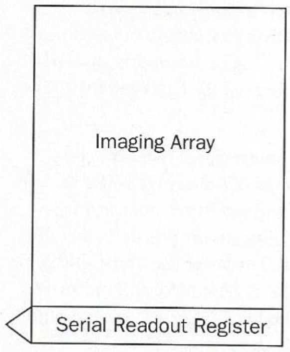

Figure 1. Architecture of full-frame CCD imager.

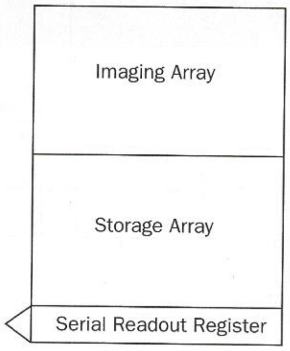

Figure 2. Architecture of frame-transfer CCD imager.

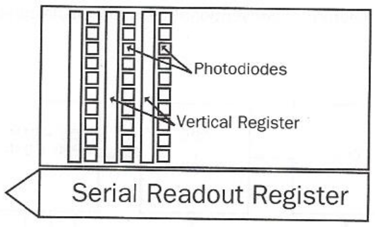

Figure 3. Architecture of interline-transfer CCD imager.

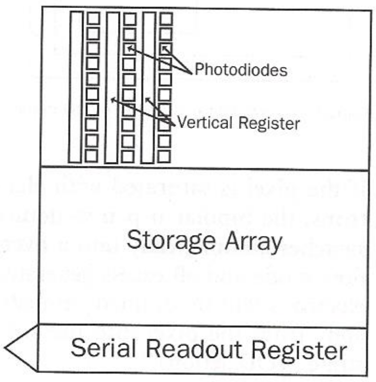

Figure 4. Architecture of frame-interline-transfer CCD imager.

Glossary

Anti-blooming: In a pixel that is exposed to a highlight, more electrons are generated by incident photons than can be stored. An anti-blooming structure will remove the excess electrons to a common drain before they will spill (bloom) to neighboring pixels.

Frame shift: An image is formed in a CCD during a certain integration time. Then, in a FT- or FIT-CCD, the information of the whole image (in the form of electron charge packets) is shifted down into a storage section.

Level shifters/drivers: Convert a digital pulse signal (0V - 5V) with a low current driving capacity to an analog signal (*e.g.*, −1V −9V) pulse with a high current driving capacity, needed to drive the capacitances of the CCD gates with the correct voltage levels.

Smear signal: In FT-CCD, a smear signal is generated during frame shift because the CCD is always sensitive to light; also during the transport of charge packets from the image area to storage section. Light falling on the sensor during this transport causes a smear signal. The faster the frame shift is done, the shorter the time smear is generated, and the lower the smear becomes. In an IL- and FIT-CCD, the vertical registers (Figs. 3 and 4) are shielded from light, but not for 100%. Also here, during frame shift (FIT) or line per line readout (IL) a smear signal is generated.

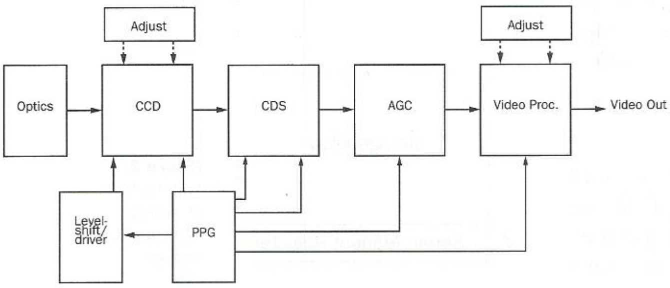

Figure 5. Block diagram of conventional consumer CCD camera module.

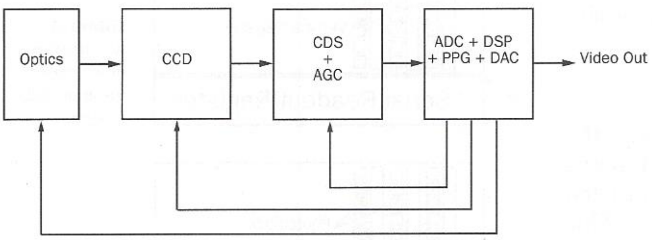

Figure 6. Block diagram of new digital consumer CCD camera module.

If the pixel is saturated with electrons, the bipolar n-p-n structure switches automatically into a overflow mode and all excess generated electrons will be drained immediately from the pixel into the substrate (VOD action).[5]

A second important function of this vertical structure is the emptying of all pixels simultaneously to shorten the integration time of the imager. An electrical pulse on the n-type substrate pulls all n-p-n structures of all pixels into the overflow status and all pixels will be cleared at once (electronic shutter action). At the ceiling of the basement, the various CCD channels and their mutual separation are defined by extra implants. For best performance, often up to nine implants are required for a complete pixel.[9]

First floor

On the first floor of the pixels, transport means are defined from two or three poly-crystalline layers. Within these layers, overlapping gates are defined by etching. By this technique, the classical charge-coupled transfer occur. In the focal plane, the charge transport can take place for all pixels simultaneously or only for pixels belonging to a single video line. The CCD gates are all driven from the outside of the device and the end-user has full control over the transport speed.[10]

Second floor

On the second floor, the various interconnects to the outside world are fabricated. The interconnects have to be low in resistivity and are made from metal layers. Some CCD technologies apply a single layer of metal, others use two metal layers.

Third floor

The third floor acts as a color separation level. Monolithic color filters are deposited on the CCD chip in such a way that different pixels are made sensitive to different parts of the visible spectrum. Today, mainly complementary color filters are applied in a mosaic configuration. This can be translated in a scheme of cyan, green, yellow, and magenta dots into every two-by-two pixel matrix.[6-11]

Fourth floor

Depending on the basic architecture of the device, the pixels have a larger (IL) or smaller (FT) dead zone that is less sensitive (FT) or not sensitive at all (IL). To increase the aperture ratio of the individual pixels, the CCD can be fitted with a microlens array: every pixel gets its own microlens to concentrate the incoming rays, which normally would be impinging on the dead zones, onto the light-sensitive part of the pixels.[12]

The total height of the four floors above the silicon substrate is about 3 μm.

Toward a single-chip CCD camera

The consumer market is driven by a demand for ever lower prices. To reduce the overall cost of a camera module, the cost of all the components has to be reduced, as well as the number of components and the number of required adjustments. Also, power consumption must be reduced.

A typical camera module consists of the following building blocks (Fig. 5):

- optics with lens and optional IR-filter and low-pass optical filter,
- a CCD imager requiring a number of ex-ternal voltage adjustments,
- a pulse pattern generator (PPG) to generate the logic- level H- and V-pulses and all required sync and processing pulses,
- level-shift-ers/drivers toconvert the logic-level output of the PPG to high-driving pulses,
- preprocessing, *e.g.*, correlated-double-sam-pling[13] (CDS) and automatic gain control (AGC) to convert the CCD output signal to a 'usable' signal waveform for processing, and
- processing circuitry, *e.g.*, to make a composite video baseline signal (CVBS) or RGB video signal.

Also, this requires a number of external adjustments, *e.g.,* for correct white balance.

To reduce the cost, a small image-format CCD with a small lens is required. Thus, pixel sizes of $5 \times 5\ \mu m^2$ have recently been developed,[14,15] allowing the reduction of the optical format of a S-VHS- and VGA-compatible CCD to 1/4-in. Also, many vendors now offer their CCDs in plastic packages, which are much cheaper than the conventional ceramic packages used previously. To further reduce the cost of the system, a fixed-iris lens can be chosen such that exposure control is obtained only by means of the electronic shutter function of the CCD. To reduce the number of components, the level-shifters/drivers can be integrated with the CCD.[7]

Also, the number of voltage adjustments should be reduced. Most consumer CCDs need only one adjustment (the voltage setting for the overflow drain). Recently, a CCD was developed in which the required adjustments are performed on-chip, thus allowing a further reduction in the number of components and in the assembly time of the camera module.[16]

To reduce the power consumption, the driving voltages of the horizontal clocks of CCDs that were recently reported were reduced from 5V to 3.3V or even lower.[14] Also, CCD design and technology are improved to reduce the inter-electrode capacitances, e.g., by adjacent (i.e., non-overlapping) electrodes.[17]

To reduce the smear in an FT-CCD, the frame shift frequency has to be increased; frequencies up to 20 Mhz have been reported.[7] In an IL-CCD, the smear is further suppressed by layout and technology improvements that limit the spurious light into the vertical CCDs. In the past, IL-CCDs had an advantage over FT-CCD with repect to smear, but this may change for smaller image formats. A smaller FT-CCD will have lower time constants for the electrodes, allowing faster frame shifts; in a smaller IL-pixel, it will be more difficult to shield the vertical register off from smear.

Another recent development is the all-digital camera. Here, the output of the CCD (after CDS and AGC) is immediately converted to a digital system. This allows the integration of PPG, pre-processing and processing into one single digital signal processing (DSP) chip, as shown in Figure 6. This again allows a drastic reduction in external adjustments, and in overall cost of the system. The CDS and AGC require a different (*i.e.,* analog) IC technology and thus until now are not integrated with the DSP.

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Conclusions

CCD imagers with an optical format of 1/4 inch and pixel sizes of $5 \times 5\ \mu m^2$ have now had performances better than those of 1/2-in., $10 \times 10\ \mu m^2$ pixel CCDs from 10 years ago, thanks to the drive for low-cost consumer imaging. Further reductions in cost will have to come from an integrated systems approach, not merely from less expensive CCDs.

Note

Further technical articles and many references can be found in two special issues of IEEE Transactions on Electron Devices [18,19] devoted to solid-state imagers.

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