1.4 There's More to the Picture Than Meets the Eye*, and in the future it will only become more so

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2021 IEEE International Solid- State Circuits Conference (ISSCC) | 978-1-7281-9549-0/20/$31.00 ©2021 IEEE | DOI: 10.1109/ISSCC42613.2021.9366058

1. Introduction

One of the fastest growing markets in the semiconductor industry is being driven by businesses in the solid-state imaging sector. An overview of the world-wide CIS (CMOS Image Sensor) market is illustrated in Figure 1.4.1. The actual CAGR (compound annual growth rate) from 2010 until 2019 was 15.2% in units and 16.9% in sales, while the forecasted CAGR from 2019 until 2024F is 11.5% in units and 7.2% in sales. Existing DRAM fabrication facilities are being converted into CIS manufacturing plants to cope with the increasing demand for CMOS image sensors [1]. Despite a small 4% drop in revenue, and nearly flat unit growth due to the disruptions caused by COVID-19 in 2020, in 2024F the CIS sector expects a record high of $26.1B and 11B units/year [2]. A simple calculation shows that over the course of 2020 (6.3B units, $18.2B), globally 200 image sensors are being produced every second at an average price of $2.9. Realizing this scale of production by the end of 2020 will require a total of 5.4M wafers (300mm diameter), which is equivalent to a silicon area of 76 soccer fields!

Primarily, this continuous growth is fueled by the mobile phone industry and automotive markets. As both mobile phones and cars now use multiple cameras, it is expected that those numbers will continue to grow in the near future. More cameras are not only needed to take better pictures, but over time more functionality will be required from image sensors, such as depth measurement (or 3D sensing) and the collecting of biomedical data. Other applications, besides mobile phones and automotive, with high projected growth rates in the coming 5 years are: medical/scientific systems, security, industrial (including robots and IoT), and toys and games (including VR and AR). The higher-end digital still market is expected to shrink, because of the high-quality images delivered today by mobile phones.

This paper will describe the landscape of solid-state imaging, from its start in the 60s of the previous century until 2020, as well as an outlook of what can be expected in the coming years. The paper is organized as follows:

– History: An overview will be given of the major developments in the CCD and the CMOS era.
– CMOS scaling: CMOS technology in general (still) follows Moore's Law, but is this also the case for CMOS image sensor technology? Will the pixels further scale down to dimensions below the wavelength of the incoming light?
– Image processing: The fact that perfect images can be captured by means of non-perfect image sensors is greatly due to the widely and cheaply available processing power of image signal processors (ISPs).
– Human Eye: How close do the imagers match the quality of the human eye, and is there still anything to learn from the human visual system?
– Masterpieces of 3D integration: Many of the high quality characteristics and features offered by today's image sensors are the result of the successful 3D semiconductor processes available in the fabrication of CMOS image sensors.
– Future outlook: New materials and new concepts all pave the way for new applications.
– What about privacy and security?: Cameras will be ubiquitous. Big Brother could be watching you, anytime, anywhere!

2. History

The development of solid-state imaging started in the 60s of the previous century. Many important inventions, which still form the basis of today's devices, were already discovered by then: the integrating photodiode by Gene Weckler [3], the first photodiode array and the concept of the active pixel sensor by Peter Noble [4], the bucket-brigade device by Freek Sangster and Kees Teer [5], the charge-coupled devices by Willard Boyle and George Smith [6], the floating -diffusion amplifier by Walter Kosonocky [7], the CCD imager by Michael Tompsett [8], and later in the early 70s the correlated double sampling technique by Marvin White [9]. It is amazing how much of the today's technology rests on the shoulders of all these (and many more) giants. Despite these numerous advances, the CCD manufacturing technology did not evolve enough in the 70s to facilitate the building of devices with a sufficiently high yield at a reasonable cost. It took more than 10 years for a reproducible and reliable CCD manufacturing process to be developed. It was only in the mid 80s that the first camcorders based on solid-state image sensors were made available to the consumer market. The superior performance of CCDs of that period was based on the low dark-current and low-lag characteristics of the pinned photodiode [10] in combination with the introduction of base-resin micro lenses [11]. Despite the high image quality delivered by CCDs, they could only be fabricated in a dedicated MOS process [12]. In connection to the CCD image sensor, every camera needed a significant amount of peripheral circuitry around the CCD. All in all, these characteristics made every CCD imaging system quite expensive, voluminous, and power-hungry [13].

In the early 90s, the first papers about solid-state imaging devices fabricated in a standard CMOS process were published [14]. Image quality was rather poor in those passive-pixel devices, but the promise that they could be fabricated in a low cost, standard CMOS process, with all the peripheral circuitry integrated on-chip [15], gave a boost to CIS developments. With the incorporation of several CCD techniques into the CMOS active-pixel approach, such as correlated double sampling and intra-pixel charge transfer with new fixed-pattern noise removal circuits [16], as well as the low-voltage pinned photodiode [18], the performance level of the CMOS image sensor was brought to the level of CCDs, but with a lower cost and lower power budget compared to CCDs. It was shown again that "Everything that can be made in CMOS, will ultimately be made in CMOS".

3.0 CMOS Scaling

CMOS image sensors for classical image capturing applications became commercially available in the 90s of the previous century. Since that time an enormous evolution has taken place in the improvement of the manufacturing technology of the devices, driven by the goal to increase performance and decrease cost. Part of this evolution is shown in Figure 1.4.2: two parameters of published CIS studies (data taken from ISSCC, IEDM, and IISW papers) are depicted as a function of time; the pixel size of the CIS is illustrated together with the technology node used to fabricate these pixels. The lower graph shows the IRDS (International Roadmap for Devices and Systems), which corresponds to the most advanced CMOS technology available in the industry [19]. In most cases, this technology is used to fabricate DRAMs. From Figure 1.4.2 several of interesting lessons can be learned:

– Over the years, the CIS pixel size has decreased at about the same pace as the technology node. In the vertical direction, the "distance" between the lines is equal to a factor of 20. It is remarkable that this factor of 20 already existed in the early days of CMOS image sensors [13]. Despite the fact that over the past 30 years the pixel architecture has changed drastically, the ratio between the pixel size and technology node has almost remained constant. In other words, the CIS technology available to commercially fabricate image sensors is driving the pixel size. The resolution of the image sensor, which plays a very important role in marketing together with the pixel size, determines to a large extent the CIS chip size and optics form-factor. It can be easily understood that a smaller pixel size has a direct impact on the cost of CIS. Therefore, this price factor is one of the most important driving forces to push for smaller pixels.
– Around 2015 there was hesitation to further shrinkage of the pixels; a pixel size of 1µm seemed to be the limit. On the one hand, the technology to fabricate smaller pixels was available, but on the other hand, the performance of the devices with smaller pixels could not achieve an acceptable level (because of the small number of electrons that can be stored in, and low-light sensitivity of, pixels of that small size). Recently, efforts to further shrink the pixels have resumed at about the same pace as before. Such a re-start was made possible by the integration in the third dimension (see below).
– By comparing the available CIS technology node with the IRDS, it seems that the CIS technology is following the IRDS but with a delay (in the horizontal direction) of about one decade. This is because a "standard" DRAM technology is not suitable for manufacturing a CIS with an acceptable performance. Issues that need to be solved to adopt a DRAM technology in a CIS technology (to name a few) are:

○ Leakage current: a CIS collects every single free electron present in the silicon, even if this electron is generated by leakage or dark current. The latter can be optimized by lowering the electrical and mechanical stress in the pixels through dedicated processing steps. Leakage currents play a vital role when it comes down to low-light level applications, or when the image sensor is operated at higher temperatures,
○ Depth of the junctions: image sensors can increase their light sensitivity if photon-generated electrons generated deeper in the silicon can be collected. To do so, deeper junctions are essential,
○ Photodiodes: the pinned photodiode used in a CIS needs several extra implants to achieve a complete charge transfer,
○ Salicides/silicides: these metallization forms need to be avoided on top of

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the (photo-)diodes, because they will block the incoming light,
- ○ Threshold voltages: CIS pixels are analog circuit blocks which can benefit from native MOS-transistors to keep the possible voltage swing as large as possible. A large analog output swing enhances the signal-to-noise ratio and dynamic range of the image sensors,
- ○ Color filters and micro-lenses: these materials are not available in any "standard" CMOS process.

With today's technology node of DRAMs, measuring 10nm and even smaller, a pixel as small as 0.20μm×0.20μm could be fabricated, but unfortunately such a device can only store the bare minimum of electrons. For decent consumer-type images, a minimum signal-to-noise ratio (SNR) of 40dB is needed. For a photon shot noise limited imager, this translates into a pixel saturation level of 10,000 electrons. To store such a charge packet, a minimum pixel size of around 0.8μm×0.8μm is required. The effect of a shrinking maximum charge packet in a pixel is shown in Figure 1.4.3. From left to right, the signal-to-noise is reduced, starting from 40dB to 16dB (as indicated in the figure). The corresponding number of electrons needed to obtain the mentioned SNR as well as the pixel size to store these electrons is indicated as well. As can be seen from left to right, the quality of the image ranges from (almost) perfect to unacceptable. (This is a simulation of a photon shot noise limited case; read noise and cross-talk are not taken into account. Read noise improves with scaling, whereas cross-talk becomes worse with scaling.)

An exception to the aforementioned argument of 40dB can be the Quanta Image Sensor (QIS) [17]. In its simplest form, this device is a kind of binary coded imager: "0" = no photons and "1" = a minimum of 1 photon. Then a few hundred QIS pixels and/or frames finally compose a signal comparable to a single classical CIS pixel.

Building on the advances in semiconductor technologies need not always result in a trend towards smaller dimensions; the opposite can also be true. For instance, wafer scale (300mm Si wafers) image sensors of 20cm×20cm manufactured in a 65nm process have been reported [20], fabricated by making use of clever stitching technologies during the fabrication of the wafers [21].

4. Masterpieces of 3D Integration

In the early days of CMOS image sensors, the imagers were fabricated in a "standard" CMOS process with a few extra "imaging" options. However, it soon turned out that high image quality could only be realized with a dedicated CIS fabrication process that is still compatible in general with CMOS. In the race for the ever-shrinking pixel size, the third dimension of the silicon substrate became more and more important. Today CMOS image sensors are masterpieces of 3D integration. Especially the combination of a back-side illuminated imager stacked on the imager signal processor has resulted in a compact, low-cost, and high-performance imaging system. Methods such as stacking a CCD on a logic chip [22] and stacking a CIS on a logic chip [23] were already introduced much earlier. As with many new ideas, however, the realization of these concepts could only be made possible after an immense surge in the development of the technology, in this case hybrid bonding at the pixel level.

The cross-section shown in Figure 1.4.4 (courtesy of TechInsights, reverse engineered Sony IMX586 with 0.8μm pixel size) represents a Quad Bayer-based CIS. The architecture of such a pixel is shown in Figure 1.4.5:
- a basic block contains 4×4 pixels,
- every 2×2 matrix of pixels is provided with the same color filter and has a common source-follower output stage,
- the latter is connected to a joint column bus.

In Figure 1.4.4, from top to bottom (following the photon path) for this back-side illuminated stacked die, what can be recognized is the following:
- The micro-lenses which bring the photons in the middle of the pixel to limit the optical and electrical cross-talk (the micro-lenses are not perfectly centered above the pixels, but they are shifted slightly to the center of the device to compensate for optical artifacts [24]),
- The color filters which split the information into the various color planes, mostly red, green, and blue. The color filters are deposited between tiny small tungsten walls, allowing the sidewall of the filters to be almost perfect, moreover the tungsten walls also act as waveguides [25]. Notice that the color filters cover two pixels each time. This is the typical filter architecture for the so-called Quad Bayer pattern configuration [26],
- Although the color filters and the micro-lenses are expected to have a repetitive structure across the total imaging array, in Figure 1.4.4 it can be observed that this is not always the case. In one situation, two pixels, instead of a single one, are covered with a single micro-lens. This architecture is used to create a phase detective auto-focus (PDAF) pixel. This is a pixel with a special feature to indicate whether the image projected on the sensor is in focus or out of focus [27],
- Below the color filters, dedicated anti-reflective coatings are incorporated to ensure that the maximum number of photons can reach the silicon,
- Inside the silicon, the (volume of the) pixels are defined by deep trench isolations (DTIs), etched from the backside. These trenches can be very deep and very narrow, the side walls of the trenches can be oxidized, and the remaining gaps can be refilled with poly-crystalline silicon or tungsten. The deep trenches have a positive effect on the optical as well as electrical cross-talk [28],
- Although not shown, in the "bulk" of the silicon and between the trenches is where the pinned photodiodes are located. This back-side illuminated device was originally fabricated on a thick silicon substrate. The latter is thinned down to about 3μm to allow back-side illumination,
- At the original front side, the MOS transistors are formed, being separated from each other by means of shallow trench isolations (STIs). From Figure 1.4.4 it can be concluded that the repetitive structure of the STI also corresponds to two pixels, which again illustrates the concept of the Quad Bayer design, in which 2 × 2 pixels share the source-follower-based readout structure [26],
- The former top layer of the image sensor is provided with four layers of interconnect,
- The back-side illuminated image sensor is hybrid-bonded to the processing part by means of a direct Cu-Cu bond pad interconnect. The hybrid bond pads in the active array have no electrical function; only in the periphery of the imager are the Cu-Cu hybrid bond pads used as electrical interconnects [29],
- The digital processing unit below the imager is provided with seven metal layers as the interconnect.

It should be clear that CMOS image sensors combine a complex fabrication technology with know-how in the fields of optics, device physics, and electronic design. If pixels continue to reduce in size in the future, integrating them in the third dimension will play an even larger role. For instance, the photodiode will be no longer present along the front side of the silicon, but will be buried into the depth of the silicon as well. To transfer the electrons out of this photodiode, the transfer gate of the pixel will also need to be built vertically into the silicon [30].

5. Image Processing

One should realize that the light sensitivity of a pixel is proportional to the area of the in-pixel photodiode. For a long time, pixels of 5.6μm×5.6μm were considered the de facto standard, but these days image sensors with a pixel size of 0.7μm×0.7μm are already commercially available [31]. This means that the latter catches only 1.5% of the photons in comparison with the former pixel.

Despite capturing only 1.5% of the photons, today's imagers deliver a better image quality than was the case a decade ago. This is thanks to progress made over the years in the digital processing of raw data delivered by the sensor. An example of how poor-quality raw image sensor data can result in a decent image is shown in Figure 1.4.6: on the left, the raw output signal of an imager with a Bayer CFA (color filter architecture) pattern is shown with many artefacts such as column defects, pixel defects, temporal noise, spatial noise, lens vignetting, color filter imperfections, and leakage current; on the right, the result is shown after the dedicated digital processing of the data.

Algorithms used to turn the left image into the right one are [32]:
- Correction of defects or deviating pixels (of all pixels present in an imaging array 0.1‰ can be defect; pixels deliver an analog value and their non-uniformity from pixel to pixel can be 1%),
- Demosaicing (every pixel in a color image sensor is made sensitive to only a single color, but on the display, every pixel requires an RGB value),
- Color correction (as the CFA is not perfect, neither is the color signal delivered by the sensor),
- Correction of fixed-pattern noise (pixel circuitry and column circuitry are analog in nature, so there will be differences between these circuits showing up as a fixed spatial noise component),
- Sophisticated filtering (of multiple images) to decrease the temporal noise (Johnson noise, 1/f noise, electrical cross-talk, kTC noise, quantization error, RTS noise, and so on),
- Rolling shutter distortion correction,
- And so on.

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All these sophisticated algorithms present in RISC processors are currently being challenged by architectures based on artificial intelligence (AI) and deep learning (DL) neural networks (NN). The first notably promising results of NN in combination with image sensors being published, report demosaicing based on deep machine learning, which makes the final image quality independent of the CFA on top of CIS pixels [33]. As a consequence, the CFA can be optimized for other image quality parameters than simply color fidelity.

Even a perfectly performing image sensor in a real camera cannot comply with all requirements a photographer demands from the camera when capturing a single image. For that reason modern smart phones start taking photos as soon as the user activates the camera function [34]. In fact, when the user taps the "red" button to take a photo, the photo has already been taken and the camera simply selects one of the last pictures stored in the memory. Or in a more sophisticated way, the final photo presented to the user is a combination of several pictures stored in the memory of the camera. In this case not only can a zero shutter lag be created, but based on the stack of images present in the memory, several optimizations can be realized: errors or shortcomings in one picture are minimized by using the content of other pictures. Examples of this processing method are:

– High dynamic range (combining (sub-)images with different exposure times and/or different gain settings),
– Noise reduction (bilateral filtering of several images),
– Auto-focusing (taking images at different focus settings and choosing the best suited one),
– Super-resolution (using a sensor shift between the shooting of several images),
– Image stabilization (calculating a motion vector from multiple images and using this to correct motion artefacts in the final image),
– And so on.

The modern stacking technology with multiple layers (imager, DRAM, logic processor) [35] makes it possible to combine aforementioned technologies into sophisticated digital processing of multiple images stored in the memory. As can be expected, the digital processing core can and will be partly replaced by AI and/or NN circuitry [36]. In this way, two basic goals can be targeted by means of on-the-fly and embedded artificial intelligence close to the image sensor:

– Improving the functionality and quality of the imaging system, for example, high dynamic range [37].
– Embedding analytics (security applications) to recognize specific objects, including humans and face recognition.

6. Human Eye

If a comparison is made between the human visual system and a digital camera, it is remarkable that in some aspects the human eye is (still) far superior to the image sensor (power dissipation, color fidelity, and so on). However, in other aspects an image sensor easily can beat the human eye (resolution, speed, temperature range, extended wavelengths, and so on) [38]. A significant advantage of the human eye is the ability to process images locally at the level of the retina level ("edge processing"), with combining high resolution in the center and low resolution outside the field of view. In this way minimal information needs to be transported to the brain for further processing, and the transporting is done through a limited number of nerves. Nonetheless, it is still not understood how the human visual system can make those beautiful images all of us can observe through only a single low-performance eye-lens, and the limited data transport to the brain based on a sparse, asynchronous stream of digital spike events [39]. Here is where the digital image sensor still can learn from the human visual system. Until recently, hardly any attention was paid to processing at the sensor level. These days, the first attempts to substantially reduce the output data of an imager have been reported, such as imagers that are put to sleep and only wake up if an event takes place in the scenery [40], or event-based devices [41]. Further incorporation of edge processing at the sensor level will drastically reduce the data traffic off the sensor die. Also in this case, full exploitation of the stacking technology can play an important role in placing AI or NN processing units close to the pixels. Stacking "extends" the volume of the pixels into the third dimension, the extra volume of which can be used to implement more analog and digital circuitry. Embedding edge processing in combination with keeping track of the data and pixel statistics will allow captured images to be processed based on the "experience" of the sensor/camera.

7. Future Outlook

In the past the main driver of the solid-state imaging technology was the mobile phone industry. Will this still be the case in the future? Most probably in the short term it will, because smart phones are already being equipped with multiple cameras, one or two on the front side, three or four on the back side. Moreover the consumer trend seems to be the frequent purchasing of increasingly more expensive mobile phones with more camera options and features. It is clear that the camera performance of a mobile phone has become a major selection criterion in the purchase of a specific mobile phone.
Another major solid-state imaging trend is the broadening of applications for silicon-based cameras, not only for shooting nice pictures, but also for using the image sensor for other purposes. Examples are:

– Extension of the spectrum of the sensors. Important developments have been announced with increased near-IR sensor sensitivity through extra trenches [42], or application of pyramidal surface structures [43]. This will expand the use of silicon detectors to the near-IR field. Applications are: eye trackers, gesture control, food sorting, and distance measurements by means of time-of-flight sensors [44],
– Image sensors that can detect the polarization of the light. This characteristic allows a camera to detect the nature of the material (plastics, metals, and so on), to locate stress in materials, to avoid reflections when looking through glass surfaces, and so on [45],
– Determining the energy of an arriving photon. This application will open many doors in the medical world. In X-ray imaging, knowledge of the energy of the incoming photon could reveal more information about possible diseases and could help the medical world to perform better and earlier diagnoses of cancer,
– Detection of the arrival time of incoming photons. This cannot be done with a consumer solid-state sensor, but by means of a Single Photon Avalanche Photodiode (SPAD). In the early days of SPAD, the resolution was very limited as was the fill factor and photon detection probability. However, advances in the technology in combination with stacking, has led to devices with high resolution and with a high fill factor [46].

It must also be mentioned that a great amount of research is taking place in the field of non-silicon-based photo converters. For instance, new materials (Perovskites [47], organic photoconverters [48], quantum dots [49], and so on) are being used in combination with silicon readout integrated circuitry (ROIC). Silicon-based detectors do respond to incoming light up to a wavelength of 1.1μm. Beyond this wavelength, silicon becomes transparent for incoming photons. However, silicon (CMOS) technology has developed to such a level that it will become extremely difficult to find other materials and technologies that perform better in the (extended) visible spectrum than silicon imagers. The combination of back-side illuminated pinned photodiodes and correlated-double sampling results in devices that approach perfection as far as noise and quantum efficiency are concerned [50] [51]. However, if the detection of wavelengths outside the "silicon" spectrum is required, these new materials in combination with a Si-CMOS-based ROIC are certainly valuable options. Recently an image sensor in which InGaAs is used as the photon-to-electron converter has been applied on top of a hybrid bonded silicon readout IC [52].

Certainly one of the most promising new developments in the field of solid-state imaging is the combination of an image sensor stacked on an artificial intelligence processing chip. This new "marriage" is opening up a multitude of new applications and new horizons, including the field of biometric optical sensors. The stacking of a CIS on top of an FPGA was the very first attempt to realize the combination imaging with a programmable processor [53]. Since then, the first announcement from academia [54] has been made, and even the first product [55] has been introduced with a stacked CIS – neural network combination. The pixels of the image sensor can be seen as the very first layer of the neural network. The latter can be programmed and trained to comply with various customized requirements. In this way more focus will be placed on edge processing, and embedded imaging solutions will become faster and much smarter. In the recent past, most progress in the field of artificial intelligence is made in the combination of imaging with AI.

8. Privacy and Security

Following the evolution of the "Internet of Things" (IoT) concept: it all started with very simple RFID tags (inventory goods and loss prevention), followed by the addition of more applications (surveillance, security, healthcare, food safety, document management), reaching the point of tracking people's location and object recognition. The next step will be remote monitoring and controlling of objects. However, for all this "luxury" a substantial privacy price must be paid: Big Brother could be watching us, more closely than ever expected! In the near future, cameras connected wirelessly will be located anywhere and functioning at all times. Examples are: smart doorbell, smart refrigerator, smart traffic lights, smart energy meter, smart banking, smart car, smart office, smart home, smart baggage scanner, smart billboards, smart grocery store, smart toilet, smart … For all these applications the same rule is valid: Big Brother can "steal" a lot of data to invade our privacy at any time! In many cases the line between security and privacy is paper thin.

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New developments in technology invariably introduce new social issues. In many of the aforementioned examples, images are being collected while it is actually not necessary to have/use full resolution images for that specific application. For instance if a camera is used to count people that are passing through an entrance, then the camera should be used for this specific purpose and not to recognize who is passing through that entrance. Counting people can be achieved without taking and storing images. The danger exists that once the images are taken and stored, they can be used for other purposes as well, even at a later time. Potential risk of data manipulation by means of AI is only a single step away. One should use the advantages of the technology without exploiting the dangers. This way of working is known as "responsible innovation" [56], and the very first example is now on the market: a "people counter" by means of an event-based image sensor. This imager captures information in which one cannot recognize individuals [57]. The ISSCC community can play an important role in the R&D of "responsible innovation" technologies in the field of digital image sensors.

Everyone is concerned about losing his/her privacy, but in cases of urgency or danger, one is willing to sacrifice part of his/her privacy in return for a safe harbor. Examples of this concession can be found after great disasters like 9/11 or the corona pandemic. However, once the threat of the disasters has disappeared, the part of the privacy lost is not automatically regained. Governments rely on convincing arguments to take part of the privacy of their people, but are not so easily willing to give back what they have taken away.

9. Conclusion

Solid-state imaging has travelled on a long and winding road from its early days in the 60s of the previous century to reach the technology level available today. This paper has strived to give a glimpse into the history, as well as a look at the future, of solid-state image capturing technology.

<u>"There's more to the picture than meets the eye"</u>: a consumer does not realize what happens in a digital camera when he/she taps the red button to take a picture. Although much can and will go wrong while shooting an image (noise, artefacts, limited dynamic range, and so on), thanks to clever and extended digital image processing, near-perfect images are being delivered by cameras, even if the camera operates in a harsh environment.

<u>"and in the future it will only become more so"</u>: the availability of a mature fabrication technology has played a crucial role in bringing solid-state imagers to consumer products. What is more, history is now repeating itself: the methods for stacking an imager on top of an AI/NN processing chip are maturing, opening up a completely new world of technologies and applications. The image sensors will no longer solely be used to shoot nice images, but it will also sense incoming light information. The AI/NN will process the generated data and can result in improved quality images or in object recognition.

A great future lies ahead of imaging engineers, but also an overwhelming responsibility is resting on their shoulders: to respect the privacy of users of the imaging technologies that are developed by them!

Acknowledgements:

The author would like to express his sincere appreciation to:

- Edoardo, Kofi and Matteo for their help in preparing this paper,
- Eric, Nobu, Johannes, Guy and Vladimir for their reviewing assistance,
- Sarah for her "English" advice,
- All his (former) co-workers, all his (former) colleagues, all his (former) clients and all his (former) competitors for creating a stimulating and challenging environment to work in for 45 years,
- His family for their support throughout this great solid-state imaging journey.

**The title of this talk "There's More to the Picture than Meets the Eye" is originating from a song of Neil Young "Hey Hey, My My" written in 1978.*

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Figure 1.4.1. Overview of the world-wide CMOS image sensor market (source: IC Insights).

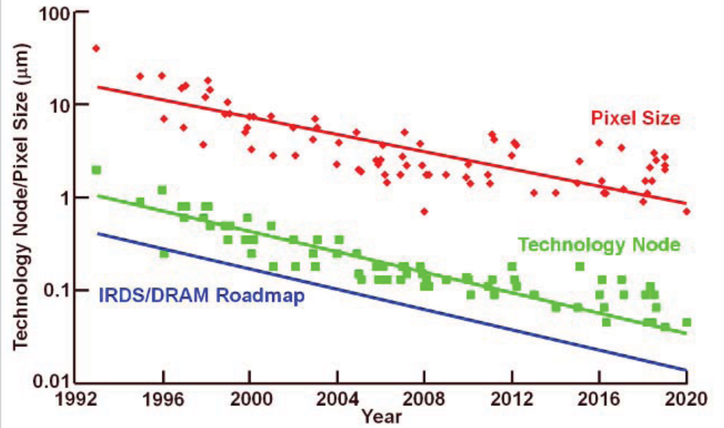

Figure 1.4.2.Evolution of the pixel size, fabrication technology node and the International Roadmap for Devices and Systems (source: ISSCC, IEDM, IISW).

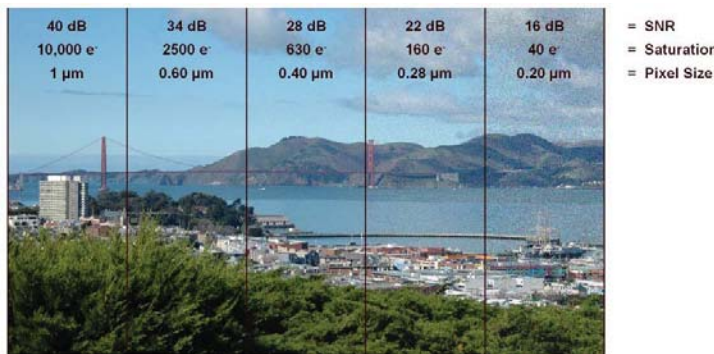

Figure 1.4.3. Visualization of the effect of shrinking pixel size and of maximum charge packet on the image quality.

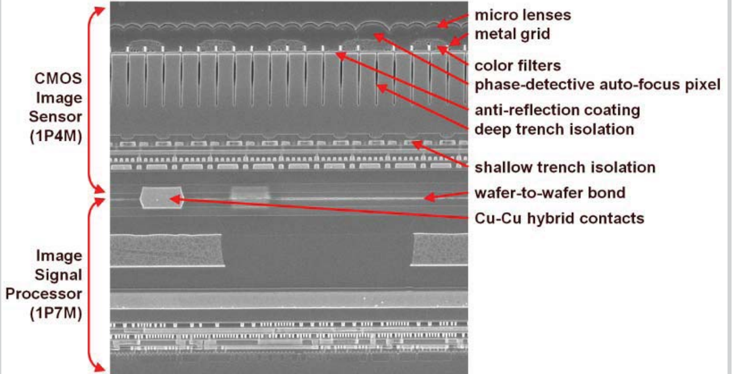

Figure 1.4.4. Cross-section of a Quad-Bayer based CIS, stacked on a logic chip by means of Cu-Cu hybrid bonding (source TechInsights).

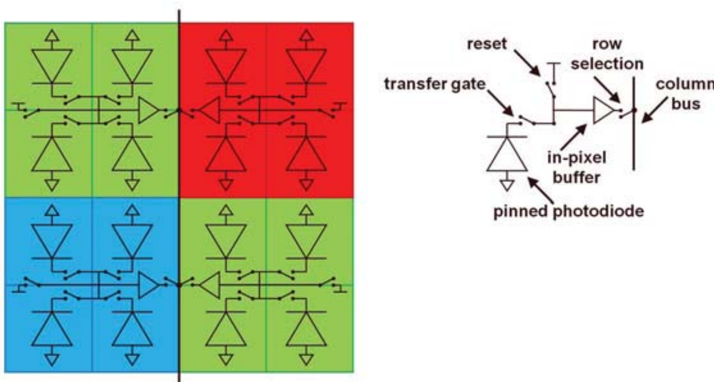

Figure 1.4.5. Architecture of a Quad-Bayer based CIS pixel (left 4 times 2x2 pixel configuration, right detailed circuit of a single photodiode + readout circuitry).

Figure 1.4.6. Raw data delivered by the sensor (left) and the final image after dedicated image processing (right).

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