Temperature sensors incorporated into a CMOS image sensor with column zoom ADCs

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***Abstract*—This paper proposes an array of nMOS based temperature sensors incorporated into a CMOS image sensor (CIS) for thermal compensation of the latter. Each temperature sensor features the same area as that of an image pixel. Both the temperature and the image sensors' outputs are read out by the column-level zoom ADCs, each of which offers 16 bits, with a 4-bit unit capacitor array (UCA) SAR and a 13-bit 2nd-order incremental delta-sigma ADC (DSADC) as the first and the second stage, respectively. The proposed UCA with improved switching and decoding technique minimizes capacitor area and switching energy, by 50 % and 75 %, respectively, compared to a conventional binary weight array (BWA) counterpart. The column zoom ADC samples twice as fast while keeping its linearity, or, expands the dynamic range by 15 dB, for the image sensors, compared to a DSADC only alternative. To digitize the temperature sensor, the proposed zoom ADC is capable of quantization errors less than 16 µV, which is equivalent to a 0.125 °C resolution for a 130 µV/°C temperature coefficient. The proposed temperature sensor is simulated to keep its errors within ±0.21 °C upon 2nd-order curve fitting, with 3 sigma Monte Carlo inaccuracies less than ±0.74 °C, between 0 and 100 °C, at a power and an area of 144 µW and 121 µm², respectively, with a sampling period of 64 µs.**

Keywords—temperature sensor, CMOS image sensor, zoom ADC, analog-to-digital converter, ADC, SAR, delta-sigma

I. INTRODUCTION

A typical CIS array may contain more than tens of megapixels, which have process variations among themselves, as all semiconductor devices. However, most process sensitive parameters, e.g., poly-resistor value, are also thermal sensitive. To calibrate the process dependent parameters within the temperature range of its application, temperature sensors could be implemented inside the image pixel array, replacing some of the image pixels, to sense the temperature locally, e.g., for dark current (or, dark FPN) compensation [1]. Being in the same array, the temperature sensors share the readout circuits with the image pixels located in the same column. However, the design requirements of the ADCs for the two types of sensors are vastly different. A typical CIS's column ADC has 12 bits with an input range of 1 Vpp (which is the pixel's output range), and therefore, a resolution of approximately 0.25 mV. Supposing its frame rate is 60 fps, a 1080p CIS array's column ADCs have to operate faster than 65 kHz (=60×1080). In contrast, a typical nMOS based temperature sensor's thermal coefficient is 130 µV/°C(=$k/q \cdot \ln(4)$), for a current ratio of 4, e.g., where k is the Boltzmann's constant while q being the electronic charge. The accuracy required in temperature sensors for dark current compensation is 1 °C [1], and to target a resolution of 0.25 °C, the ADC has to offer a resolution as fine as 32 µV, operating at a speed from a few tens to a few kilo Hz. Designing one ADC for both sensors requires it to provide a resolution of 30 µV within an input voltage range of 1 V and therefore a minimum 15 bits, when the sampling rate is at a minimum 65 kHz. Considering the above mentioned design challenges, this design employs a zoom ADC with programmable gain and conversion time. By using a SAR to assist the delta-sigma ADC, one either obtains more quantization bits while maintaining the same conversion time (oversampling ratio, OSR) and hardware complexity of the on-chip digital delta-sigma filter, or, to cut down the conversion time (OSR) while maintaining its linearity. This is in comparison to a pure DSADC alternative. To minimize the additional area and energy incurred by the first-stage SAR, a UCA based switching and decoding method, which saves the SAR's capacitor area and switching energy by 50 % and 75 %, is proposed for the first time in this paper. The aforementioned savings in area and energy are in comparison to a binary weight array (BWA) or UCA [2] of the same number of bits. The expense paid is less than 5 % area and power increment incurred by the UCA SAR (comparing to a DSADC only alternative), but gains 3 bits (or 18 dB more dynamic range, in theory). Moreover, by using column 2nd-order incremental delta-sigma ADCs, the programmable gain amplifier (PGA) circuits are eliminated from a CIS, as the delta-sigma's OSR can be adjusted to accommodate between a faster operating speed and a finer resolution (lower noise), and overall, a wider dynamic range. 2nd-order DSADCs have been used as column ADCs for CIS in [3][4]. SAR has been proposed to assist delta-sigma ADC in its loop [5]; however, for DC-input ADCs, it is more energy and time efficient to locate the SAR outside instead of inside the delta-sigma modulator [6], as a zoom ADC. However, unlike [6], this paper has the analog equivalent of the digital outputs from the first-stage SAR deduced from the input capacitor's charge sampling instead of having the input analog voltage multiplied accordingly. The proposed temperature sensor employs an nMOS instead of BJT based front-ends, for avoiding electronic luminescence (EL) caused by forward biased BJTs to surrounding image pixels [7]. Compared to previous publications on MOSFET based temperature sensors in [8]–[12], the proposed temperature sensor has the minimum area, comparable accuracy and FOM, when providing on-chip digital outputs. This paper is organized as follows. Section II explains the operating principles of the UCA, the zoom-in ADC, and the temperature sensor front-end with their schematics. Section III shows the simulation results of each building block and the temperature sensor as a whole. Conclusions and future works are given in section 0.

II. OPERATING PRINCIPLES

A. UCA SAR

Fig. 1 shows a UCA SAR's schematic: each time a bit switches, a voltage of $\pm VREF \cdot Cu/2Ctotal$ ($\approx \pm VREF/16$ if omitting the parasitic capacitance) is added or subtracted from the charge balancing node Vx, depending on the logic value of Bi (1 or 0), where Cu and $Ctotal$ are the unit capacitor and the total capacitance weight in the ADC, respectively; $VCM=VREF/2$. On one hand, during each switching, the charge balancing node Vx steps up or down by a voltage less than that in a BWA. However, in the conventional UCA described in [2], Vx keeps switching up and down even after it is close to the level of VCM within a voltage of $\Delta=VREF/2^N$'s, and this incurs unnecessary switching energy. The reasons are that, in a UCA, the digital representation of the input voltage's level can readily be deduced from the moment that two neighbouring bits show opposite signs, when Vx can be approximated to VCM, within errors of $\pm\Delta$. The proposed timing diagram in this paper is shown in Fig. 1, where the comparator and the following bits stop comparing or switching after two neighbouring bits have opposite signs. The proposed

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switching method provides 4 bits instead of 3 as in [2], when using the same number of capacitors. In other words, capacitor area is saved by 50 % for the same number of bits, compared to [2] or a conventional BWA. The reasons are in addition to positive and negative steps, there is a third switching mode of the capacitors—non-switching. If the positive and the negative steps generate digital output 1 and 0, respectively, the non-switching mode is analogous to a 0.5, and this helps double the number of stairs in practice and gains an extra bit. However, the thermometer to binary encoder, which is comparable to that for a delay-line based time to digital converter (TDC) [13] is still of 3-bit complexity, with an extra Magnificent Significant Bit (MSB).

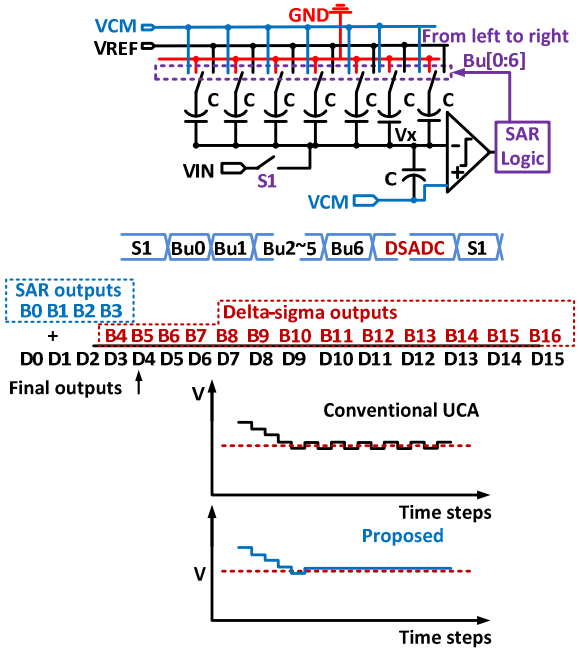


Fig. 1 Proposed UCA SAR ADC and its timing diagram.

B. *zoom ADC*

The proposed SAR-assisted 2nd-order incremental delta-sigma ADC (zoom ADC) is shown in Fig. 2, with the delta-sigma ADC in reference to [12]. It places the SAR-assisted DAC voltage at the position of that of the conventional common mode voltage. The delta-sigma ADC works in series with the UCA SAR. Once the comparison for all the 4 bits are complete in the SAR, whose outputs are fed into the capacitor array connected to *VDAC_SAR* shown in Fig. 2, and the conversion in the delta-sigma ADC begins. Since *VDAC_SAR*=*Vx*, the charge sampled on *C11*(=*Ctotal*) during phase 2 is approximately (*VIN*-*VDAC_SAR*)·*Ctotal* ≈(*VCM*-*Vx*)·*Ctotal* (*Ctotal* and V_X are the total capacitance and final V_X value of the SAR and *Ctotal* = *C11*). This is mathematically similar to using a multi-bit quantizer in the delta-sigma loop. However, the fact that the input level does not change over the conversion period for a temperature/image sensor makes it possible to move the SAR outside the delta-sigma loop. Using a 4-bit SAR, the input charge sampled (*VIN*-*VDAC_SAR*) is suppressed by a factor of 8 ($8=2^3$, losing 1 bit for the digital error correction shown in Fig. 1). In other words, the input range of the delta-sigma modulator is reduced to its original 1/8. Meantime, the requirements of the output swing (in the opamp) in the delta-sigma modulator can also be reduced to its original 1/8. The capacitor size of *C12* and *C22* can be reduced accordingly.

A. *Temperature sensor front-end*

The proposed temperature sensors are imbedded inside the CIS array, sharing the power supply voltages, column and row buses, as shown in Fig. 3 with their system block diagram. Their timing diagram is shown in Fig. 4: When the row select switch (RS) is on at $t_1(0)$, the pixel output voltage V_{TS}=V_{PIX_SUP}–V_{GS} (V_{GS} is the gate-source voltage of M_{SF}), when ignoring the voltage drop on M_{RS}. When biased in subthreshold region, an nMOS transistor has an I-V characteristic [15] of:

$$I_1 = I_{DS} \cdot e^{(V_{GS}-V_{TH})/nV_T} \quad (1)$$

where I_1, I_{DS}, V_{TH}, V_T are the column bias, saturation current, threshold voltage of the transistor M_{SF} and V_T=kT/q (k is Boltzmann's constant, q is electronic charge and T is the temperature), respectively; while n is a process dependent factor. From (1), one obtains mathematically:

$$ln\left(\frac{I_1}{I_{DS}}\right) = \frac{(V_{GS}-V_{TH})}{nV_T} \quad (2)$$

As shown in Fig. 4, when two ratiometric currents $I_{1,1}$, $I_{1,2}$ are biased as I_1 sequentially, the voltage change at V_{TS} becomes:

$$V_{GS,2} - V_{GS,1} = n\frac{kT}{q}ln(N) \quad (3)$$

Which is proportional to the temperature T; where N=$I_{1,1}/I_{1,2}$ is the ratiometric current ratio, which is 4 in this design. During $T_{ADC,1}$ and $T_{ADC,2}$, the temperature sensors are readout: sensors in same the row are readout together by the column ADC, and then, row by row, the entire array of sensors are all read out. In this way, the introduced temperature sensors only incur additional area, power and conversion time proportional to its spatial occupancy among the entire image sensor array. For instance, if the maximum predictable thermal gradient is around 0.25 ºC for every 1 mm when the pixel pitch is 10 µm, 1 temperature sensor for every 10000 (=100×100) image sensor will suffice, incurring only 0.01 % additional area, power and readout time, or the same portion of dead image pixels. As the nMOS M_{SF}'s body cannot be connected to its source in this technology, the difference in the threshold voltage V_{TH} during $I_{1,1}$ and $I_{1,2}$ deserves some attention. However, $\partial V_{TH}/\partial V_{SB} = \gamma/2\sqrt{(2\Phi_F+V_{SB})}$ is lowered when V_{SB} increases. Since V_{SB} (close to V_{TS}) is around 2 V in practice, the aforementioned body effect can be ignored for the accuracy requirement in this paper. In transistor level implementation, one has to make sure that M_{SF} works in subthreshold region. In Fig. 4, V_{PIX} is the image pixel voltage output and its schematic is similar to that described in [3].

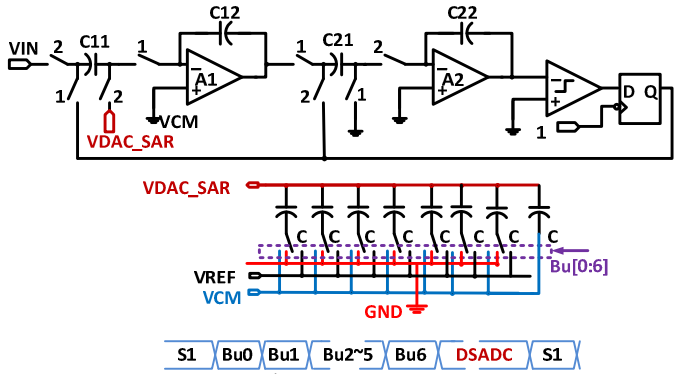


Fig. 2 Schematic of proposed 2nd order delta-sigma ADC for the zoom ADC.

III. Simulation Results

A. *Capacitor swithcing energy in UCA SAR*

To compare the switching energy of the proposed and the conventional UCA methods shown in Fig. 1, along with that of a conventional BWA, simulations are performed in MATLAB. This is performed by modelling the charge balancing node *Vx*'s voltage changes, versus the input range of the ADC through its conversion steps and calculating the switching energy. Using the proposed UCA method, the switching energy dissipated by the capacitor array is saved, particularly around the middle of the input range—*VCM*, where, in contrast, is the most energy-hungry region for the other two conventional techniques, as illustrated in Fig. 5. The reasons are that in the proposed method, the closer an input voltage is to the *VCM*, the fewer the UCA SAR's active cycles are, before the comparator and the capacitors idle. The total number of capacitors in the

proposed design is only half as much as those in [2] or in a conventional BWA. In this way, the switching energy is further reduced, by at least 75%, compared to a conventional BWA alternative. In this design, the averaged operating cycles of the comparator for a ramp voltage input is 4, which is the same as that in a BWA SAR. Moreover, most of the time the comparator output is monotonous, being static at "0" or "1". According to the simulation results in this technology, a non-switching step consumes around 15 % energy as in a switching one. Assuming the leakage current in the comparator is negligible during its idling, the proposed 4-bit UCA also saves comparator energy by a total of around 50 %. The UCA based SAR has more conversion cycles than a conventional alternative. However, the total conversion time of a 4-bit UCA SAR in this design is much less than 1 of the 16 or 128 cycles of the delta-sigma in the zoom ADC.

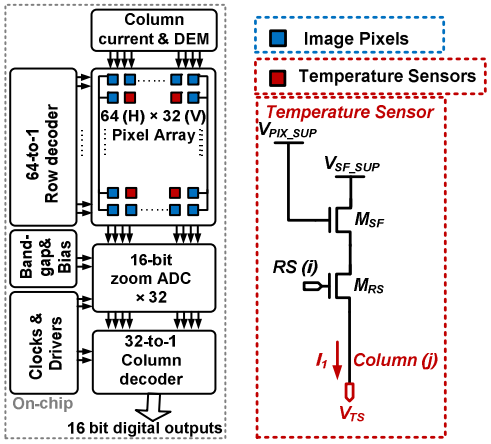


Fig. 3 Proposed temperature sensor's system diagram and schematic.

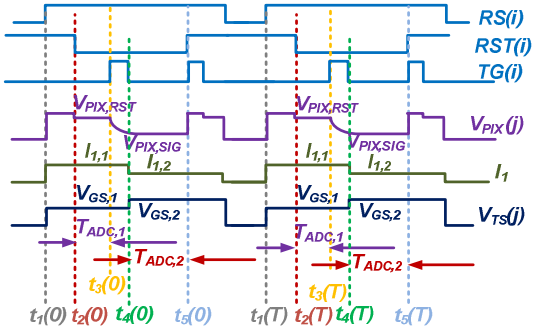


Fig. 4 Proposed temperature sensor's timing diagram.

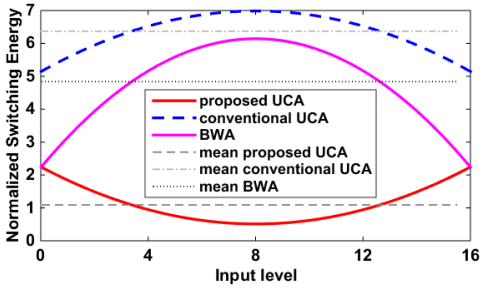
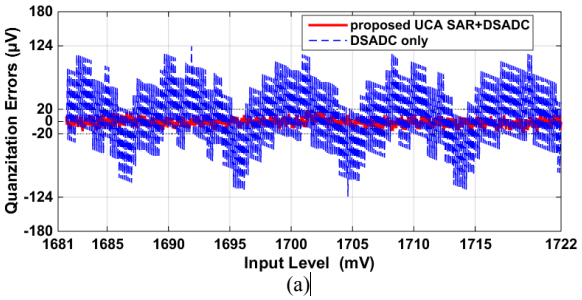


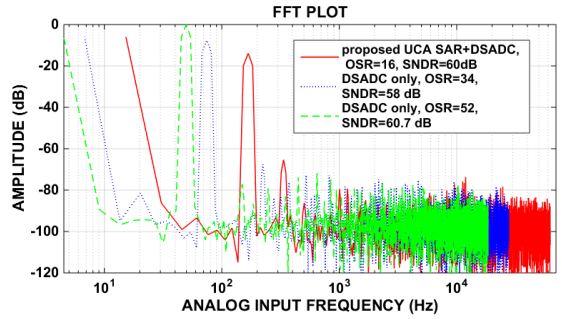
Fig. 5 MATLAB simulations of energy dissipation in a 4-bit capacitor array using BWA, UCA [2] and proposed UCA method of the same unit capacitor size.

B. *Linearity of zoom ADC*

Cadence transistor level simulations are performed in 0.18 µm 3.3 V technology, using the proposed zoom ADC's schematic shown in Fig. 1 and Fig. 2, with a decimator filter similar to that in [14]. The first opamp shown in Fig. 2 has a gain and a UBW of 65 dB and 40 MHz. The second opamp has a similar gain but its UBW is a quarter as in the first one. The reference voltage and the sampling clock rate are 1 V and 2 MHz. Two separate simulations are performed. The first is on static linearity, performed using a ramp input voltage between 1681 mV and 1722 mV (typical output level of the proposed temperature sensor front-end described in II.A), with 1500 sampled points. The results are shown in Fig. 6 (a) and have verified that linearity is improved by at least 15 dB, from 1 °C (124 µV) to 0.17 °C (20 µV), a little bit less than 8 time improvements (in theory) mentioned in section II.B. The second simulation is performed with sine wave input of amplitude of 0.8 Vpp with various frequencies and its results are shown in Fig. 6 (b), which indicate that the proposed zoom ADC is able to operate twice as fast with 2 dB higher dynamic range, as a column ADC for image sensors.



(a)



(b)

Fig. 6 Simulation results of static and dynamic linearity using Cadence transistor level designs. (a) Quantization errors (linearity) of the zoom ADC. (b) Spectral response and SNDR (signal to noise and distortion ratio) of the zoom ADC.

C. *Temperature sensor front-end*

The transistor level design of the temperature sensor proposed in section II.A is constrained by the available area inside the image sensor array. In other words, the temperature sensor's taking additional area means a larger number of dead image pixels. Therefore, in this design, it is decided that each temperature sensor should take no more than that of one image pixel's area. On the other hand, a smaller-sized temperature sensor may lead to more process variations, which, in general, either make calibration more time consuming or increase measurement errors in mass production. To verify its process variations in transistor level, 100 Monte Carlo simulations have been performed on the proposed nMOS based temperature sensor front-end (SF sized 8 µm ×8 /0.35 µm) and are shown in Fig. 7, which indicates a resolution of 130 µV/°C in average. By calibrating each sensor at 50 °C, their 3 sigma (σ) errors (including process variations) among the 100 Monte Carlo simulations are within ±0.53 °C, deviating from a 2nd-order mater curve, from 0 to 100 °C. The errors due to curvature in the master curve are less than ±0.1 °C. As a single-ended rather than two differential nMOS transistors are used for thermal sensing, threshold mismatches are eliminated. The process variations of "*n*" and "*N*" in equation (3) can be corrected by one-point calibration. What remain uncorrected are the geometrical mismatches of the M_{SF} and the column level current biasing circuit that generates I_1 (Fig. 3), among the temperature sensor array. They have caused M_{SF}'s transfer function to further deviate from equation (1)– the simplified model.

D. *nMOS based temperature sensor with digital outputs*

The nMOS based temperature sensor front-end proposed in section II.A is quantized by the the zoom ADC described in section II.B (V_{TS} shown in Fig. 3 is connected to *VIN* shown in

Fig. 2). The reasons for choosing nMOS over BJT alternative is due to the latter could incur EL to its neigbouring image pixels [7]. Transistor level simulations are performed in 0.18 µm CIS technology using Cadence Environment and are plotted in Fig. 8. The digital outputs are approximately from 3200 digital number (DN) to 4000 DN between 0 and 100 ºC, so the temperature's resolution is around 0.125 ºC. The sensor's errors due to curvature is less than ±0.21 ºC, after a 2nd-order curve fitting which can correct some of the errors incurred by leakage current, as an non-ideality to equation (3). Since an incremental delta-sigma ADC relies on feedback loop to make sure that its digital output bit stream's representation equals its analog input, independent of temperatures or process variations, it is safe to assume the overall temperature sensor's 3 σ process variations using that of the front-end sensor shown in Fig. 7. As a result, the proposed temperature sensor's 3 σ accuracy is estimated to be around 0.74 ºC, including both curvature and mismatches. Noise affects the finest resolution of the sensor. The kTC noise of the zoom ADC is √kT/C/OSR, in theory. When OSR=128, to make the kTC noise less than 0.125 ºC (the sensor's required resolution), the input sampling cap *C11* has to be larger than 163 fF, which is rounded up to 200 fF. As a result, the unit-size *C* in the UCA shown in Fig. 1 is 25 fF=(200 fF/8).

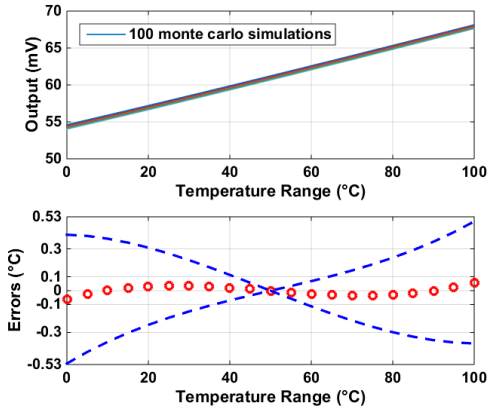


Fig. 7 100 Monte Carlo simulations of transistor-level temperature sensor front-end outputs (ΔV_{GS}) and their temperature errors including process variatons after a one-point calibration at 50 ^{0}C and a 2nd-order master curve fitting, from 0 to 100 ºC.

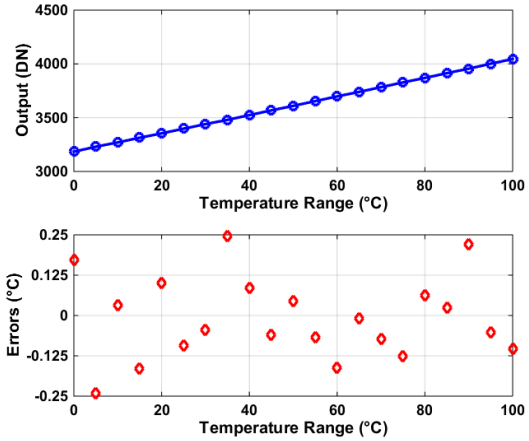


Fig. 8 Transistor level simulation results of the proposed temperature sensor: its digital outputs versus temperature and its errors due to curvature after a 2nd-order curve fitting, from 0 to 100 ^{0}C.

IV. Conclusions & Future Works

This paper proposes an array of temperature sensors incorporated into a CMOS image sensor. The nMOS based temperature sensors are quantized by column-level zoom ADCs, which also digitize the image pixels in the same array. The zoom ADC's transistor level simulations demonstrate twice faster sampling speed and 2 dB higher SNDR, comparing to the case using DSADC only, for the image pixels. Its linearity is improved by 15 dB (or, its resolution is improved by a factor of 6), compared to using DSADC alone, as the temperature sensors' column quantizer. The UCA based SAR incurred at least 50 % less capacitor area and 75% less capacitor switching energy, when compared to a conventional BWA alternative. The proposed temperature sensor offering digital outputs is simulated to have an overall curvature errors of ±0.21 ^{0}C and 3 σ process variations within ±0.53 ^{0}C, when consuming a total power of 144 µW,within a conversion time of 64 µs (when OSR=128), from 0 to 100 ^{0}C, as shown in the comparison chart in Table I. Compared to previous publications [8]–[11], this design has the minimum area: each temperature sensor takes an area within the image pixel pitch (11 µm ×11 µm) using 0.18 µm CIS technology. It also maintains reasonable FOM and accuracy. The design's layout view is shown in Fig. 9, with both the sensor and its zoom ADC labelled with their dimensions. The decimator filter can be column wise but is off-chip for this tapeout. When quantizing image pixels, the zoom ADC has a column rate of 110 kHz (when OSR=16 and sampling frequency is 2 MHz), which is equivalent to a 100 frame per second (fps) for a 1080p pixel array. Digital dark current compensation using the proposed temperature sensor is expected, as the measured dark current can be modelled exponentially with temperature within an inaccuracy less than 17 %, as shown in Fig. 10, which are measurements results from the authors' previous tapeout.

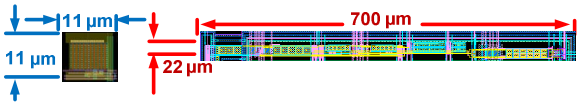


Fig. 9 Layout of the temperature sensor (left) and the zoom ADC (right), not shown in scale.

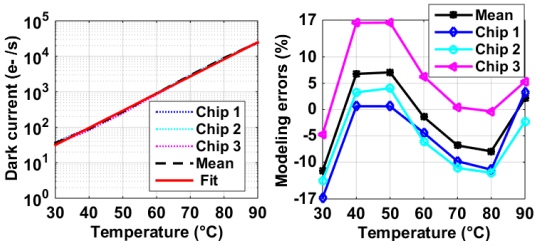


Fig. 10 Measured average dark current for 3 chips and their exponential fit (left) and deviations from the exponential fit (right).

Table I

	This work	[10]	[11]	[8]	[9]
Sensor Type	MOS	MOS	MOS	MOS	MOS
CMOS Technology	0.18 µm	65 nm	0.18 µm	0.18 µm	0.18 µm
Outputs	digital	digital	digital	analog	analog
Area (µm^2)	121	4000	220000	329	177000
Temperature Range (^{0}C)	0 to 100	0 to 100	-20 to 80	-20 to 100	-40 to 125
3 σ accuracy (^{0}C)	±0.53	±2.3	±0.76	±0.21	±2
Power Consumption (µW)	144 (with ADC)	154 (with ADC/TDC)	0.57 (with ADC/TDC)	103 (without ADC)	2000 (without ADC)
Conversion time (ms)	0.064	0.022	8	N/A[b]	N/A[b]
Resolution (^{0}C)	0.125	0.3	0.09	N/A[b]	N/A[b]
Resolution FOM (pJ·K^2)[a]	144	304.9	36.9	N/A[b]	N/A[b]

[a] Energy/Conversion×(Resolution)^2

[b] In these publications, the conversion time, resolution and FOM are unavailable (N/A) as the sensor outputs are analog instead of digital

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