On-Chip Smart Temperature Sensors for Dark Current Compensation in CMOS Image Sensors

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***Abstract*— This paper proposes various types of on-chip smart temperature sensors, intended for thermal compensation of dark current in CMOS image sensors (CIS). It proposes four different architectures of metal–oxide–semiconductor (MOS)-based and bipolar junction transistor (BJT)-based temperature sensors inside and outside the CIS array. Both of the MOS-based temperature sensors make use of the thermal dependence of MOS transistors working in the subthreshold region with ratiometric currents and are quantized by the 14-bit first-order incremental delta–sigma analog-to-digital converters (ADCs). Fabricated using 0.18-μm CIS technology and measured on four chips, the proposed temperature sensors are compared, on their resolution and process variability, as well as on their effects on the neighboring image pixels implemented on the same chip. Experimental results show that the MOS-based temperature sensors inside and outside the array consume a power of 36 and 40 μW, respectively, both achieving 3-sigma (σ) inaccuracy less than ±0.75 °C on four different chips, over a temperature range from −20°C to 80 °C at a conversion time of 16 ms. The temperature sensors facilitate the digital thermal compensation of dark current in the CIS array, by at least 80%, in experiments.**

***Index Terms*— Temperature sensor, CMOS image sensor, dark current, process variability, thermal compensation.**

I. Introduction

IN MODERN VLSIs, most process sensitive parameters are also thermal sensitive [1]. Hence, on-chip temperature sensing for dynamic thermal management has been a popular topic [2]–[6], e.g., on microprocessor chips, due to elevated temperatures caused by the increased power density associated with VLSIs' growing performance demands. Similarly, on a CIS chip, its image pixel array's thermal profile can also rise rapidly due to fast operating digital logics and/or analog-to-digital converters (ADCs) on its edge. The elevated temperature can give rise to increased dark current and dark fixed pattern noise (FPN). However, measures to tackle with the aforementioned thermal problems in CISs have seldom been reported, even in publications on digital compensations of CIS's FPN [7]. Normally, a reference dark frame can be taken immediately before the current frame to cancel out the dark current with a physical shutter, but this is infeasible for low cost or very high speed video applications. In [8], [9], an array of over 500 BJT based temperature sensors are imbedded inside a CIS array, each occupying an area of two image pixels, to sense the temperature locally, although without actually compensating for the dark current. On one hand, the imbedding of the BJTs has caused the dark current and electroluminescence (EL) to increase significantly [9], [10], proportional to the forward-bias current in and the distance to the BJT. Besides, the dark current/EL increases even when the BJTs are turned off, compared with a design without them [9]. On the other hand, the temperature sensors' mean errors are reported to be ±0.5 °C (20∼90 °C, when each chip's averaged outputs are calibrated individually [9]), and 3 σ process variability of ±2.5 °C (±2.5 %, 30∼70 °C [8]), after a one-point calibration, respectively. Similarly, a design using scattered BJT based temperature sensors reports to have 3 σ inaccuracies less than ±0.7 °C on a single chip, over the military temperature range [11].

This paper has three main aims: (1) to look for an alternative that does not increase dark current or EL to its neighboring image pixels, other than BJT based thermal sensing front-ends; (2) to further optimize its accuracy, 3 σ inaccuracy while maintaining calibration efforts, within the scope of thermal compensation for CIS (with accuracy ∼1 °C) and (3) to use the thermal information provided by the suitable on-chip temperature candidates to compensate for the CIS's dark current's thermal dependency. For the first purpose, resistor-based [5], [12], [13] and MOS (or, delay-line) based temperature sensors [14]–[20] are the most popular choices offering reasonable accuracy (<1 °C) beyond the BJT based ones. Considering the available area for the in-pixel temperature sensor–one image pixel area (11 μm× 11 μm), this design favors the MOS based type over the resistor based ones. The design considerations of temperature sensors for CIS thermal compensation are medium accuracy (∼1 °C for 15 % of prediction errors) and minimum (less than 0.1 %) overhead of the total chip area and power (a CIS chip normally measures a few tens millimeter in each dimension and consumes a few tens to a few hundred milli watts). Although implemented for thermal compensation in CIS, the proposed

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work can also serve as a prototype for thermal sensing network [21].

By fulfilling the aforementioned aims, this paper has the following novelties/advantages, compared to previous publications: (i) In-pixel nMOS based temperature sensors implemented in the same array as the image pixels, using a CIS technology. With them, dark current in image pixels have been compensated by 80 % in experiments. (ii) self-referenced MOS temperature sensor with novel sensing front-end and modulator architecture for medium accuracy, using less complicated calibration method. This work uses one delta-sigma analog-to-digital converter (DSADC) instead of a two-stage one (with a successive approximation register, SAR, as the first stage) as in [19]. In this way, the calibration efforts to align the outputs of SAR and delta-sigma ADCs are saved, while maintaining reasonable accuracy (better than 0.7 °C 3 σ inaccuracy for 4 measured dies in this work).

Implemented using 0.18 μm CIS technology, the MOS based temperature sensor outside the array has a 3 σ inaccuracy of $\pm$0.7 °C among 4 chips. The in-pixel nMOS temperature sensor achieves 3 σ inaccuracies within $\pm$0.75 °C. They facilitate digital compensation for the averaged dark current and dark non-uniformities by at least 80 %, with their temperature information. Compared with previous publications on MOS based temperature sensors [16]–[18], the advantage of the proposed temperature sensors are lower FOM (the MOS sensor outside the pixel) and smaller area (the in-pixel ones), with reasonable accuracy. This paper is the first of its kind demonstrating the measurement results of digital dark current compensation using on-chip temperature sensors. It is organized as follows. Section II describes the operating principle of the proposed 4 varieties of smart on-chip temperature sensors. Here, "smart sensors" refer to sensors providing digital outputs with reasonable accuracy despite process variability (e.g. $< \pm 1$°C for intended applications). Section III compares the proposed temperature sensors' mismatches by running Monte Carlo simulations. Section IV shows the experimental results of the 4 proposed temperature sensors' thermal behavior and their effects and compensations on the image sensors implemented on the same chip. Section V concludes this paper.

II. Operating Principles

Fig. 1 shows the system diagram of all the 4 on-chip temperature sensors, which are described as: self-referenced MOS based temperature sensor (type i), self-referenced BJT based temperature sensor (type ii), conventional BJT based temperature sensor (a conventional design only for comparison purpose), in-pixel BJT based temperature sensor (type iii), and in-pixel nMOS based temperature sensor (type iv). All are digitalized by 14 bit delta-sigma ADCs. No correlation is required among the four types of temperature sensors for them to function properly. In other words, they can function independently. They may or may not share their input clocks. However, the in-pixel BJT and MOS (type iii and type iv) share their column and row decoders and their outputs are read out by the same multiplexer. Also on the chip is a reference

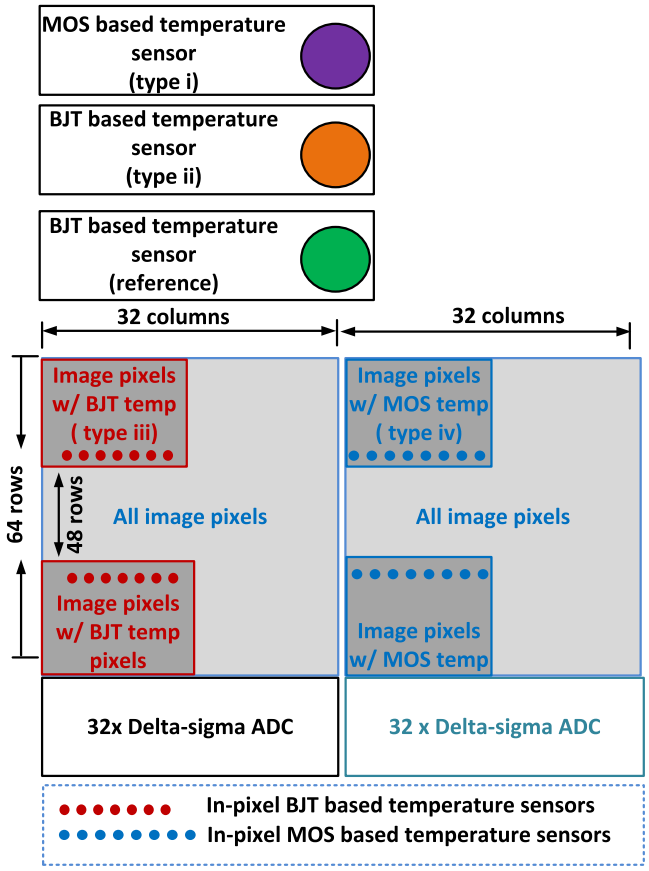

Fig. 1. System diagram of the proposed on-chip temperature sensors. The solid purple, orange and green circles represents the MOS based (type i) and the two BJT based (type ii, iii) temperature sensors outside the image pixel array.

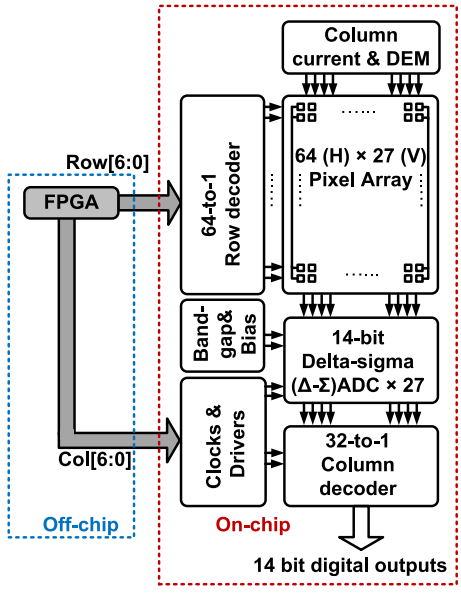

Fig. 2. System block diagram of in-pixel MOS (type iv) temperature sensors.

design without any type number assigned. Fig. 2 shows a more detailed block diagram with input and output I/Os for type iv sensor (in-pixel MOS). It also applies to type iii sensor (in-pixel BJT).

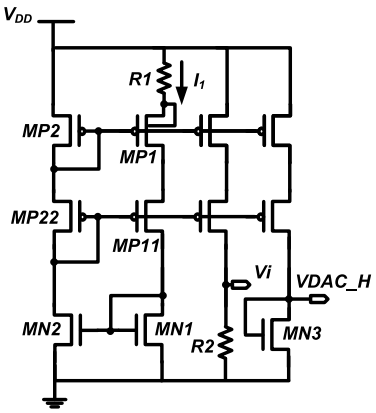

Fig. 3. Schematic of proposed self-referenced MOS based temperature sensor.

A. Self-Referenced CMOS Based Temperature Sensor (Type i)

Fig. 3 shows the schematic of the proposed self-referenced CMOS based temperature sensor. By "self-referenced", the sensor does not need any bandgap reference voltage as reference, neither for the sensor nor for its ADC. Compared to the design published in [19], this design separates the temperature sensing elements (*MP1*∼*2*, *MN1*∼*2* and *R1*) and the voltage conversion elements (*MN3* and *R2*). This is by considering its application in CIS, it can afford a little bit more power, which helps gain some stability as the voltage conversion elements can be subjected to ringing, when they are connected to the back-end switched capacitor circuits (delta-sigma ADCs). Another main difference (from [19]) is that the thermal sensing elements in this design are pMOS transistors operating in subthreshold region instead of the "DTMOS" (a type of dynamic threshold pMOS described in [19]). The output of this design is single-ended, as the target design accuracy (∼1 °C) can be achieved using a single-ended design, which can save chip area, in general. The operating principle of the proposed CMOS based temperature sensor (shown in Fig. 3) is as follows. *MP1*∼*2*, MP*11, 22*, *MN1*∼*2* and *R1* work as in a constant-gm circuit as in [22], except that *MP1* and *MP2* work in subthreshold region:

$$I_1 = I_{DS} \cdot e^{(V_{GS}-V_{TH})/nV_T} \tag{1}$$

where I_1, I_{DS}, V_{GS}, V_{TH}, V_T are the bias currents and saturation currents, gate-source voltages, threshold voltages of the transistor *MP1* and*MP2*, respectively and V_T=*kT/q* (*k* is Boltzmann's constant, q is the electronic charge and T is the temperature), respectively; and n is a process dependent factor. The voltage drop across resistor *R1* is:

$$V_{R1} = n\frac{kT}{q}ln(N) \tag{2}$$

which is proportional to the absolute temperature T (PTAT). N is the ratiometric current ratio in *MP1* and *MP2*, and is 4 in this design. *MN1* and *MN2* are identical while *MP1* is sized 4 times as large as *MP2*. n is a process dependent factor. The PTAT current in the branch of *R1* and *MP1* is mirrored to that of *R2*, which generates a PTAT voltage across *R2*:

$$V_i = n\frac{R2}{R1}\frac{kT}{q}ln(N) \tag{3}$$

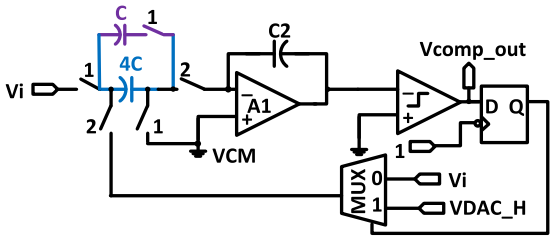

Fig. 4. Schematic of the proposed delta-sigma ADC for digitizing the CMOS based temperature sensors (type i) in this paper. The is an illustrative circuit rather than the exact practical circuit implementation.

R1 and *R2* are poly-resistors with minimum process and temperature variations that are available in the reference design library. Nowadays, resistors have been widely used as accurate temperature sensing devices [5], [12]. However, it is found in our design library that the types of resistors having higher temperature coefficients are subject to larger process variability, which require additional calibration efforts, as mentioned in [13]. *R1* and *R2* are layout next to each other in an inter-digitalized manner. *MN1,2* are actually implemented by cascode devices in this design, as allowed by the power supply level. *VDAC_H* is a CTAT, with negative temperature coefficient, as the *MN3*'s current is PTAT, but its threshold voltage V_{TH3} is CTAT, as for most nMOS transistors [23]. However, *VDAC_H* may not need to be a strict CTAT. More importantly, *VDAC_H*'s voltage level should be higher than *Vi* for the sensor's operating range. Fig. 4 draws the schematic of the proposed discrete time delta-sigma ADC that quantizes the proposed temperature sensor. *Vi* and *VDAC_H* shown in Fig. 3 is connected to *Vi* and *VDAC_H* labeled in Fig. 4 where *C* is approximately 200 fF in this design. This introduction of capacitor C series with phase 1's switch makes it possible to compare *Vi*, which is the sensor's *PTAT* analog outputs, with a *CTAT* voltage *VDAC_H*, thus achieving reasonable resolution, without introducing a zoom ADC as in [19], [24]. The considerations are that although in [19] a zoom ADC adds more resolution, it is basically a two-step ADC, which requires calibration for each (ADC) in general. Besides, in [19] the mismatches among the capacitors in the first-step SAR in the zoom ADC has to be calibrated for each capacitor's weighing. This problem is eliminated in our design, where the output bit stream (*bs*) of Vcomp_out shown in Fig. 4 is:

$$Vi = \frac{4}{5}Vi \cdot (1 - bs) + VDAC\_H \cdot bs \tag{4}$$

where exists only one variable *bs* that can be figured out during bit streaming. Moreover, as *4/5Vi* is close to but always lower than *Vi*, no overflow occurs yet the resolution can be reasonable. According to equation (4), the digital outputs of the sensor are nonlinear. It is true process variability exists between the 5× and 4× of *C* among each individual sensor, but it can be trimmed out by a one-point calibration. Here, the one-point calibration is performed by assigning a gain correction factor to each individual sensor. However, one-point calibration may also be performed by assigning an offset factor to each sensor. The gain and the offset correction cannot be

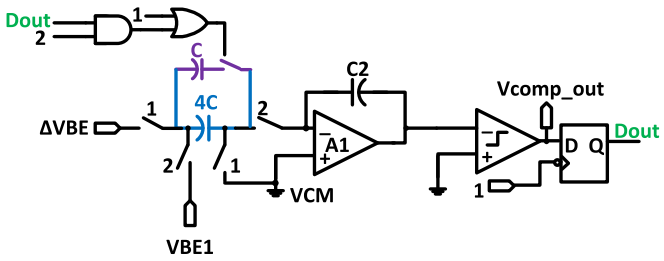

Fig. 5. Schematic of the proposed delta-sigma ADC for digitizing the BJT based temperature sensors (type ii) in this paper.

performed at the same time by a one-point calibration, but can be done by a two-point calibration. The majority of the state-of-the-art temperature sensors calibrate at least at one temperature point, most of the time at two [5], [11], [15], [19].

The non-idealities in the thermal model shown in equation (3) include: mismatches between threshold voltages (if applicable), ratiometric currents and devices sizes of *MP1*∼*2*, *MN1*∼*2* and *R1*∼*2*.

B. Self-Referenced BJT Based Temperature Sensor (Type ii)

The BJT based temperature sensor front-end is in reference to [24]. Its delta-sigma ADC for quantizing the sensor, different from that in [24], is shown in Fig. 5, whose input $\Delta VBE = kT \cdot ln(N)/q = VBE1 - VBE2$ is drawn as single-input but is in fact differential. Its output *bs* represents $5 \cdot \Delta VBE/VBE$, which is always less than unity over the temperature range of interest, -20 ∼80 °C. The renovation in this paper, compared to [24], is the change to the delta-sigma modulator's architecture (the capacitor *C* and the AND and OR gate in Fig. 5), which improves the resolution of the sensor, by, e.g., a factor of 5 in this design, without using a two-step zoom ADC as in [24]. This saves calibration efforts for the two-step zoom ADC while maintaining reasonable resolution in this design.

The delta-sigma ADCs Fig. 4 and Fig. 5 are analogous in their operating principles and architectures, yet their differences are as follows. First, the one in Fig. 4 is single-sided while that in Fig. 5 is differential. Second, to accommodate their separate sensing front-ends, their timing logics are different, which are shown in both figures.

C. In-Pixel BJT Based Temperature Sensor (Type iii)

It is proposed in [25] that a single BJT can be implemented on-chip as a calibration circuit for its temperature sensors, and upon this principle many publications are based [8], [11], as shown in Fig. 6, where the PTAT voltage $\Delta VBE = kT \cdot ln(N)/q$ and $N = 4$ is ensured by dynamic element matching (DEM) in this design. *RS* is the row select switch, which enables the temperature sensor to share the column and row buses with the image pixels. *M0*∼*M4* are in fact implemented by cascode devices as the power supply level allows. Reference [25] explains that the temperature dependence of ΔVBE decreases with temperature, due to reverse early effect. However, in our simulation, the effect has caused linear errors less than ±0.25 °C. This degree of errors is acceptable for the target application of 1 °C. The advantage of using a single transistor for sensing is without the mismatches as in a

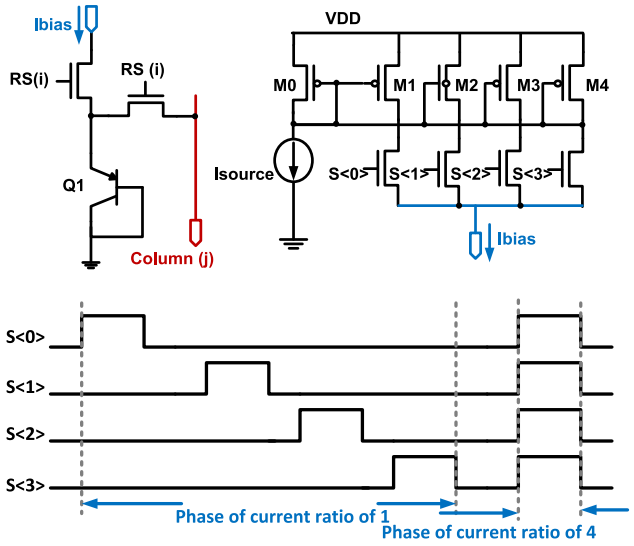

Fig. 6. Top: Schematic of in-pixel BJT based temperature sensor (type iii) and its current biasing with DEM. Bottom: the DEM's timing diagram.

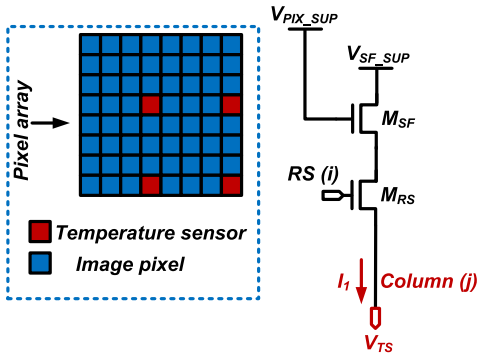

Fig. 7. Schematic of in-pixel nMOS based temperature sensor (type iv) and its layout among the image pixel array. A similar layout among the image pixel array applies to the BJT based alternative.

two transistor sensing pair device. These mismatches may be geometrical or due to saturation current (*Is*). However, *Is* and bias current level still varies from one sensor to another.

D. In-Pixel nMOS Based Temperature Sensor (Type iv)

The in-pixel BJT based temperature sensor has been measured to cause elevated dark current and EL to its neighboring pixels, as will be shown in section IV-D. Therefore, in this paper it is replaced by an nMOS transistor, as shown in Fig. 7. Its operating principle is analogous to that described in section II.II-A of the self-reference MOS based temperature sensor. Its output change during two phases becomes $\Delta V_{TS} = nkT \cdot ln(N)/q$ where $N = 4$ is ensured by a DEM similar to that shown in Fig. 6. *n* is a process dependent factor. V_{PIX_SUP} and V_{SF_SUP} are shared with image pixels [9] implemented in the same array. Their voltage levels depend on the performance requirements of the image pixel and they may or may not be of the same voltage value. In fact, this type *iv* in-pixel nMOS based temperature sensor is reconfigured using the existing 4T Pinned Photodiode (PPD) imager pixel, as shown in Fig. 8. When the imager pixel's *TG* is turned off

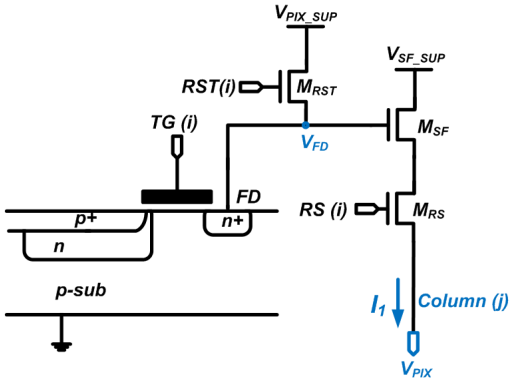

Fig. 8. Schematic of the 4T Pinned Photodiode (PPD) image pixel.

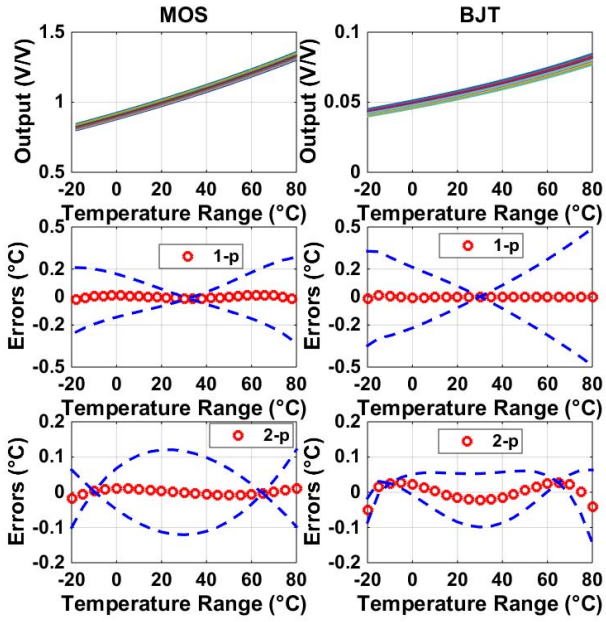

Fig. 9. 100 Monte Carlo simulations of self-referenced temperature sensors, MOS (left, type i) versus BJT (right, type ii), and their temperature errors (red circles) including process variations (blue dashed lines) after a one-point calibration at 30 °C (2nd row) and a 2nd-order master curve fitting, and two-point calibration at -10 and 65 °C. The figure legend "1-p" and "2-p" mean one-point calibration at 30 °C and two-point calibration at -10 and 65 °C.

and when $V_{RST} > V_{PIX\_SUP} + V_{TH}$, it can be seen as the schematic shown in Fig. 7, where V_{TH} is the threshold voltage of the M_{SF}. In this way (of reconfiguring the image pixels for thermal sensing), no additional dead pixels would be incurred and hence the image quality is maintained.

III. Monte Carlo Simulations

In this section, Monte Carlo simulations are performed to help investigate process variability and curvatures for the 4 different types of proposed temperature sensors.

A. Self-Referenced MOS Versus BJT Temperature Sensor-Monte Carlo Simulations

100 Monte Carlo simulations are performed on the self-referenced MOS based and BJT based temperature sensors, as shown in Fig. 9.

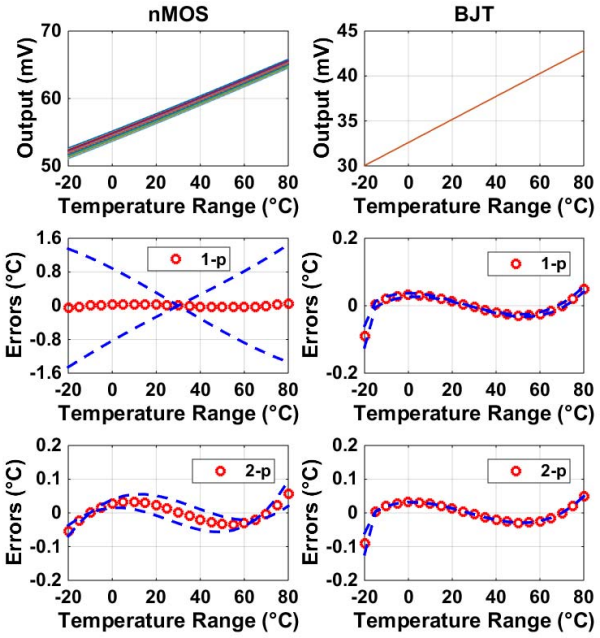

Fig. 10. 100 Monte Carlo simulations of transistor-level in-pixel temperature sensors, nMOS (left, type iv) versus BJT (right, type iii), and their temperature errors (red circles) including process (blue dashed lines) variations after a one-point calibration (2nd row) at 30 °C and a 2nd-order master curve fitting, and two-point calibration at -10 and 65 °C. The figure legend "1-p" and "2-p" mean one-point calibration at 30 °C and two-point calibration at −10 and 65 °C.

For one-point calibration, the calibration point is placed in the middle of the range to minimize errors. For two-point calibration, the choice of the positions of the two temperature points affects the errors, but only to a lesser extent. As having two-points, both gain and offset mismatches can be cancelled.

Before trimming, the MOS based sensors' process variability is 5 %, compared to 6 % for the BJT alternative.

B. In-Pixel nMOS Versus BJT Temperature Sensor-Monte Carlo Simulations

To investigate the process variability and thermal curvatures of in-pixel MOS and BJT based temperature sensors, 100 Monte Carlo simulations are performed using transistor level circuits, supposing DEM can be performed. Both employ cascode current biasing. Fig. 10 shows the simulation results, from which the following observations can be made. First of all, the in-pixel nMOS based temperature sensor (type iv, shown in Fig. 7) has much larger process variability than the BJT based alternative (type iii, shown in Fig. 6), without trimming, when their areas are comparable. The former has an untrimmed 3 σ process variability of 1.6 %, compared to 0.01 % in the latter. Secondly, the process variability of the in-pixel nMOS temperature sensor are nonlinear, or, at least contains a large portion of 2nd-order components, which cannot be trimmed out by calibrating at one temperature point. At last, upon a two-point calibration, the errors of both sensors are comparable. It is speculated that three main sources contribute to the first and the second points mentioned above. The first and second source are the "n" factor in equation (1) and the threshold voltage of M_{SF} shown in Fig. 7 that

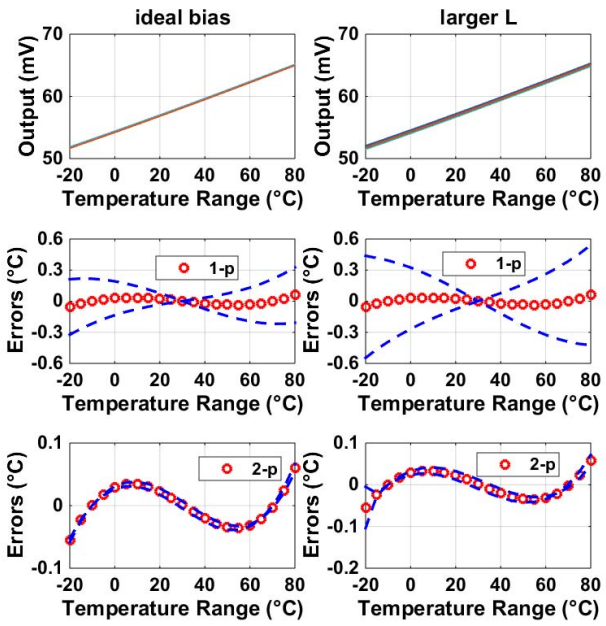

Fig. 11. 100 Monte Carlo simulations of transistor-level in-pixel temperature sensors, both using nMOS, with ideal current bias (left) versus 4 times as larger W and L in its current bias (right) as in Fig. 10, and their temperature errors (red circles) including process variations (blue dashed lines) after a one-point calibration at 30 °C (2nd row) and a 2nd-order master curve fitting, and two-point calibration at -10 and 65 °C. The figure legend "1-p" and "2-p" mean one-point calibration at 30 °C and two-point calibration at −10 and 65 °.

is subject to body effect, which makes the cancellation of V_{TH} in eq. (2) incomplete for the in-pixel MOS sensor. The third one is that an MOS-transistor has a much narrower subthreshold operating region, which is further sharpened by the mismatches in its biasing circuits. By keeping the area of the nMOS based temperature sensor, but increasing length and width of its biasing circuits to both 4 times as large, the 3 σ process variability upon one-point calibration is reduced from 1.6 % to 0.24 %, by a factor of 6, larger than the expected improvement of 4, in theory, as shown in Fig. 11.

This indicates that increasing the sizes of the biasing transistors alone not only helps reduce its own mismatches, but also better defines the in-pixel sensors in its own subthreshold region. Fig. 12 simulates the I-V characteristics for both sensors, showing that the BJT based type has a wider and flatter region that has exponential I-V relationship, which is the basis for linear and lower process variability temperature sensing operation, compared to its nMOS based counterpart.

Compared to the in-pixel ones, without trimming, the larger area self-referenced sensors in this section do not perform better in Monte Carlo simulations, as the in-pixel one has only one device and is less susceptible to geometrical mismatches. This point will be supported with the measurement results shown in section IV.

C. Power Supply Sensitivity

Fig. 13 shows the simulation results of all 4 types of temperature sensors' power supply sensitivity. It indicates that type i and type ii (self-referenced, outside the array) temperature sensors are insensitive to power supply change

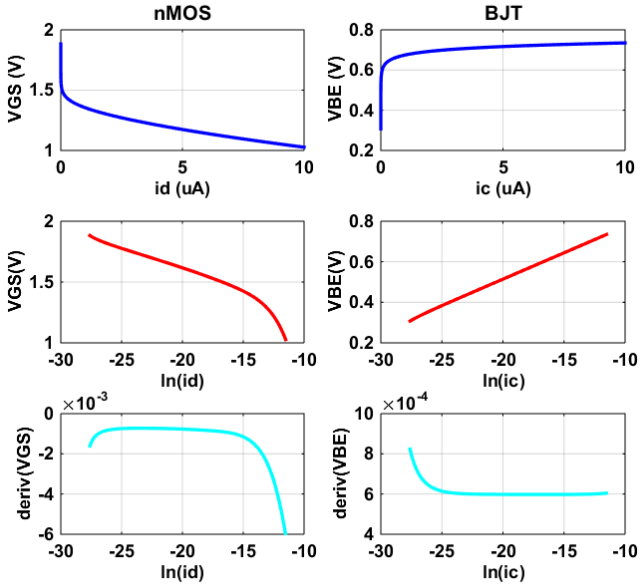

Fig. 12. DC simulations of transistor-level in-pixel temperature sensor, nMOS (left) versus BJT (right), both using ideal current bias, showing their operating region that follows exponential I-V characteristic similar to that in equation (1).

of 10 %, from 3 V to 2.7 V. This can be explained by the fact that their bias circuits are either constant gm circuit (as shown in Fig. 3) or PTAT, whose operations are independent of power supply voltages (which, if not too low to drive the transistors from saturation into triode region). The type iii in-pixel BJT based temperature sensor's dependency on power supply voltage is negligible in terms of the accuracy required in this paper. As its bias is not a PTAT but instead a constant current one whose mirrored current depends slightly on the supply level. In contrast, without trimming, type iv in-pixel MOS based temperature sensor's power supply sensitivity is around 5 °C/V, or ±1.5 °C when power supply drops by 0.3 V, or change by 10 % from 3 V. However, with a two-point calibration that has to be performed for all the sensors in this paper, the type iv sensor (in-pixel MOS)'s power supply sensitivity becomes negligible. This two-point calibration is performed at the same time when removing process variability. The origins of both, the power supply sensitivity and the process variability, are the body effect of the SF M_{SF}, which changes with V_{TS} in Fig. 7, as $V_{TS} = V_{PIX_SUP} - V_{GS}$, $\partial V_{TH}/\partial V_{SB} = \gamma/2\sqrt{(2\Phi_F + V_{SB})}$ (where γ, Φ_F, V_{SB} are body effect constant, Fermi level and source-body voltage of SF). In other words, in change of V_{TH}, or, ΔV_{TH}, is affected by the power supply V_{PIX_SUP} level since $V_{SB} = V_{TS}$ and $V_{TS} = V_{PIX_SUP} - V_{GS}$. If the SF $M'_{SF}s$ body is connected to its source, the drop of V_{PIX_SUP} will have not affected the sensors' outputs, which are differential ones quantized in two different phases. However, this design's fabrication process does not allow the short of source and body in a CMOS, unless the source is grounded.

IV. Measurement Results and Discussions

A prototype has been fabricated using 0.18 μm CIS technology, and the measurement setup is shown in Fig. 14.

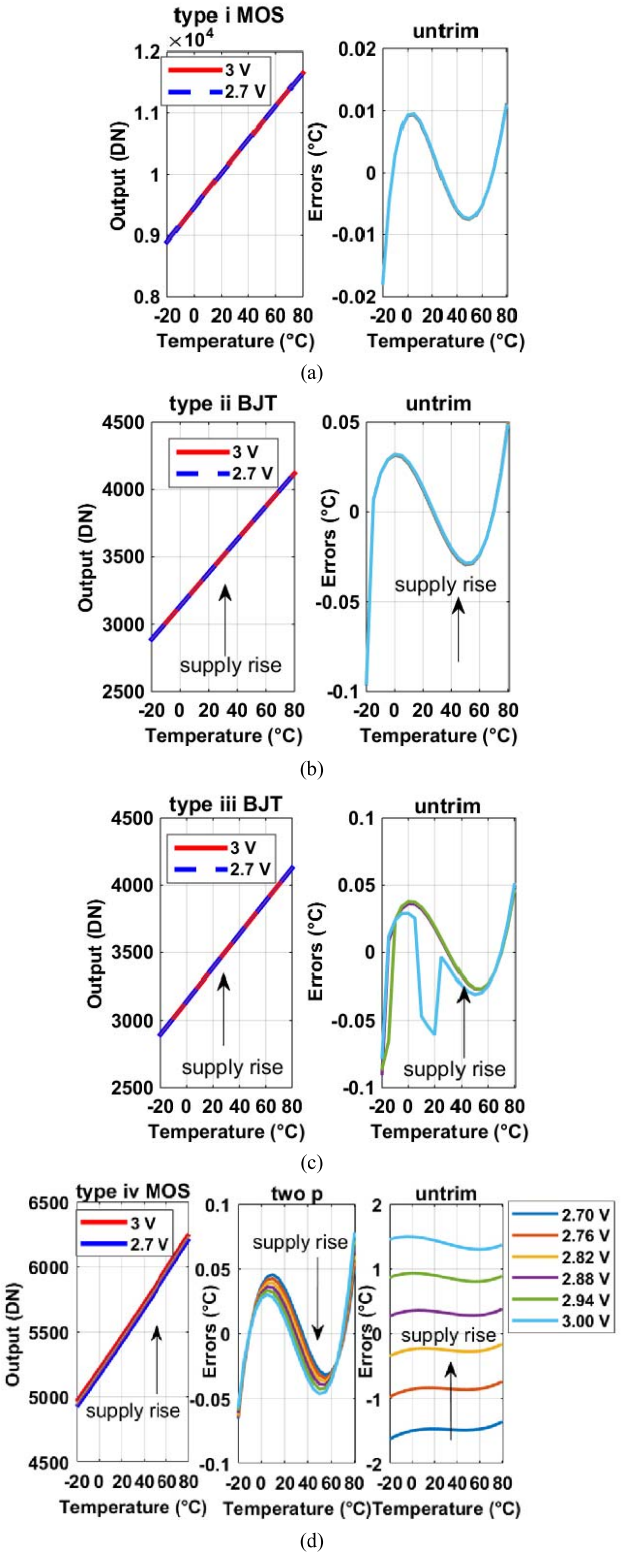

Fig. 13. Transistor-level schematic simulation results of all types (i∼iv) of temperature sensors, when supply voltages change from 2.7 V to 3 V, upon a two-point calibration at -10 and 65 °C, if necessary, and upon a 2nd order global curve fit, and untrimmed. "two p" and "untrim" refer to "two-point calibration" and "untrimmed", respectively.

The camera shown is placed on the top of the test chip to capture images. Input signals are generated in the ALTERA FPGA in the left-side mother board using Quartus II software.

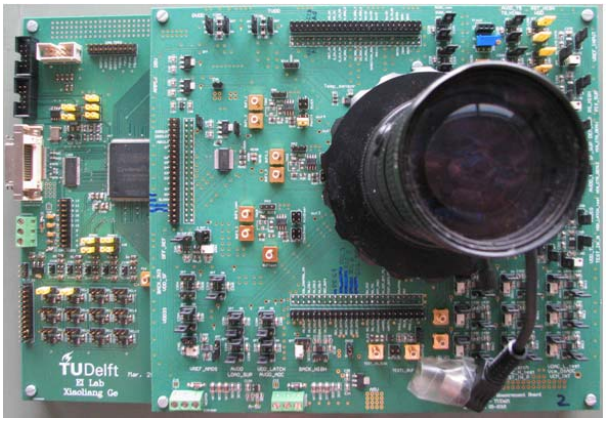

Fig. 14. Measurement setup of the prototype.

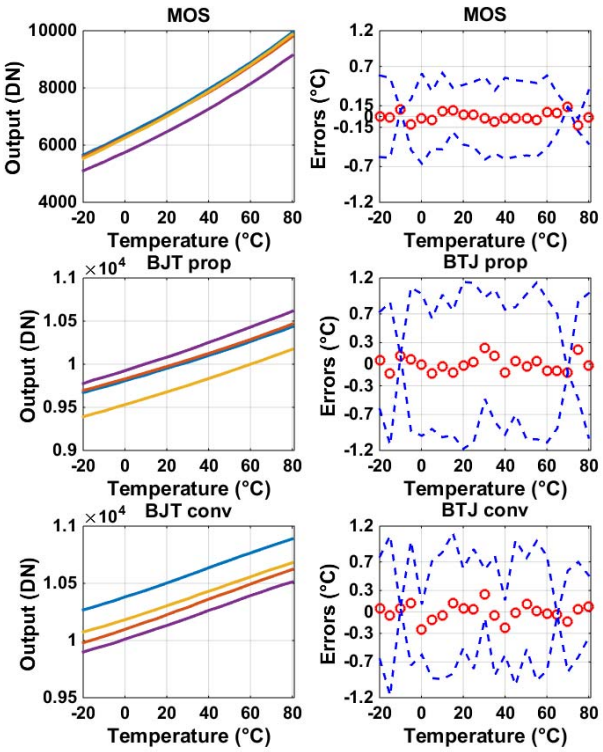

Fig. 15. Measurement results from 4 chips of the self-referenced temperature sensors, proposed MOS (1st row, type i) and BJT (2nd row, type ii), versus a conventional design (3rd row, type iii), and their temperature curvature errors (red circles) including process variability (blue dashed lines), after a two-point calibration at -10 and 65 °C and a 2nd-order master curve fitting.

The temperature measurement has been performed using a temperature chamber. The reference temperature is from a Pt100 thermometer, in physical contact with an aluminum box and the PCB under test. Our chip under test is in close contact with the aluminum box. The Pt100 temperature sensor reference is trimmed to have accuracy better than 0.02 °C. The conversion time for all temperature sensors is 16 ms, or, their sampling frequencies are all 62.5 Hz. The image capture was performed using Cameralink and Labview.

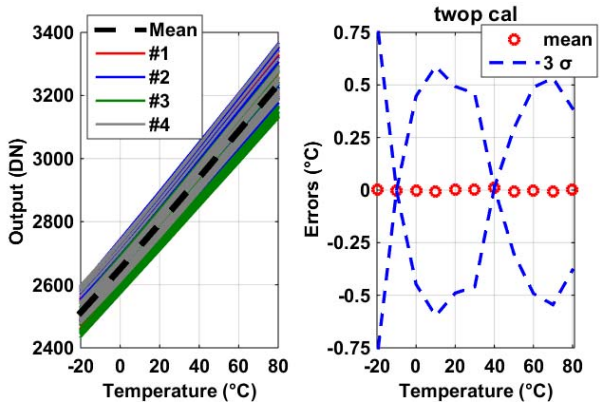

Fig. 16. Measurement results of the in-pixel MOS based sensors (type iii), against a 2nd-order master curve fitting, and after a two-point calibration at −10 and 40°C.

A. Self-Referenced nMOS (Type i) Versus BJT (Type ii) Temperature Sensor

The self-referenced MOS and BJT based temperature sensor are measured for 4 chips, as shown in Fig. 15, from which the following observations can be made. First of all, the untrimmed 3 σ process variability for the three types (i, ii and the reference design) of temperature sensors are 4.1 %, 4.8 % and 4.6 %, respectively. However, looking at Fig. 15, it seems that the process variability in the top row (type i) are much lower than those in the other two, being ±0.7 °C (type i) versus ±1.2 °C (type ii). This could be explained as follows. The resolutions of the three types are 0.025 °C, 0.125 °C and 0.15 °C, respectively. Therefore, the 3 σ process variability of the MOS based temperature sensor translates to less temperature errors (for the same amount of process variability), compared to the other two, which are ±0.7 °C for the MOS and ±1.2 °C for the two BJT counterparts. Secondly, the fact that the resolution of the MOS based one is finer corresponds to that in simulations (Fig. 9). Type i and ii's sensing devices' thermal coefficients are similar, both around 120 μV/°C, although the former is a bit larger due to the "n" coefficients shown in equation (1), to be 130 μV/°C.

However, due to the multiplication shown in equation (3), the output voltage Vi can be much closer to $1/5V_{TH}$ than that of ΔV_{BE} to $1/5V_{BE}$, at the highest temperature point of interest. It is true $1/5V_{BE}$ can be reduced to $1/10V_{BE}$, or $1/X \cdot V_{BE}(X$ can be a number from 1 to 10). However, ΔV_{BE} is a PTAT voltage while V_{BE} is a CTAT voltage sensitive to its current and one has to make sure that $1/X \cdot V_{BE}$ is larger than ΔV_{BE} over the temperature range of interest. Finally, the two BJT based temperature sensors, type ii and the conventional reference design show similar curvature and process variability.

B. In-Pixel nMOS (type iv) Versus BJT Temperature Sensor (Type iii)

Fabricated using 0.18 μm CIS technology, 27 in-pixel nMOS based temperature sensors based on the schematic shown in Fig. 7 (quantized by 1st-order delta sigma ADC

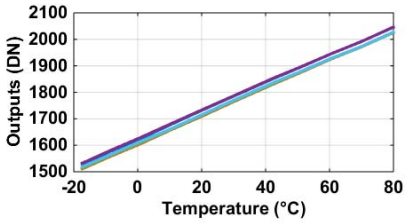

Fig. 17. Measurement results of the 6 in-pixel BJT based sensors (type iii), without DEM.

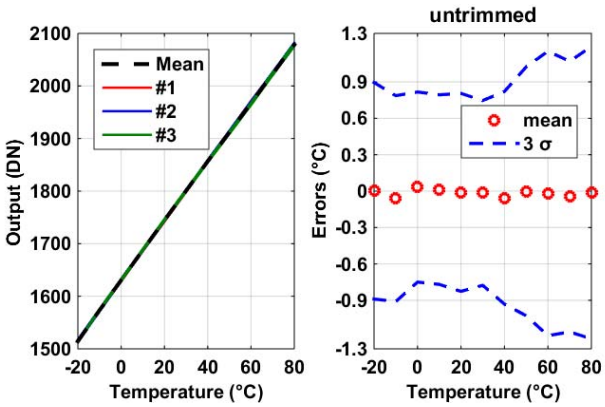

Fig. 18. Measurement results of the in-pixel BJT based sensors (type iii), after a 2nd-order master curve fitting, without trimming, with DEM.

(f_s = 2 MHz)) are measured to have untrimmed 3 σ process variability of ±3.8 % between -20 and 80 °C, on the same chip, for 4 chips, as shown in Fig. 16. As they are readout by delta-sigma ADCs, which are equipped with feedback loop to ensure the ADCs' digital outputs represent the analog input, the above mentioned process variability are all attributed to the sensor front-ends. Besides, DEMs are already employed. The measured thermal curvature and 3 σ inaccuracy after a two-point calibration at -10 and 40°C and a 2nd-order master curve fitting, are within ±0.75 °C.

Measurements are also performed on 6 in-pixel BJT based temperature sensors on the same chip, for 3 chips. Without DEM, they show 3 σ process variability of ±1.8 %, as shown in Fig. 17. With the help of DEM, their measured untrimmed 3 σ process variability are reduced to be less than 0.25 %, as shown in Fig. 18.

In the following aspects, the measurement results in this section correspond well to the Monte Carlo simulation results shown in section III. (1) The untrimmed 3 σ process invariability of in-pixel BJT (type iii) sensors are less than that of the in-pixel MOS (type iv), that of which are less than the type i, and then type ii which are outside the array; (2) The type i sensors' 3 σ inaccuracy is better than that of type ii and it is comparable to that of type iii and iv, for simulation results upon one-point calibration and measurement results upon two-point calibration.

What is different between the measured and the simulations is that the 3 σ inaccuracies are larger during measurements, upon a 2-point calibration, for all sensors. The explanations are that non-idealities such as noise, capacitor cross coupling

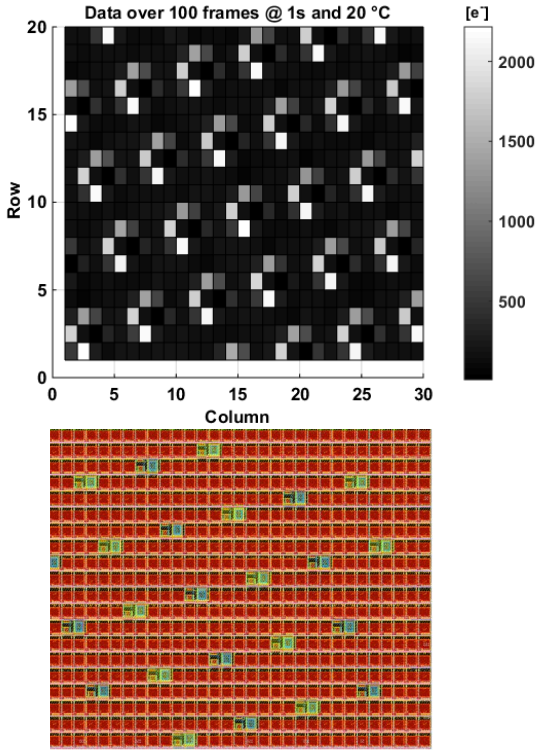

Fig. 19. Top: The incorporated BJT based temperature sensors (the darkest ones taking the size of two pixels, in the center of the brighter ones) shown in the figure incur dark current to its neighboring image pixels (brighter/whiter cells) in [9]. Bottom: the locations of the sensors relative to the image pixels in [9]. Those yellow and blue pixels taking two cells each are the temperature sensors, corresponding to the darkest ones in the top graph. The rest in red are image pixels.

and systematic offset give rise to higher order of variations that cannot be removed by calibrating at one point, for each sensor.

C. Self-Referenced (Type i, ii) Versus In-Pixel (Type iii, iv) Sensors

On one hand, compared to the in-pixel temperature sensors (type iii and iv), the proposed sensors outside the array (type i and ii) show larger 3 σ process variability, both in simulation and in measurements, before trimming. The larger untrimmed 3 σ process variability in type i and type ii outside the array is due to the sensing front-ends are from two sensing devices, compared to a single device used in the in-pixel alternatives (type iii and iv). Upon trimming, type i (MOS) shows comparable 3 σ inaccuracy as type iii and iv. The noise is measured to be around 0.09 °C for all temperature sensors. The advantage of the self-referenced temperature sensors, type i and ii, is the elimination of an external reference. This saves chip area and power and ensures thermal coefficient. However, for CIS, there is always a reference circuit implemented on-chip. This compromises benefit of the area and power saving of the self-referenced ones, but does not guarantee the thermal coefficient for the in-pixel sensors as the available on-chip reference voltage can be slightly thermal curved.

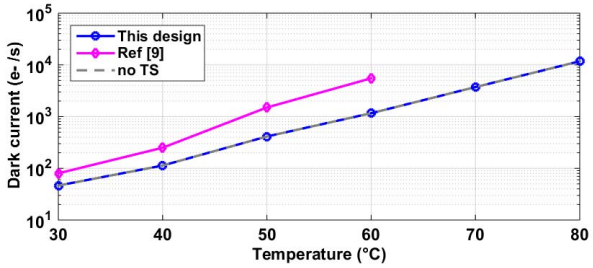

Fig. 20. Dark current measured for this prototype CIS imbedded with nMOS based temperature sensors (v), and for [9] incorporated with BJT based temperature sensors, compared to a reference design without temperature sensor ("no TS").

D. Temperature Sensors Imbedded Into an Image Sensor: The Choice Between MOS and BJT Temperature Sensors

Following the statement in [20], as the role of thermal sensing is auxiliary; the temperature sensors should incur minimum effects to the main circuitry and its function, which, on an image sensor chip, is image sensing. Unfortunately, the BJT based temperature sensors are demonstrated to incur EL (similar to a forward biased light emitting diode) to their neighboring image pixels, during their operation, proportional to their forward biased current level and distance to the pixels [10]. Furthermore, our experiments confirmed that they introduce dark current/EL into the image pixels even when they are turned off [9], as shown in Fig. 19, where BJT temperature sensors are incorporated with a density of 1:22 to the image pixels. "dark current" means current generated in the reverse biased photodiode of the image pixels in dark, and it is undesirable since it incurs signal offset to each pixel, as a dark signal and spatial FPN, it limits the dynamic range of the image sensor. In contrast to its name, dark current shows itself as brighter/whiter pixels when a frame is taken in dark. For example, in Fig. 19, the neighboring image pixels of the BJT based temperature sensors (shown as the darkest ones taking the area of two image pixels) are a lot brighter than those image pixels located a little further away.

Fig. 20 shows the dark current measured for a CIS imbedded with on-chip nMOS based in-pixel temperature sensors (type iv) and BJT based alternative ([9], 1 BJT temperature sensor for every 22 image pixels), along with a reference array. It indicates that this prototype with in-pixel nMOS temperature sensors has incurred no additional dark current, compared to the reference design of an all image sensor array. In contrast, the design in [9] with in-pixel BJTs has incurred 3 times more (average) dark current to the image array that they are embedded into.

The in-pixel nMOS based temperature sensors have at least one more advantage over its BJT alternative. When speculating Fig. 6 and Fig. 7, one may find that the current biasing for nMOS is going away from the device (a current sink), while in contrast, that for BJT is going toward the device (a current source). However, as the image pixels are read out through an nMOS source follower, the former shares the biasing circuits with the image pixels and can be read out together with minimum additional biasing circuit hardware and readout time.

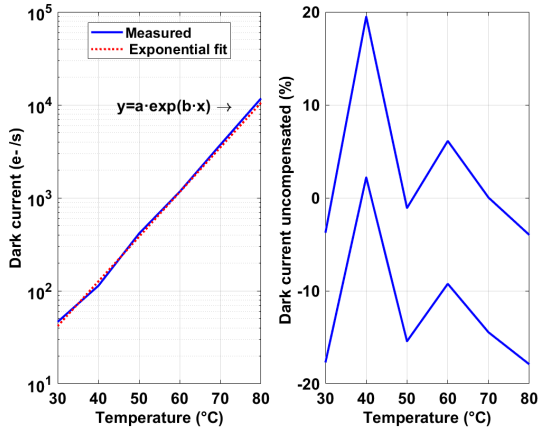

Fig. 21. Measured average dark current for this prototype CIS and remaining dark current uncompensated (errors) after digital compensation using the proposed MOS based temperature sensors (type iris).

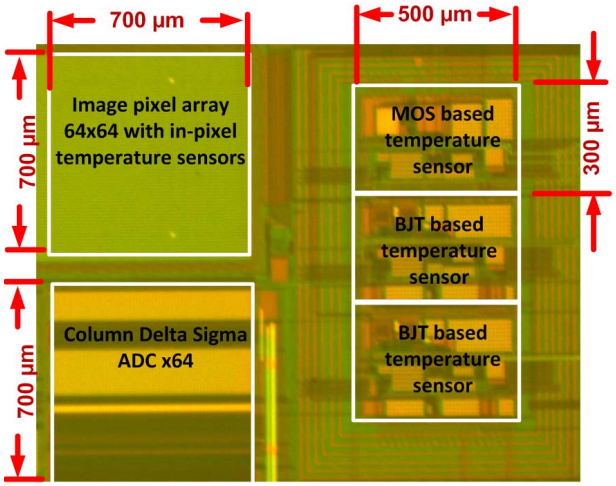

Fig. 22. Part of the micrograph of the prototype with each block labeled.

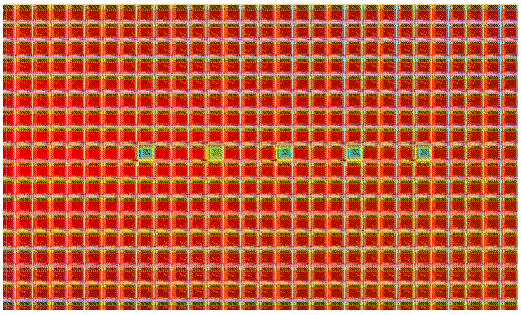

Fig. 23. Part of the layout view of the image pixels (red) with imbedded temperature sensor pixels (green). Both sensors have an area of 11 μm×11 μm for each pixel.

Fig. 24. An image taken by the part of the prototype 64×27 CIS.

TABLE I
SUMMARY OF IMAGE PIXEL PERFORMANCES

Parameters	This image sensor
Process	0.18 µm CIS 1P4M
Pixel Pitch	11 µm ×11 µm
Array Size	64 ×64
Conversion Gain	78 µV/e$^-$
Fill Factor	52 %
Supply voltage	3.3 V
Dark current @ 25 ^{0}C	30 e$^-$/s

E. On-Chip Smart Temperature Sensors for Dark Current Compensation

Dark currents are measured and digitally compensated using the temperature information provided by the proposed on-chip MOS based smart temperature sensors, type i and iv, as shown in Fig. 21. It can be observed in Fig. 15 that using the self-reference temperature sensor (type i) whose 3 σ inaccuracy is within $\pm$0.7 °C including its chip-to-chip process variability, the average dark current can be digitally corrected by up to 80 % (worst case). As dark current shows itself as brighter spots (areas) added to the original image, the reduction of 80 % of dark current means the final image will be 80 % less bright and 80 % closer to the original image (without any dark current).

A micrograph of the fabricated chip and an image taken by the image sensor are shown in Fig. 22 and Fig. 23, respectively. In Fig. 22, the three 500 μm × 300 μm blocks on the right side (from top to bottom) are: type i (self-referenced MOS based temperature sensor, outside the pixel array), type ii (self-referenced BJT based temperature sensor, outside the pixel array), and a conventional design only for comparison purpose. The in-pixel temperature sensor, each taking an area of 11 μm × 11 μm (type iii and iv), is imbedded inside the array, which is 700 μm× 700 μm, in Fig. 22. Fig. 23 shows a layout view of the image sensors with imbedded temperature pixels, each has an area of 11 μm × 11 μm.

Table I shows a summary of image pixel performances. The image pixel schematic was shown in Fig. 8.

V. CONCLUSIONS

This paper proposes 4 different types of on-chip smart temperatures for dark current's thermal compensation: (1) type i, self-referenced MOS based; (2) type ii, self-referenced BJT based; (3) type iii, in-pixel BJT and (4) type (iv) in-pixel nMOS based. Also implemented on-chip is a conventional design only for comparison purpose. They are all implemented on the same chip fabricated using 0.18 μm CIS technology and 4 chips are measured.

First of all, between the self-referenced MOS based (type i) and BJT based (type ii) in this paper, the former are measured to have lower curvature and process variability, and hence,

TABLE II
COMPARISON WITH THE STATE-OF-THE-ART TEMPERATURE SENSORS

	This work (type i)	This work (type ii)	This work (type iii)	This work (type iv)	[16]	[17]	[18]
Sensor Type	MOS	BJT	BJT	MOS	MOS	MOS	MOS
CMOS Technology	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	28 nm	90 nm
Area (μm^2)	(400 ×350) 141250	(350 ×350) 116250	(11 ×11) 121	(11 ×11) 121	89000	1000	74 slices
Temperature Range	-20 ^{0}C to 80 ^{0}C	-20 ^{0}C to 80 ^{0}C	-40 ^{0}C to 60 ^{0}C	-20 ^{0}C to 80 ^{0}C	-20 ^{0}C to 80 ^{0}C	-5 ^{0}C to 85 ^{0}C	-20 ^{0}C to 100 ^{0}C
3 σ accuracy	±0.7 ^{0}C	±1.2 ^{0}C	-0.9/1.1 ^{0}C	±1.2 ^{0}C	±1 ^{0}C	-3.3/1.9 ^{0}C	-0.7/1.1 ^{0}C
Calibration	Two-point	Two-point	Two-point	Two-point	Two-point	One-point	One-point
Power Consumption (μW)	40	40	36	36	0.8	56	90
Conversion Time (ms)	16	16	16	16	800	0.036	1
Resolution (^{0}C)	0.025	0.125	0.1	0.09	0.09	0.76	0.05
Resolution FOM ($nJ \cdot K^2$)[a]	0.4	10	5.7	4.6	5.3	1.2	0.23
Rel.IA (%)[b]	1.4	2.4	2	2.4	2	5.8	1.5

[a] Energy/Conversion×(Resolution)^2, in reference to [29], [b] 3 σ accuracy /temperature range, in reference to [29]

better accuracy. This advantage corresponds with their Monte Carlo simulations using one-point calibration. As explained in IV-A, the reasons are larger thermal coefficient in proportion to its self-referenced voltage in the former, compared to the BJT alternative.

Secondly, for on-chip thermal sensing and compensation for CIS, either inside or outside the CIS array, the nMOS based temperature sensors are better choices, compared to the BJT based alternatives, which can incur significant (up to 3 times) dark current with a BJT density of 1: 22 to the imagers, as shown in section IV-D. The former also has less design complexity in its biasing circuits when located inside the image sensor array.

Thirdly, using the thermal information provided by the proposed MOS based smart temperature sensors, type i and iv, the average dark current of the prototype CIS is compensated by 80 % at least.

Fourthly, based on the discussions from the above 3 paragraphs, the solution to on-chip thermal compensation for dark current for CIS is to use either in-pixel nMOS based temperature sensors or a MOS temperature sensor outside the image pixel array. When the pixel array is larger and consumes larger power, the in-pixel temperature sensors are better options over their counterparts outside the CIS array, as the thermal gradients may increase thereafter. On the other hand, when the pixel array is smaller or consumes less power, it is always possible to predict the thermal profile of a CIS array, using one or a few accurate on-chip temperature sensor's outputs (may be located next to the hotspots, outside the array) and information including its static power consumption, thermal resistance. When thermal resistance or capacitance cannot be found in the datasheets provided by sensor vendors, it could be extracted and employed to predict the chips' (VLSIs and CISs) thermal profile [27], [28] dynamically and spatially.

Fifthly, the trade-offs of incorporating temperature sensors into a CIS array are as follows. The number of in-pixel temperature sensors required for dark current compensation depends on the thermal gradients across the array and the compensation requirements of the dark current. For instance, for a 300 mW CIS array, the thermal gradient can be no more than 0.1 °C/mm [6]. Therefore, for a pixel pitch of, e.g., 10 μm, and for the aforementioned thermal gradients of 0.1 °C/mm, one temperature sensor among every 100 columns/rows would suffice. This makes the spatial density of the in-pixel temperature sensors around 0.01 %, which is the trade-off, both in area and in power, for incorporating temperature sensors inside a CIS array for dark current compensation.

The last but not the least, the proposed temperature sensors are compared to those in publications, as shown in Table II, which shows that the advantage of the proposed self-referenced MOS based temperature is its lower FOM (The FOM is defined in reference to [29]) and better relative accuracy while that of the in-pixel nMOS temperature is its smaller silicon area, when maintaining comparable accuracy. Although implemented for thermal compensation in a CIS, they could also be seen as a prototype for thermal management/compensation in many other VLSI platforms, e.g., microprocessors or other types of sensors, whose performances may migrate or degrade with elevated temperature or temperature gradients. On VLSI platforms other than CIS, BJT based temperature sensors may as well be a good or even better choice due to their better untrimmed accuracy.

ACKNOWLEDGEMENT

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REFERENCES

[1] S. Shah, H. Toreyin, J. Hasler, and A. Natarajan, "Temperature sensitivity and compensation on a reconfigurable platform," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 3, pp. 604–607, Mar. 2018.

[2] R. McGowen *et al.*, "Power and temperature control on a 90-nm Itanium family processor," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 229–237, Jan. 2006.

[3] H. Lakdawala, Y. W. Li, A. Raychowdhury, G. Taylor, and K. Soumyanath, "A 1.05 V 1.6 mW, 0.45°C 3σ resolution $\Sigma\Delta$ based temperature sensor with parasitic resistance compensation in 32 nm digital CMOS process," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3621–3630, Dec. 2009.

[4] J. S. Shor and K. Luria, "Miniaturized BJT-based thermal sensor for microprocessors in 32- and 22-nm technologies," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2860–2867, Nov. 2013.

[5] X. Tang, W. T. Ng, and K.-P. Pun, "A resistor-based sub-1-V CMOS smart temperature sensor for VLSI thermal management," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 9, pp. 1651–1660, Sep. 2015.

[6] S. Xie and W. T. Ng, "An all-digital self-calibrated delay-line based temperature sensor for VLSI thermal sensing and management," *Integr., VLSI J.*, vol. 51, pp. 107–117, Sep. 2015.

[7] J. M. Margarit *et al.*, "A 2 kfps Sub-μW/Pix uncooled-PbSe digital imager with 10 bit DR adjustment and FPN correction for high-speed and low-cost MWIR applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2394–2405, Sep. 2015.

[8] S. Xie, A. Abarca, J. Markenhof, X. Ge, and A. Theuwissen, "Analysis and calibration of process variations for an array of temperature sensors," in *Proc. IEEE Sensors*, Oct./Nov. 2017, pp. 1–3.

[9] A. Abarca, S. Xie, J. Markenhof, and A. Theuwissen, "Integration of 555 temperature sensors into a 64 × 192 CMOS image sensor," *Sens. Actuators A, Phys.*, vol. 282, pp. 243–250, Oct. 2018.

[10] K. Seo, S. Lee, P. Ahn, D. Kim, and K. Cho, "A study on photon effect to image plane," in *Proc. Int. Image Sens. Workshop*, 2017, p. 31. [Online]. Available: http://www.imagesensors.org/Past%20Workshops/2017%20Workshop/2017%20Papers/P31.pdf

[11] B. Vosooghi, L. Lu, and C. Li, "5 × 5 scattered temperature sensor front-end based on single-doide with non-trimmed ±0.7°C 3σ relative inaccuracy," *Electron. Lett.*, vol. 50, no. 24, pp. 1806–1808, Nov. 2014.

[12] S. Pan and K. A. A. Makinwa, "A 0.25mm^2 resistor-based temperature sensor with an inaccuracy of 0.12 °C (3σ) from-55 °C to 125 °C and a resolution FOM of 32fJK^2," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3347–3355, Dec. 2018.

[13] C.-H. Weng, C.-K. Wu, and T.-H. Lin, "A CMOS thermistor-embedded continuous-time delta-sigma temperature sensor with a resolution FoM of 0.65 pJ°C^2," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2491–2500, Nov. 2015.

[14] T. Anand, K. A. A. Makinwa, and P. K. Hanumolu, "A self-referenced VCO-based temperature sensor with 0.034 °C/mV supply sensitivity in 65 nm CMOS," in *Proc. Symp. VLSI Circuits (VLSI Circuits)*, Jun. 2015, pp. C200–C201.

[15] K. Yang *et al.*, "9.2 A 0.6nJ-0.22/+0.19°C inaccuracy temperature sensor using exponential subthreshold oscillation dependence," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 160–161.

[16] W. Song, J. Lee, N. Cho, and J. Burm, "An ultralow power time-domain temperature sensor with time-domain delta-sigma TDC," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 10, pp. 1117–1121, Oct. 2017.

[17] M. Cochet *et al.*, "A 225 μm^2 probe single-point calibration digital temperature sensor using body-bias adjustment in 28 nm FD-SOI CMOS," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 1, pp. 14–17, Jan. 2018.

[18] C.-C. Chen, C.-L. Chen, Y. Lin, and S.-Q. You, "An all-digital time-domain smart temperature sensor with a cost-efficient curvature correction," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 1, pp. 29–36, Jan. 2019.

[19] K. Souri, Y. Chae, F. Thus, and K. Makinwa, "12.7 A 0.85V 600nW all-CMOS temperature sensor with an inaccuracy of ±0.4 °C (3σ) from −40 to 125 °C," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2014, pp. 222–223.

[20] D. Ha *et al.*, "Time-domain CMOS temperature sensors with dual delay-locked loops for microprocessor thermal monitoring," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 9, pp. 1590–1601, Sep. 2012.

[21] S. Paek, W. Shin, J. Lee, H.-E. Kim, J.-S. Park, and L.-S. Kim, "Hybrid temperature sensor network for area-efficient on-chip thermal map sensing," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 610–618, Feb. 2015.

[22] T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*. Hoboken, NJ, USA: Wiley, 2012.

[23] S. Xie and W. T. Ng, "A low power all-digital self-calibrated temperature sensor using 65 nm FPGAs," *Proc. IEEE Int. Symp. Circuits Syst.*, May 2013, pp. 2617–2620.

[24] K. Souri, Y. Chae, and K. Makinwa, "A CMOS temperature sensor with a voltage-calibrated inaccuracy of ± 0.15° C (3σ) From −55 °C to 125 °C," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 208–210.

[25] A. P. M. Pertijs and J. H. Huijsing, *Precision Temperature Sensors in CMOS Technology*. Dordrecht, The Netherlands, Springer, 2006.

[26] S. Xie, A. A. Prouza, and A. Theuwissen, "A CMOS-imager-pixel-based temperature sensor for dark current compensation," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, to be published.

[27] R. Cochran, "Techniques for adaptive power and thermal sensing and management of multi-core processors," Ph.D. dissertation, Dept. Elect./Comput. Eng., Brown Univ., Providence, RI, USA, 2008.

[28] S. Xie and W. T. Ng, "Delay-line temperature sensors and VLSI thermal management demonstrated on a 60 nm FPGA," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Jun. 2014, pp. 2571–2574.

[29] K. Makinwa. *Smart Temperature Sensor Survey*. Accessed: Nov. 1, 2018. [Online]. Available: https://ei.tudelft.nl/smart_temperature

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