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Suppression of spatial and temporal noise in a CMOS image sensor

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***Abstract*—This paper presents methodologies for suppressing the spatial and the temporal noise in a CMOS image sensor (CIS). First of all, it demonstrates by using a longer-length column bias transistor, both the fixed pattern noise (FPN) and temporal noise can be suppressed. Meantime, it employs column-level oversampling delta-sigma ADCs to suppress temporal noise as well as to facilitate the realization of the thermal compensation of dark signal non-uniformity (DSNU). In addition, the image pixels are re-configured as temperature sensors with inaccuracies within ±0.65 ºC, between -20 and 80 ºC. If the dark current and its non-uniformities are caused by thermal gradients, the obtained in-pixel thermal information can be employed to compensate for the measured dark current by 95 % and DSNU, up to 13 %. All the column-level 13 bit 2nd-order incremental delta-sigma ADCs are measured with SNR around 65 dB and INL around 1.5 LSB, when tested with a -8 dB input signal and sampling at 2 MHz with an oversampling ratio (OSR) of 128, when the full scale voltage is 2 Vp-p. The 4T Pinned Photodiode (PPD) CIS is measured to have a temporal noise of 34 μV rms (with an OSR of 128, or, an input referred temporal noise of 0.5 e^- rms, with a conversion gain, CG, of 73 μV/ e^-), a column gain FPN of 0.06 %, a dynamic range (DR) of 92 dB (with OSR=512), as well as a linearity of 1 %. It has a measured DSNU of 3.2 %, after the thermal compensation using the in-pixel temperature sensors, a dark current of 290 pA/cm^2 and 15 pA/cm^2, measured at 60 ºC, before and after the thermal compensation, respectively.**

***Index Terms*—CMOS image sensor, dark current, DSNU, delta-sigma ADC, temperature sensor, thermal compensation**

I. Introduction

FPN caused by non-uniformities among a CIS array deteriorates the image quality. It originates from device mismatches and dark current non-uniformities. In general, offset mismatches among pixels can be compensated using correlated double sampling (CDS). The gain mismatches can be compensated by adjusting each pixel or each column's gain [1].

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Previously, significant improvement in FPN has been reported using digital CDS and column-level incremental delta-sigma ADC in [2]. On the other hand, dark current and DSNU are, to a large extent, affected by the electron-hole pair generations within the image pixel device. As dark current is positively correlated with the intrinsic carrier concentration n_i, which doubles every 11 ºC, thermal gradients among a CIS array also add to dark current non-uniformities. Previously, reference [3] reduces the dark current by optimizing the pixel architecture. In [5], the CIS pixels are reconfigured for thermal sensing to compensate dark current and DSNU. Compared to the aforementioned publications [1]–[5], the highlights of this paper is as follows: (1) Suppression of the temporal noise that is measured along with the dark FPN (DSNU) using column-level 2nd-order oversampling ADCs. (2) Lower DSNU is achieved by using a longer-length current bias transistor in the column circuitry. (3) The DSNU component that is caused by thermal gradients is suppressed using the information generated by the in-pixel temperature sensors, which are designed for less process variability and hence provide a 3σ inaccuracy of ±2.2 ºC by calibrating at room temperature. The improvement of the proposed temperature sensors' accuracy with less trimming points (one point) is through using a longer bias-current-source device length. (4) The CIS is measured a temporal noise of 34 μV rms, with a CG of 73 μV/e^- and an OSR of 128. It has a measured gain column FPN of 0.06 %, a DR of 92 dB and a non-linearity of 1 %. To explain the aforementioned (1): In principle, DSNU is a FPN that cannot be altered by oversampling, which is a noise reduction technique. However, when the images are not averaged over a very large number of frames, e.g., the temporal noise is measured along with the DSNU. Particularly, compared to our previous work in [5], this paper further reduces DSNU and the process variability among the in-pixel temperature sensors through: (i) longer-length current bias devices while keeping its pixel design unchanged and (ii) higher order of incremental delta-sigma modulators.

This paper is organized as follows. Section II explains the operating principles of the CIS array: the 4T PPD image pixel and its column-level biasing circuits, whose influence on FPN is also discussed. Monte Carlo simulations about FPN are reported in Section III. An analysis of the measured DSNU plus temporal noise is given in IV. Section V and VI show the proposed the 2nd order incremental delta-sigma ADCs' circuit schematic and measurement results, respectively. Section VII shows measurement results of the CIS's temporal noise, FPN, dark current and DSNU, using the proposed incremental

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delta-sigma ADCs and, along with the thermal compensation methods. Section VIII concludes this work.

II. 4T PPD CIS Array

A. Pixel Architecture and Operating Principle

Fig. 1 shows a block diagram of the proposed CIS. This work makes use of conventional 4T PPD pixels. The schematic of the 4T PPD pixel employed in this design is shown in Fig. 2. It is based on a classical architecture and its timing diagram is drawn in Fig. 3: when the row select switch turns on at $t_1(0)$, as the reset switch is on (to prevent background illumination), the pixel output V_{PIX} goes up to V_{PIX_SUP}-V_{GS}, where V_{GS} is the gate-source voltage of the source-follower transistor (SF), if $V_{RST} > V_{PIX\_SUP} + V_{TH,RST}$, where $V_{TH,RST}$ is the threshold voltage of the reset transistor M_{RST}. At $t_2(0)$, M_{RST} turns off and V_{PIX} drops due to cross coupling from the falling clock signal at *RST*. At this moment, the column ADC starts to quantize the reset voltage, during $T_{ADC,1}$, until $t_3(0)$. $T_{ADC,1}$=2OSR·T_s, where T_s is the sampling clock duration, $T_s = 1/f_s$ while f_s is the delta-sigma ADC sampling clock frequency. OSR is the oversampling ratio of the ADC. Then, the transmission gate *TG* turns on and the photon induced charge inside the PPD is transferred to the FD. Once the *TG* turns off, the signal voltage is quantized by the ADC, during $T_{ADC,2}$, with: $T_{ADC,2} = T_{ADC,1}$. At the end of each row readout period, the switches, *RST* and *TG* are turned on at the same time to eliminate all the charges inside the PPD. At $t_1(T_1)$, the next row begins to be readout, and T_1 is the single row readout time. For an array having N rows, the frame readout time would be $N \cdot T_1$.

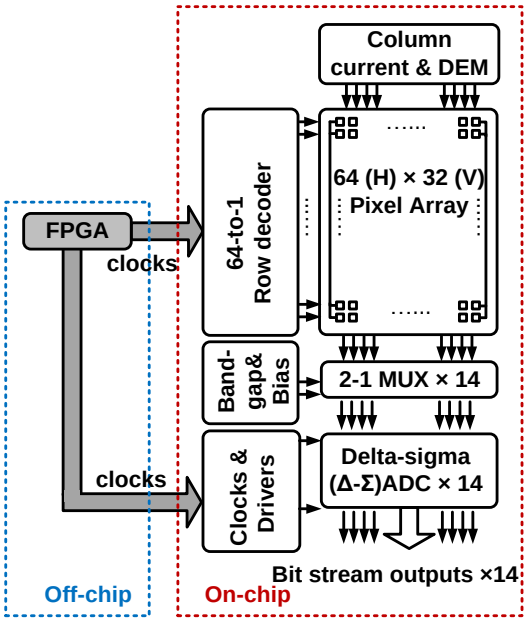

Fig. 1 Block diagram of the proposed CIS.

B. Imager Based Temperature sensor

The imager based temperature sensor re-uses the image pixel for thermal sensing [5]. To make sure a proper thermal sensing function, the following conditions have to be met: (1) $V_{RST} > V_{PIX\_SUP}+V_{TH,RST}$, then $V_{PIX} = V_{PIX\_SUP}$-V_{GS} if neglecting the voltage drop across the row select transistor. (2) TG must be off to avoid light induced charge which might disturb the FD node voltage. (3) All the pixels in the same column are selected so that the actual SF area equals that of a single SF times the number of devices in the same column. In this manner, if the SF works in subthreshold region, its voltage outputs, when biased with ratiometric currents, has a proportional-to-absolute-temperature (PTAT) behavior [5]:

$$\Delta V_{GS} = \frac{nkT}{q}\ln(N) \tag{1}$$

where n is a process dependent factor; k is the Boltzman constant; T is the absolute temperature in Kelvin and q is the unit electron charge. N is the ratiometric current ratio, e.g., 4 in this design and it is set precisely by a dynamic element matching (DEM) circuit. The thermal dependent voltage ΔV_{GS} is readout by the column incremental delta-sigma ADC as well.

C. Mismatches that cause FPN

It is well known that FPN caused by mismatches can be reduced by increasing device sizes. However, the pixel pitch is crucial for image quality and thus cannot be altered arbitrarily. For instance, if, increasing the SF size, the fill factor will drop. In theory, the mismatches between two current sources are [6]:

$$\left(\frac{\sigma(\Delta I_D)}{I_D}\right)^2 = \left(\frac{g_m}{I_D}\right)^2 \sigma^2(\Delta V_t) + \frac{\sigma^2(\Delta K')}{K'^2}$$

$$\sigma^2(\Delta V_t) = \frac{A_t^2}{WL} + S_{Vt}^2 D \tag{2}$$

$$\frac{\sigma^2(\Delta K')}{K'^2} = \frac{A_{K'}^2}{WL} + S_{K'}^2 D$$

$$K' = \frac{\mu_n C_{ox} W}{L}$$

where A_t, A_k S_{Vt}, S_K are the process parameters and D is the distances between the (two) devices. W and L are the width and length of the transistors, respectively; g_m, V_t and I_D are transconductance, threshold voltage and bias current of transistors, respectively. $K'=\mu_n C_{OX} W/L$ where μ_n is the surface carrier mobility and C_{OX} is the oxide capacitance per unit area. Meantime, the mismatches between two SF transistors when biased with the same current level is [6]:

$$\sigma^2(\Delta V_{GS}) = \frac{1}{WL}\left[A_t^2 + A_{K'}^2\left(\frac{I_D}{g_m}\right)^2\right] \tag{3}$$

Note the contrast between equation (2) and (3): one decreases and another increases with $I_D/g_m \propto V_{GS}$-V_{TH}. Transistor-level Monte Carlo simulations will be performed in Section III to further explain the above statement.

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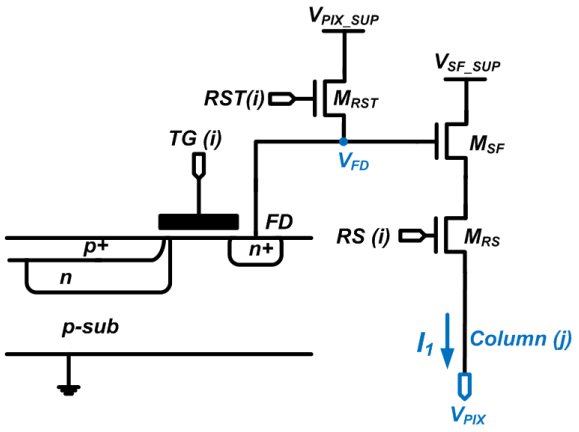

Fig. 2 Schematic of a 4T PPD image pixel.

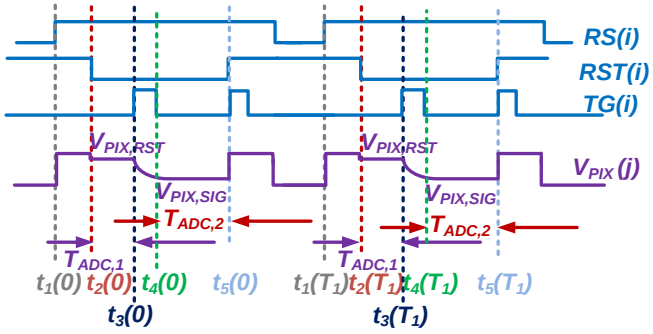

Fig. 3 Proposed image sensor's timing diagram

III. Monte Carlo Simulations of FPN

To investigate the influence of column biasing circuits on the pixel and the column FPN, Monte Carlo simulations are performed in Cadence Environment, using 0.18 µm transistor level design. Firstly, in this section/paper, FPN is defined as the ratio between the standard deviation and the mean of the measured value. To focus investigating on the effects from the column bias circuits, the pixel size and other circuit parameters are maintained. Fig. 4 shows the column bias circuit schematic employed in the simulation. Fig. 5 compares the gain and offset FPNs against the device length, while W and L are increased in proportion to keep V_{GS}-V_{TH} constant. Fig. 6 shows the offset and gain FPN extracted from 100 Monte Carlo runs, versus overdrive voltage V_{GS}-V_{TH} = $2I_D/g_m$ when keeping the bias current constant by adjusting W accordingly, for the same line in Fig. 6. The device L is 1.2 µm (in Fig. 4) to make sure the influence from increasing W is negligible. When the transistor multiplier m increases from 1 to 8, the bias currents go up proportionally.

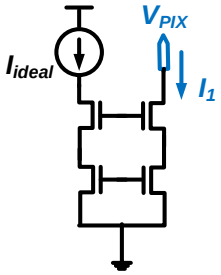

Fig. 4 Column bias circuit for the Monte Carlo simulations.

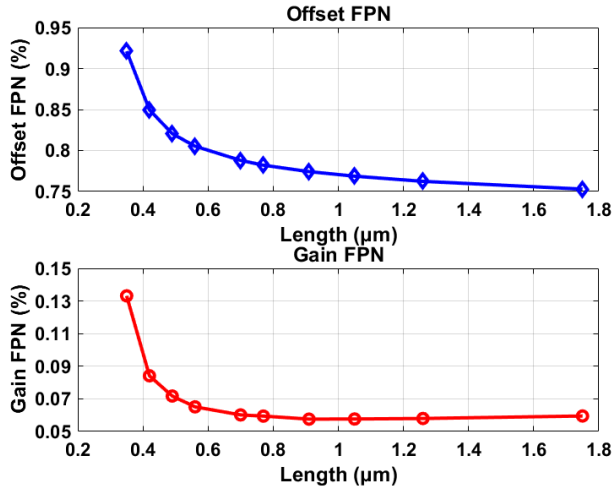

Fig. 5 100 Monte Carlo runs of pixel gain and offset FPN, versus device dimension L. W is increased in proportion to keep the bias current and overdrive voltage constant. The column current is approximately 3.6 µA.

A few observations and deductions can be made from Fig. 5 and Fig. 6. Firstly, when the transistor length (and width) is relatively small, the mismatches from current bias circuits can contribute an equal or more weight to the total gain and offset FPN, compared to those from the pixel. For example, the mismatches among the pixels contribute to around 0.06 % (gain FPN) in the bottom graph of Fig. 5. Accordingly, when W and L (of the column bias transistors) are smaller, the gain FPN is 0.13 %, indicating that they (the column bias devices) contribute more than 0.11 % to the total gain FPN. Secondly, when the channel length reaches a reasonable level (e.g., 1.2 µm), the contributions to the total FPN from the bias current's mismatches become less significant. Thirdly, as expected in equation (1), for the same V_{GS}-V_{TH}, the larger the bias current, the worse the FPN is, as shown in Fig. 6, from m = 1 to m = 8 (m is the transistor multiplier number). Fourthly, despite the predictions in equation (1), an increased overdrive voltage V_{GS}-V_{TH} does not necessarily lead to any decrease in offset or gain FPN, at least when the device size is reasonably large. Possible reasons include: W is larger for smaller V_{GS}-V_{TH} to maintain the same current; the bias transistor goes from weak to strong inversion as V_{GS}-V_{TH} rises and when it is in weak inversion, it is less sensitive to V_{TH}, which in its turn is process dependent. Although this is not exactly what has been predicted in equation (1), it is a more practical situation: one cannot change V_{GS}-V_{TH} while leaving the bias transistor area intact. The last but not the least, one thing that is certain from Fig. 6 is

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that if one wants to minimize the FPN, one has to use a moderate current level that meets the speed requirements. As a larger current would increase the mismatches among the pixel SFs, as shown in Fig. 6.

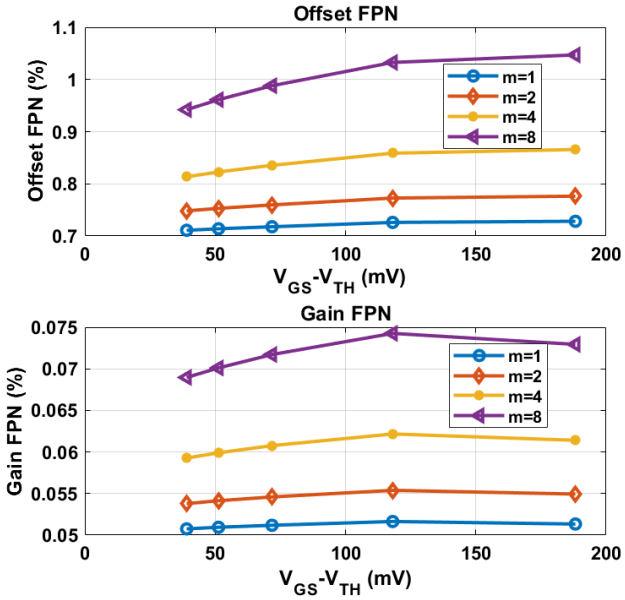

Fig. 6 100 Monte Carlo simulations of pixel gain and offset FPN, versus V_{GS}-V_{TH}, when current is kept the same (for the same line) by adjusting bias transistor width *W*. The effects from varying *W* is kept to a minimum by using a considerably large *L*=1.2 µm. *m* is the transistor multiplier number to increase the current proportionally.

IV. Noise Composition

The measured dark FPN plus temporal noise($\sigma^2_{MEASURED}$), is defined in this paper, as a combination of the DSNU ($\sigma^2_{DSNU,I}$), which is the FPN and the temporal noise ($\sigma^2_{TEMPORAL}$), in the following manner:

$$\sigma^2_{MEASURED}=\sigma^2_{DSNU}+\sigma^2_{TEMPORAL}/OSR \qquad (4)$$

which indicates that when averaging more number of frames and the temporal noise is suppressed, and the measured noise approximates the DSNU. The temporal noise of an image sensor can be expressed in electrons (e^-), which is referred to the SF gate. Theoretically, the input referred temporal noise power spectral density (PSD) is [7]:

$$S_n(f)=v_n^{\,2}=\frac{8}{3g_{m1}}kT(1+\frac{g_{m2}}{g_{m1}})+\left[N_{f1}+\left(\frac{g_{m2}}{g_{m1}}\right)^2 N_{f2}\right]\frac{1}{f} \qquad (5)$$

where the Boltzman constant k=1.38e^{-23} J/K; $g_{m1,2}$ and $N_{f1,2}$ are the trans-conductance and flicker noise parameters of the SF and the bias circuit common source transistor, respectively. Indicated in equation (3): increasing the area of the biasing circuit to a reasonable degree would help to reduce the flicker noise. In addition, to reduce the input referred temporal noise, one might increase W/L of the SF, albeit this may be impractical or infeasible, as the layout of the SF is optimized for imaging performances. Therefore, for g_{m1} set by the combination of the SF geometry and the bias current determined by speed, one could reduce g_{m2}, by reducing its W/L ratio. The temporal noise shown in equation (3) is further suppressed by a factor of √OSR (of the column oversampling ADC), e.g., if OSR=128, the noise could be further suppressed by a factor of 11.

V. 2ND Order Incremental Delta-Sigma ADC

Fig. 7 shows the schematic of the 2nd order incremental delta-sigma ADC used in this design, in reference to [8] below. Despite the pixel output is single-sided, the ADC is actually fully differential, whose design considerations are better power supply rejection ration (PSRR) and immunity to even order harmonic distortion. Its second input is the common mode voltage. At a supply voltage of 3.3 V, the opamp has a DC gain of 72 dB and unity-gain-bandwidth (UBW) of 20 MHz with a loading capacitor of 400 fF. C11 is sized according to the noise requirements *kT*/C11/OSR (e.g., 10 µV in this design, when OSR=128). The power supply is equal to the pixel supply voltage to ensure the ADC is able to handle the pixel output. The first stage opamp is sized 4 times as large as the second, both of which share the bias circuits. Being a fully differential design, it has a folded cascode architecture and needs a switched capacitor common mode feedback (CMFB) [8]. The comparator design is similar to that in [9], except our design has a pre-amp biased by a constant voltage for lower noise. Its output is bit stream and the decimation filter is off-chip for more flexibility in post-processing. The delta-sigma's measurement results will be reported in Section VI.

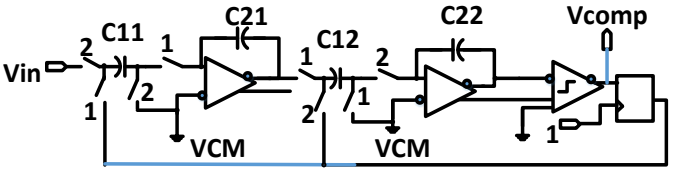

Fig. 7 Schematic of the 2nd-order delta-sigma modulator in this design.

VI. Measurement Results of Column-Level Incremental Delta-Sigma ADC

Fabricated using 0.18 µm CIS technology, a micrograph of the chip is shown in Fig. 8. Each of the 14 column incremental delta-sigma ADCs occupies an area of 20 µm × 900 µm. The CIS pixel pitch is 11 µm × 11 µm. With a power supply voltage of 3.3 V, the ADC consumes 36 µW of power.

The column-level incremental delta-sigma ADCs, based on the schematic shown in Section V, are measured. The input signal is a 800 mVp-p (-8 dB of the full scale voltage, which is 2 Vp-p), 349 Hz sine wave, generated by an Agilent 3220A function generator. The reference voltage range of the ADC is 2 V (as a fully differential ADC, with low voltage reference of 0.7 V and high voltage reference of 1.7 V). The digital outputs are captured by Labview and post-processed using decimator filters implemented in MATLAB. Instead of using a 13 bit (max bit weight=128) cascade integrator as that in [10], two cascade 5.5 bit ones (max bit weight=64) are employed to further suppress high frequency noise. The FFT plot measured of column #1 at a sampling frequency of 2 MHz and OSR = 128

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(after the decimation filter) is shown in Fig. 9. By quadrupling the OSR (128 compared to 32), SNR is increased by approximately 12 dB, as shown in Fig. 10.

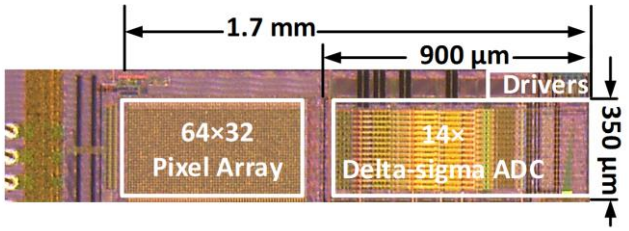

Fig. 8 Micrograph of the chip.

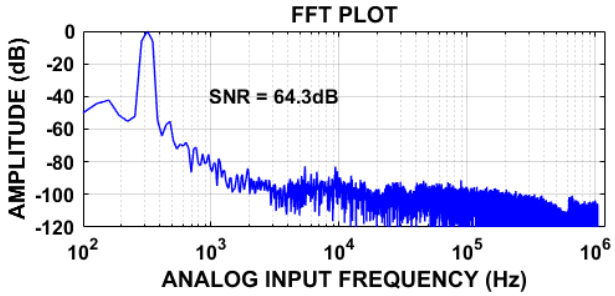

Fig. 9 Measured FFT the column #1 incremental delta-sigma ADC, when input signal is at -8 dB of full scale, when OSR=128, 13 bit, and sampling at 2 MHz. This result is after the decimation filter.

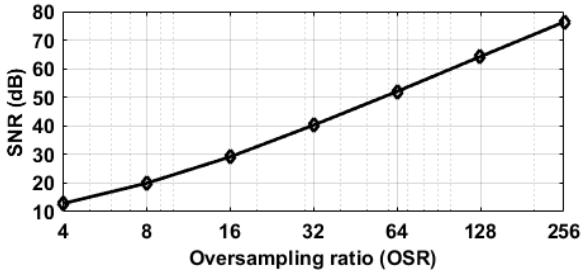

Fig. 10 Measured SNR versus oversampling frequency (OSR), when input signal at -8 dB of full scale, and sampling at 2 MHz.

VII. Measurement Results of the CIS

Fabricated using 0.18 µm CIS technology, the 64×32 CIS array was shown in Fig. 8. The pixel architecture is based on the 4T PPD image pixel schematic shown in Fig. 2. Its column ADCs are those measured in Section VI.

A. Column FPN

In our FPN measurements, the change of column bias transistor device width, to keep the bias current constant, is realized by the dynamic element matching (DEM) circuit with a phase number of 4. Fig. 11 shows the measured column level offset and gain FPN, for different current levels. It can be seen that a larger bias current reduces the column offset FPN and increases the column gain FPN. In addition, the gain FPN decreases with increased V_{GS}-V_{TH}, especially when V_{GS}-V_{TH} is relatively smaller. As in practice, the offset FPN can be corrected by CDS, one may need to keep the bias current low, as long as the speed requirements are met, for reducing column gain FPN.

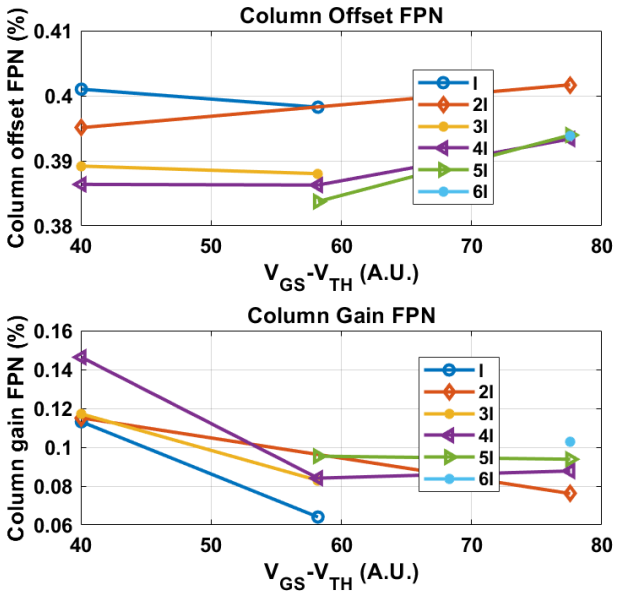

Fig. 11 Measured column FPN versus V_{GS}-V_{TH} for different levels of current bias.

B. Temporal Noise

The pixel temporal noise has been measured, referred to the pixel output, among 100 captures, from 256 pixels and its histogram is shown in Fig. 12. The averaged noise is measured 34 µV rms, when the OSR of the ADC is kept at 128, but the full scale voltage is reduced to 250 mV (while still sampling at 2 MHz) so that the noise measurement is not limited by the resolution (250 mV/(2·2^13) = 15 µV) of the ADC. The conversion gain (CG) of the pixel is 73 µV/e$^-$ and the measured averaged noise level translates to less than 0.5 e$^-$ input referred temporal noise. When the OSR is lower, the measured noise increases, in a similar manner as shown in Fig. 10. The low temporal noise, compared to [5] and [10] can be explained as follows: (i) higher order (2nd versus 1st order) oversampling ADCs and (ii) longer length (4 µm versus 1 µm) of the column current biasing devices and its smaller W/L.

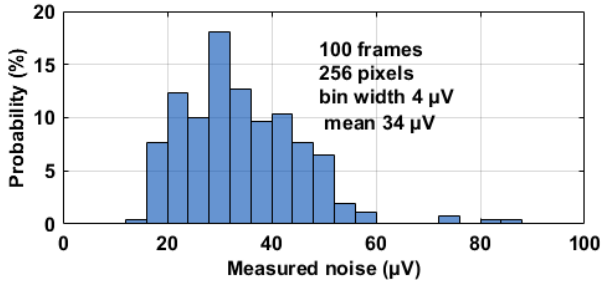

Fig. 12 Measured pixel output referred temporal noise histogram among 100 frames from 256 pixels, when the CG is 73 µV/e$^-$ and the OSR equals 128.

C. Imager based Temperature Sensor

For thermal sensing, the image pixel array is reconfigured by selecting all the 64 rows' SF in the same column and then quantized by the column 2nd-order delta-sigma ADCs. 26 pixel column based temperature sensors have been measured from 2 chips, at an interval of 10 ºC, between -20 ºC and 80 ºC and their measurement results are shown in Fig. 13. The reference

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temperature (x-axis) is from a calibrated temperature sensor, pt100 having an accuracy of 0.02 ºC. Without calibration, the 1 σ process variability among all the pixel column based temperature sensors is around ±0.45 %. The sensor outputs change by approximately 600 DN over 100 ºC, which makes a resolution of 0.16 ºC/DN. Upon a two-point calibration at -10 and 60 ºC for each individual sensor and then after a 2nd-order master curve fitting for all the sensors, the measured errors are less than ±0.65 ºC, with 3 σ inaccuracy less than ±1.4 ºC. Alternatively, upon a one-point calibration for each sensor at 30 ºC and a 2nd-order master curve fitting, the measured errors and 3 σ inaccuracy are less than ±1.2 ºC and ±2.2 ºC, respectively. Normally, at least a one-point calibration can be done, otherwise, the untrimmed accuracy can be kept within ±3 ºC, taking into account the process variability of 0.45 % (1 σ), which will add ±1.5 ºC of additional errors, when the sensors are untrimmed. Alternatively, if using the entire pixel array as one temperature sensor, the thermal sensing accuracy can be kept within ±0.2 ºC. Compared to our last prototype in [5], this work has less untrimmed process variability and hence better accuracy upon a one-point calibration, due to longer bias current device length, while maintaining the pixel design and layout dimensions.

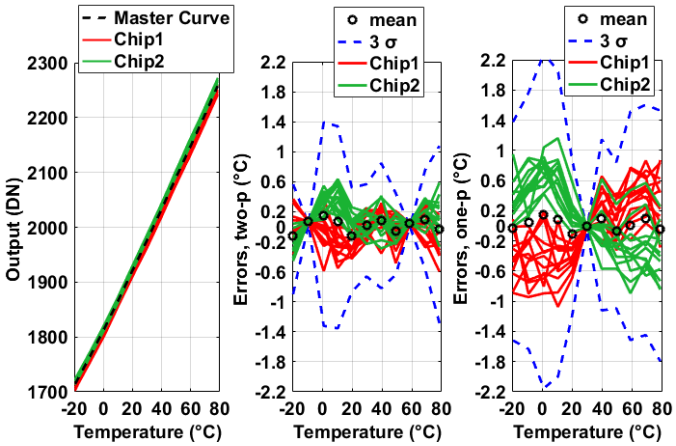

Fig. 13 Measured digital outputs (DN, left) and errors upon a two-point calibration for each sensor at -10 and 60 ºC (middle) and errors upon a one-point calibration at 30 ºC (right).

D. Dark current, DSNU plus temporal noise (total noise) and their thermal compensation

This section describes the compensation for dark current and the attempts to suppress the temporal noise that is measured along with the dark FPN, when the dark FPN is not averaged for many frames, e.g., 10000, to suppress the temporal noise to a negligible level, using column-level oversampling ADCs, as well as using the in-pixel thermal information. Fig. 14 (left graph) shows the measured dark current, between 30 ºC and 80 ºC. It can be seen at 60 ºC, the measured dark current is around 2200 e^-/s, or equivalently 290 pA/cm^2, with a fill factor of 50 %, in a 11 µm × 11 µm pixel. Meantime, the dark current is modeled with an exponential fit ($y = a \cdot exp(b \cdot T)$, where a and b are constants and T is the temperature). When using the measured temperature T (from the temperature sensors from Section C) to predict the dark current y, based on known a and b obtained from the left graph, the prediction can be as close as 95 %. In other words, the estimation errors are within ±5 %. Fig. 15 shows the dark signal before thermal compensation. It shows visible column FPN like dark non-uniformity (shade). However, the column gain FPN has been measured to be no more than 0.15 % in Section A. In general, both an elevated temperature and increased thermal gradients contribute to dark FPN. Using the imager based temperature sensors presented in Section C, each of the middle 22 columns' temperature has been measured and shown in Fig. 17. It can be seen that a 0.4 ºC of thermal gradients has been measured across the array. The generations of the thermal gradients are because other circuits (not related to this paper) are also implemented on the same chip and generate some heat to the left side of the image pixel array in this paper. The dark FPN is measured to decrease from 3.6 % to 3.2 %, by an absolute 0.4 % and relative 13 %, using thermal compensation facilitated by the in-pixel temperature sensors. The dark FPN plus temporal noise is also measured versus the OSR and shown in Fig. 18, indicating a reasonable large OSR (e.g., 48) in fact suppresses the temporal noise, compared to when OSR is smaller and also makes the thermal compensation more effective. The explanations can be similar to that in [2] which demonstrates that oversampling (correlated multiple sampling, CMS) reduces the temporal noise, which is measured along with the column FPN [2].

E. Linearity

The non-linearity of the CIS has been measured to be lower than ±1 %, between 5 % and 95 % of its saturation level and with the OSR=128, as shown in Fig. 19. The largest value of a 13 bit ADC measuring the linearity is 2^{13}=8192, when OSR=128, so the output range of the CIS is approximately (6000/2^13)×2 V=1.46 V. Taking into considerations the measured readout noise of 34 µV in Section B, the dynamic range of the CIS can be 92 dB (when OSR=128).

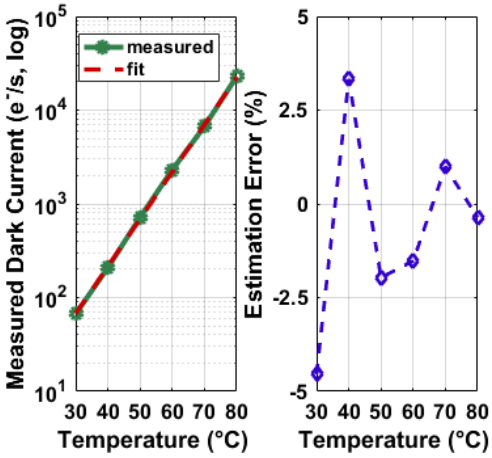

Fig. 14 Measured dark current (in e^-/s, logscale, left) and the estimation errors (right) using its exponential fit $y = a \cdot exp(b \cdot T)$.

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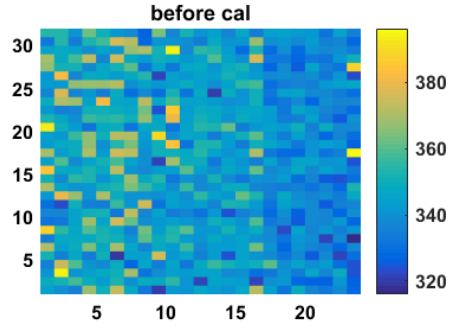

Fig. 15 Measured dark signal before thermal compensation, at 60 ºC and 500 ms.

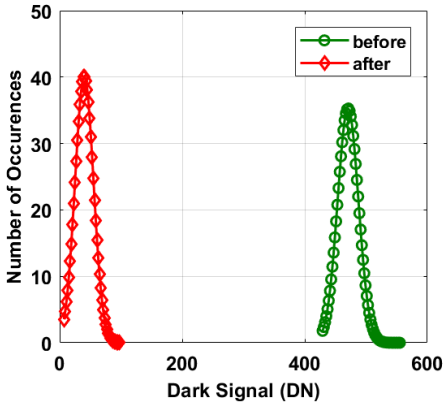

Fig. 16 Histograms of measured dark signal before (at 60 ºC and 500 ms) and after thermal compensation (room temperature), using $y = a \cdot \exp(b \cdot T)$ and the thermal map of Fig. 17.

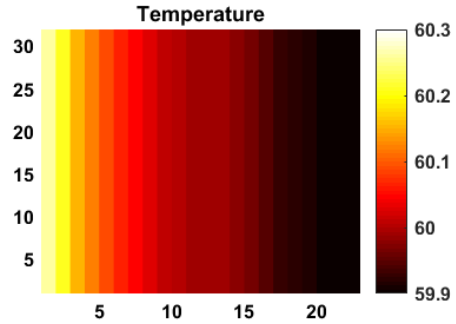

Fig. 17 Measured thermal map of the CIS array, using the column-imager based temperature sensors of Section C, for thermal compensation of Fig. 15. The temperature sensors are calibrated before hand to ensure minimum measurements errors.

For noise suppression, the upper limit of the column bias transistor's length is set by the speed requirements. The reasons are a longer device length (and width) leads to larger parasitic capacitance at the column output. The oversampling ADC's conversion time increases with its oversampling ratio. Fortunately, for each sampling, its conversion time can be shorter (compared to an alternative without oversampling), as its input capacitance can be kept smaller (for the same kT/C noise level), thanks to oversampling. The thermal compensation of dark current in a CIS can be performed much less often than the readout of the image sensors, as the thermal networks are slower compared to their electronic alternatives.

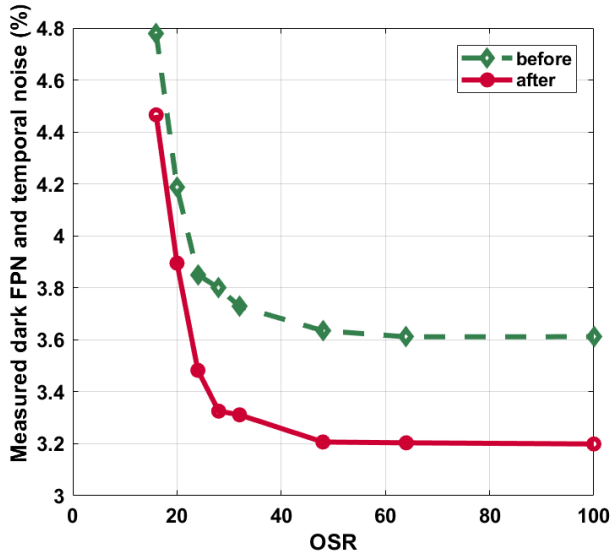

Fig. 18 Meaured dark FPN (DSNU) and temporal noise, along with quantization noise when the OSR is lower (e.g., lower than 30), before and after thermal compensation, versus OSR.

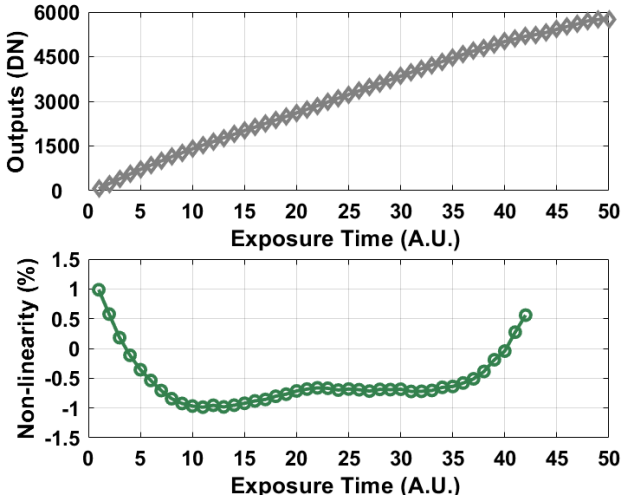

Fig. 19 Measured Non-linearity of the image sensor between 5 % and 95 % of the saturation level.

VIII. Conclusions

This paper aims to suppress the temporal noise which is measured along with the spatial dark FPN (DSNU) and to compensate for the dark current of a CMOS image sensor. This is achieved by: (i) longer-length column-level current bias devices, (ii) column-level 2nd-order incremental delta-sigma ADCs and (iii) imager-pixel based thermal sensors. Particularly, for (i), this paper demonstrates that by using sufficiently large current bias devices, both the FPN and the temporal noise can be suppressed quite effectively, without modifying the pixel design. The dark current is compensated by 92 % and the FPN is further suppressed by 13 %, with the aid of in-pixel thermal sensing. The CIS is measured to have a temporal noise of 34 µV rms (0.5 e^- rms input referred, with OSR = 128 and with a CG of 73 µV/e^-), a DR of 92 dB, a dark current of 290 pA/cm^2, before compensation and equivalent to

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Table I Comparison with the state-of-the-art CISs

	This work	[5]	[2]	[3]	[4]	[12]
Process	0.18 µm	0.18 µm	0.35 µm	0.18 µm	0.18 µm	90 nm
Pixel	4T PPD	4T PPD	3 T	STI-less shared	4T HDR PPD	1.75 T shared
Array size	64×28	64×32	480 k	50×570	2048×2048	1920×1440
Pixel pitch	11 µm × 11 µm	11 µm × 11 µm	16 µm × 16 µm	7.5 µm × 7.5 µm	6.5 µm × 6.5 µm	1.4 µm × 1.4 µm
Fill factor	50 %	50 %	N/A	43 %	N/A	N/A
CG (µV/e^-)	73	73	N/A	22.9	20 ~80	N/A
DR (dB)	92	80	84	N/A	87	66.5
Noise	32 µVrms (0.42 e^-)	140 µVrms (2 e^-)	3.5 e^-rms	92.5 µVrms	2 e^-rms	273.6 µVrms
Dark current	290 pA/cm^2 @ 60 ºC (before compensation) 15 pA/cm^2@ 60 ºC (after compensation)	296 pA/cm^2 @ 60 ºC (before compensation) 60 pA/cm^2 @ 60 ºC (after compensation)	N/A	30 pA/cm^2	5.7 pA @ room temperature	N/A
DSNU	3.6 % (before thermal compensation) @ 60 ºC, 250 ms 3.2 % (after thermal compensation), @ 60 ºC, 250 ms	6.7 % @ 60 ºC, 250 ms	N/A	N/A	N/A	N/A
Non-Linearity	1 %	N/A	N/A	N/A	0.5 %	N/A

15 pA/cm^2 after compensation, at 60 ºC, and a dark FPN (DSNU) of 3.2 % (OSR = 64), a non-linearity better than 1 % and a column gain FPN of 0.06 %. It is well known by using oversampling ADC, the temporal noise can be reduced. This paper demonstrates that since the temporal noise is also measured along with the dark FPN (DSNU) (when, in most applications, the measured dark FPN is not averaged for many, e.g., 10000 frames, to suppress the temporal noise to a negligible level), the total measured DSNU plus temporal noise can be reduced, as the OSR increases, until the point that the temporal noise is negligible. A comparison of this design with the state-of-the-art CISs is shown in Table I. Table II compares the proposed imager based temperature sensor with the state-of-the-art MOS based temperature sensors: this work requires no additional area while maintaining the FOM and relative accuracy.

Table II A comparison with the state-of-the-art temperature sensors

	This work	[13]	[14]	[15]
Sensor Type	MOS	MOS	MOS	MOS
CMOS Technology	0.18 µm	0.18 µm	28 nm	90 nm
Area (µm^2)	No additional area	89000	1000	74 slices
Temperature Range	-20 ^{0}C to 80 ^{0}C	-20 ^{0}C to 80 ^{0}C	-5 ^{0}C to 85 ^{0}C	-20 ^{0}C to 100 ^{0}C
3 σ accuracy	±1.4 ^{0}C	±1 ^{0}C	-3.3/1.9 ^{0}C	-0.7/1.1 ^{0}C
Calibration	Two-point	Two-point	One-point	One-point
Power Consumption (µW)	36	0.8	56	90
Conversion Time (ms)	1.28	800	0.036	1
Resolution (^{0}C)	0.14	0.09	0.76	0.05
Resolution FOM (nJ·K^2)[a]	0.9	5.3	1.2	0.23
Rel.IA (%)	2.6	2	5.8	1.5

[a] Energy/Conversion×(Resolution)^2, in reference to [16]
[b] 3 σ accuracy /temperature range, in reference to [16]

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REFERENCES

[1] J. M. Margarit, G. Vergara, V. Villamayor, R. Gutiérrez-Álvarez, C. Fernández-Montojo, L. Terés, and F. Serra-Graells, "A 2 kfps Sub-µW/Pix Uncooled-PbSe Digital Imager With 10 Bit DR Adjustment and FPN Correction for High-Speed and Low-Cost MWIR Applications," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 10, pp. 2394-2405, 2015..

[2] N. Chen, S. Zhong, M. Zou, J. Zhang, Z. Ji, and L. Yao, "A Low-Noise CMOS Image Sensor With Digital Correlated Multiple Sampling," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 1, pp. 84-94, 2018.

[3] M. Seo, S. Kawahito, K. Yasutomi, K. Kagawa, and N. Teranishi, "A Low Dark Leakage Current High-Sensitivity CMOS Image Sensor With STI-Less Shared Pixel Design," *IEEE Transactions on Electron Devices*, vol. 61, no. 6, pp. 2093-2097, 2014.

[4] C. Ma, Y. Liu, Y. Li, Q. Zhou, X. Wang, and Y. Chang, "A 4-M Pixel High Dynamic Range, Low-Noise CMOS Image Sensor With Low-Power Counting ADC," *IEEE Transactions on Electron Devices*, vol. 64, no. 8, pp. 3199-3205, 2017.

[5] S. Xie, A. A. Prouza, and A. Theuwissen, "A CMOS-Imager-Pixel-Based Temperature Sensor for Dark Current Compensation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Early Access, pp. 1-1, 2019.

[6] T.C. Carusone, D.A. Johns, K.W. Martin, Analog Integrated Circuit Design. USA: Wiley, 2012.

[7] X. Ge, B. Mamdy, and A. Theuwissen, A comparative noise analysis and measurement for n-type and p-type pixels with CMS technique, *Electronic Imaging* 2016 (12).
[8] Schreier, R. and Temes, G.C., Understanding delta-Sigma Converters, (WILEY, 2005).
[9] J. H. Tsai *et al.*, "A 0.003 mm 10 b 240 MS/s 0.7 mW SAR ADC in 28 nm CMOS With Digital Error Correction and Correlated-Reversed Switching", *IEEE Journal of Solid-State Circuits*, vol. 50, no. 6, pp. 1382-1398, 2015.
[10] Y. Chae, et al., "A 2.1 M Pixels, 120 Frame/s CMOS Image Sensor With Column-Parallel ADC Architecture," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 236-247, 2011.
[11] S. Xie, A. Abarca, A. Theuwissen "A CMOS Image Sensor with In-Pixel Temperature Sensors for Dark Signal Non-Uniformity Compensation," accepted for presentation in IISW 2019.
[12] S. Hwang, J. Chung, H. Kim, I. Jang, M. Seo, S. Cho, H. Kang, M. Kwon, and S. Ryu, "A 2.7-M Pixels 64-mW CMOS Image Sensor With Multicolumn-Parallel Noise-Shaping SAR ADCs," *IEEE Transactions on Electron Devices*, vol. 65, no. 3, pp. 1119-1126, 2018.
[13] W. Song, J. Lee, N. Cho, and J. Burm, "An Ultralow Power Time-Domain Temperature Sensor With Time-Domain Delta–Sigma TDC," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 10, pp. 1117-1121, 2017.
[14] M. Cochet, et. al, "A 225 µm2 probe single-point calibration digital temperature sensor using body-bias calibration in 28nm FD-SOI CMOS," *IEEE Solid-State Circuits Letters, vol. 1, no. 1, pp. 14-17, 2018.*
[15] C. Chen, Y. Lin, and S. You, "An All-Digital Time-Domain Smart Temperature Sensor With a Cost-Efficient Curvature Correction," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, pp. 1-8, 2018.
[16] K. Makinwa, Smart Temperature Sensor Survey, available online at: https://ei.tudelft.nl/smart_temperature/, Sep. 2018.

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