A CMOS image sensor with improved readout speed using column SAR ADC with digital error correction

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***Abstract*—This paper proposes a CMOS image sensor (CIS) whose readout speed is improved by 33%, through applying a digital error correction (DEC) method to its column-level successive approximation register (SAR) analog to digital converters (ADC), compared to an alternative without using the DEC technique. The proposed addition-only DEC alleviates the ADC's incomplete settling errors, hence improving conversion rate while maintaining accuracy. It is based on a binary bridged SAR architecture with 4 redundant capacitors and conversion cycles, which ensure the ADC's linearity of 10 bit within a 5 bit accuracy's settling time. Simulation results show the DEC method improves the ADC's static and dynamic linearity, eliminating its missing codes and increasing its signal to noise plus distortion ratio (SNDR) from 64.5 dB to 67.5 dB, when operating at the same sampling speed. The proposed SAR keeps the same straightforward timing diagram as that in a conventional SAR ADC, incurring no offset to the ADC, while increasing the sampling rate by 33 %. The simulated linearity of the prototype CIS is within ±0.07 %, when sampled at a column readout rate of 10 MHz.**

Keywords—CMOS image sensor, digital error correction, successive approximation register, analog-to-digital converter, SAR, ADC, DEC

I. INTRODUCTION

Industrial applications such as machine vision requires a CIS to have continuous readout speed between 100 fps and 10 Mfps [1][2]. In theory, the maximum achievable readout speed is constrained by the voltage-to-digital conversion. 128 analog memories per pixel have been implemented on-chip to achieve a burst readout speed of 1T pixel/s in [2], for 128 burst instead of continuous video outputs, and 780 Mpixel/s (or, 2 mega columns/s) continuous outputs. In [1], the pixel source-follower (SF) and correlated double sampling (CDS) circuits have been optimized, achieving a continuous column readout speed of approximately 2 MHz. On the other hand, in previous publications, despite being a crucial component in the aforementioned voltage to digital conversion, the column ADC has seldom been optimized to further improve the continuous readout speed. This paper aims to explore the maximum achievable continuous readout speed without incurring additional area (e.g., on-chip memories), using area and power efficient column readout circuits in a standard CIS technology process. This aim is achieved by employing DEC for a bridged SAR ADC as column ADC that features a conversion rate of 11 MHz. This translates to a higher continuous column conversion rate, compared to previous publications [1][2]. SAR ADCs are known for their medium resolution, prominent area and power efficiency [3]–[6]. They have been recently used for high speed applications ranging from a few tens to a few hundred megahertz [7]–[9]. An N bit accurate conventional SAR ADC operates as both an N bit ADC and an N bit charge balancing DAC, both of which have to meet the accuracy of N bit [9]. In contrast, in SAR ADCs with DEC [7]–[9], the DAC settling time could be less than $-ln(1/2^{(N+1)})\cdot\tau$ [10], which is required for a conventional counterpart, while τ being the product of RC in the DAC. DEC is generally based on the principle that if a comparator misjudges in a step, either due to comparator dynamic offset or incomplete settling, the following steps could correct for the misjudge: given that in each step, the DAC increases or decreases the charge balancing node voltage in an amount (Δ %) proportionally less than that in a conventional counterpart. The value of Δ % and the DEC logic determines the amount of settling errors that could be compensated for (e.g., up to 37 % in [8]) or the comparator offset that could be tolerated (e.g., $\pm V_{REF}/8$ in a 1.5 bit/stage pipelined ADC while V_{REF} is its full range voltage), without incurring linearity penalties. Based on the aforementioned redundancy algorithm, this paper presents an alternative DEC method, which retains the straightforward timing diagram in a conventional binary SAR ADC, while removing missing codes due to incomplete settling and comparator dynamic offset, when operating at the same sampling rate as the conventional one. The missing code removal is achieved by introducing 4 additional unit sized capacitors and conversion cycles. This paper is organized as follows. Section II explains the operating principles and section III shows the simulation results. Section IV concludes this paper.

II. OPERATING PRINCIPLES

A. DEC in bridged SAR ADC

Fig. 1 a [11] shows a conventional schematic: each time a bit switches, a voltage of $\pm V_{REF}\cdot Ci/2C_{TOTAL}$ is added or subtracted from the charge balancing node Vx, which is successively approximated toward $V_{CM}=V_{REF}/2$, depending on the logic value of Bi (1 or 0), where Ci and C_{TOTAL} are the capacitance of the bit Bi (i=1~10) and the total ADC, respectively. In the proposed schematic shown in Fig. 1(b), the weight of the two redundant capacitors B5 and B6 adds approximately another 1/32 of the total capacitance to the left side capacitor array. In this way, each time a bit switches, the voltage added or subtracted is scaled by a factor $Scale\_factor$=31/32, approximately. For instance, if B0 incurs an incomplete settling error of 1/32, and causes the comparator to misjudge for the logic value of B1, the maximum error accumulated after B1's switching is $(V_{REF}/(4\cdot32)+V_{REF}/8)\cdot Scale\_factor$ (assuming that B1 is fully settled to simplify the discussion at this moment), which is the sum of B0's settling error $(V_{REF}/(4\cdot32))\cdot Scale\_factor$ and B1's weight $(V_{REF}/8)\cdot Scale\_factor$. The maximum weight of the remaining capacitors are $(V_{REF}/8+V_{REF}/64)\cdot Scale\_factor$, which can fully quantize and compensate for the errors resulting from switching the first two bits. The bit value of B5 and B6 can be 01, 10, 11 and 00. For the first two cases (01 and 10), these two capacitors can be seen as one parasitic capacitor that is always connected to V_{CM} and only shrinks the ADC's gain as a whole, but incurring no offset. For the case 11 and 00, B5 and B6 functions as one capacitor of the unit capacitor size C, adding or subtracting a voltage of $V_{REF}/64$ from the node Vx.

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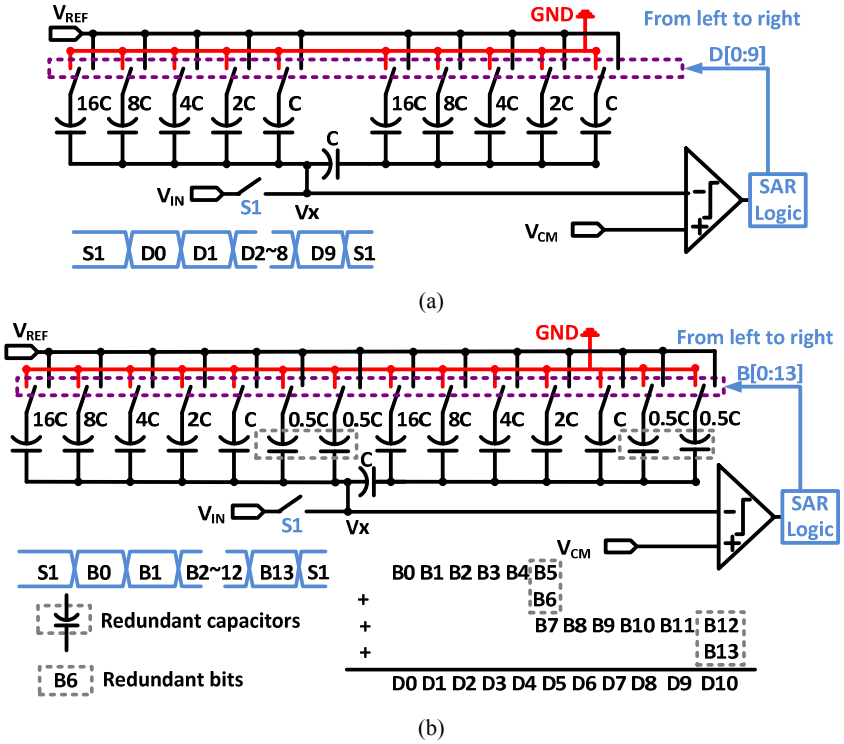


Fig. 1 Conventional and proposed bridged SAR ADCs. (a) Conventional bridged SAR ADC and its timing diagram. (b) Proposed bridged SAR ADC, its timing diagram and DEC logic.

This would compensate for up to the same amount of incomplete settling errors ($\pm V_{REF}/64$) from earlier bits. The settling errors of B5~B11 can be corrected by B12 and B13, in a similar manner. As a result, the settling time per step required for the SAR ADC will be $-\ln(1/32)\approx 3.4\tau$, in theory, compared to $7.6\tau=(ln(1/2^{(N+1)})\cdot\tau,\ N=10)$ for a conventional SAR. Taking into consideration the 4 redundant cycles, the proposed DEC method improves the sampling speed (or reducing the total conversion time) by 33%, without incurring penalties in the ADC's linearity. The proposed DEC algorithm is also able to tolerate comparator offsets, given their effects when combined with that from incomplete settling, are less than $\pm V_{REF}/64$. Comparator dynamic offset can be caused by drain-source voltage variations of the input transistors and the parasitic capacitors [12], which are related to plate voltages. From the DEC logic illustrated in Fig. 1 (b), the bridged SAR is mathematically analogous to a two-step one, where DEC makes the accuracy requirement of the first ADC 5 bit instead of 10 bit, which is the case for Fig. 1 (a). The reasons are that in a SAR without redundancy as shown in Fig. 1 (a), the settling errors, in a similar way as the quantization errors, will lead to overflow to the latter bits, and thus can never be corrected. In contrast, in the proposed design shown in Fig. 1 (b), a 10 bit's ADC's accuracy requirement is $\pm 1/2^{11}\cdot V_{REF}$ and the 6-bit second stage (B6~B13) can quantize up to a total of $\pm 1/2^{5}\cdot V_{REF}$, which could cover the non-ideal 5-bit first stage (B1~B5)'s quantization error ($\pm 1/2^{5}\cdot V_{REF}$). B5 and B6 could be seen as one bit with the same weight as B4, according to the aforementioned discussion, which also applies to B12 and B13.

B. *CIS:3T pixel architecture & programmable gain amplifier (PGA)*

Fig. 2 and Fig. 3 show the classical 3-transitor (3T) active pixel architecture used in the design and its timing diagram, respectively. The removal of the transmission gate has eliminated the requirements of high-speed charge transfer between the photodiode and the floating diffusion. At $t_1(0)$, the row select switch (*RS*) and reset switch (*RST*) are both on and when the $V_{RST}>V_{PIX\_SUP}+V_{TH}$ (V_{TH} being the threshold voltage of M_{RST}), the M_{SF} gate voltage V_{PD} equals that of V_{PIX_SUP} and the pixel output voltage $V_{PIX,RST}=V_{PIX\_SUP}-V_{GS}$ (V_{GS} is the gate-source voltage of M_{SF}), if ignoring the voltage drop on the row select switch M_{RS}. When *RST* goes from on to off at $t_2(0)$, the voltage V_{PIX} goes down in a slope proportional to $dV_{PIX}/dt=i_{photo}/C_{PD}$, where i_{photo} is the photo current proportional to photodiode area and input light density, and C_{PD} is the capacitance at node V_{PD}.

To alleviate the constraint of the speed of PGA circuit on that of the CIS and to achieve reasonable unity-gain-bandwidth (UBW) using less biasing current, two cascade stages of PGA, each of which having a maximum gain of 4 (12 dB), is used, as shown in Fig. 4, achieving a total gain of 16 (24 dB). As $UBW=\beta\cdot g_m/C_L$ (where β is the feedback factor of the PGA), e.g., when the PGA gain is 4, $\beta=1/4$; g_m and C_L are the transconductance of the input pair and capacitive load of the opamp, respectively. Compared to a single PGA stage of the same overall gain using the same opamp schematic (neglecting the slew-rate limitation), the current and area consumption in the PGA is saved by 50% in total in the proposed PGA, by increasing β from 1/16 to 1/4. As shown in Fig. 3, when *RST_PGA* is on at $t_3(0)$, the opamp is unity-gain connected and V_{PGA} equals V_{REF}. At $t_4(0)$, *RST_PGA* turns off and the pixel is reset again. Due to charge balancing, $V_{PGA}=V_{REF}+C_1/C_2\cdot(V_{PIX,SIG}-V_{PIX,RST})$, indicating the gain of the PGA set by C_1/C_2 during the double sampling is negative, as $V_{PIX,SIG}<V_{PIX,RST}$. Between $t_4(0)$ and $t_3(T)$ is the conversion time T_{SAR} of the column-wise SAR ADC described in section II.A. T is the CIS's single row readout time. The frame conversion time would be $T\cdot N_{row}$, while N_{row} is the total number of rows in the array. The practical timing in rolling shutter in a 3T imager is more complex than that shown in Fig. 3, which is illustrative.

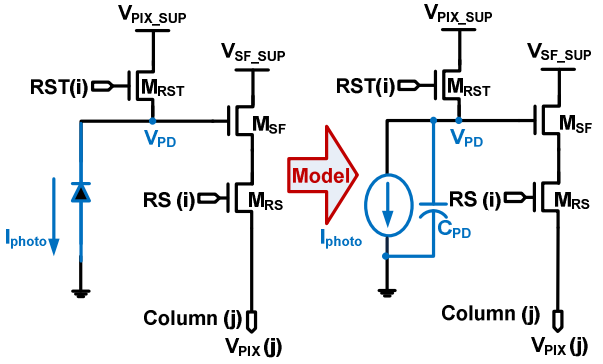


Fig. 2 The 3T pixel architecture in the proposed CIS.

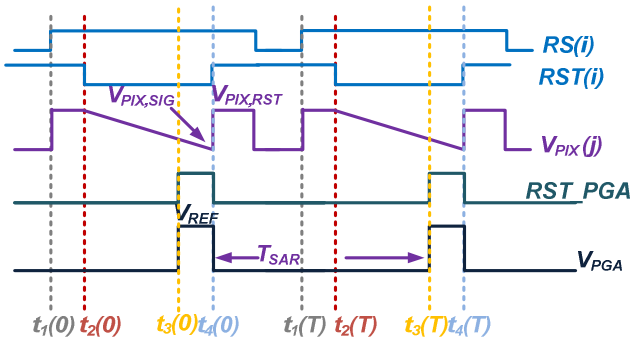


Fig. 3 The timing diagram of the pixel and its PGA in the proposed CIS.

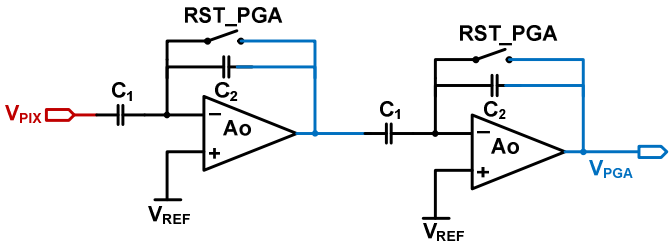
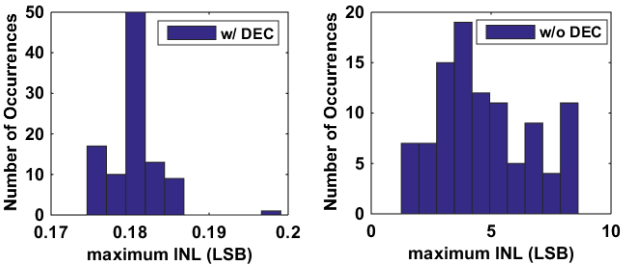


Fig. 4 The proposed PGA circuit schematic.

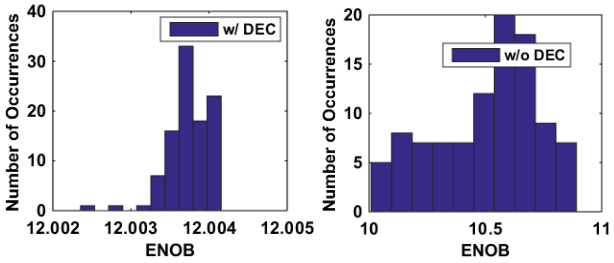
III. Simulation Results

A. SAR ADC with DEC

To demonstrate the effectiveness of the proposed DEC method shown in Fig. 1 (b), this paper models the bridged SAR ADC with and without DEC (Fig. 1 (a) and (b)) in MATLAB and adds uniformly distributed random numbers within ±1/32 of the total bit weight, as the comparator offset and the DAC settling errors, into the model. Fig. 5 shows the 100 Monte Carlo simulations of sine wave input for the SAR ADC models, with and without using the proposed DEC, respectively. With the DEC, both static and dynamic linearity (effective number of bits, ENOB) are improved, in their mean as well as standard deviations, compared to the case without using DEC, whose much larger worst case integration nonlinearity (INL) indicates a few missing codes. Cadence transistor level simulations are performed in 0.18 µm 3.3V CIS technology, using the schematics shown in Fig. 1 (a) and (b), respectively, with identical comparators, switches and unit capacitor sizes; their different logic and architectures are shown in Fig. 1. For fair comparison, the sampling rate for the two schematics is kept the same, at 13.3 MHz. τ is calculated to be around 0.8 ns~1.2 ns (unit cap 24 fF and the transmission gate switch size 4µm/0.35µm) for both designs while the settling time (for the DAC) for each step is 3.5 ns and 4.75 ns for the case with and without DEC, respectively. The former has less conversion time per bit as it has 4 redundant cycles but has to keep the same sampling speed. The input sine wave is at 17.9 kHz, with 0.8 Vpp. The designs are single-ended, due to the same nature of the CIS pixel outputs. Fig. 6 shows the simulation results. The case without using the proposed DEC method has its worst INL/differential nonlinearity (DNL) larger than 2 LSB, indicating a few missing codes, which are corrected by using the proposed DEC, gaining an additional 3 dB in SNDR, improved from 64.5 dB to 67.5 dB. The MATLAB simulations shown in Fig. 5 for the case without using the DEC method demonstrate even worse INL (instead of DNL as INL is more critical for CIS between the two) than its counterpart of the Cadence simulation results shown in Fig. 6, for most of the latter's 100 runs. The reasons are that the incomplete settling errors are randomly distributed within, rather than a fixed number of, $e^{-t/\tau}$. In other words, settling behavior is nonlinear and for this reason, the 100 runs of Monte Carlo simulation in MATLAB show a more statistical scenario than the Cadence simulation does.



(a)

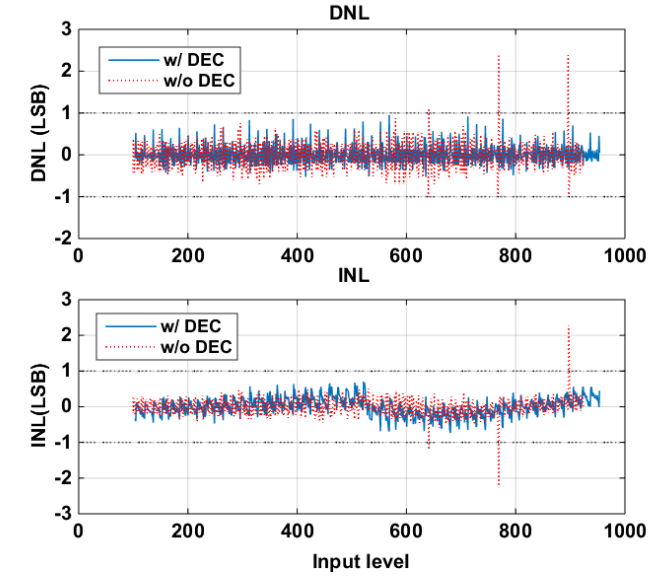


(b)

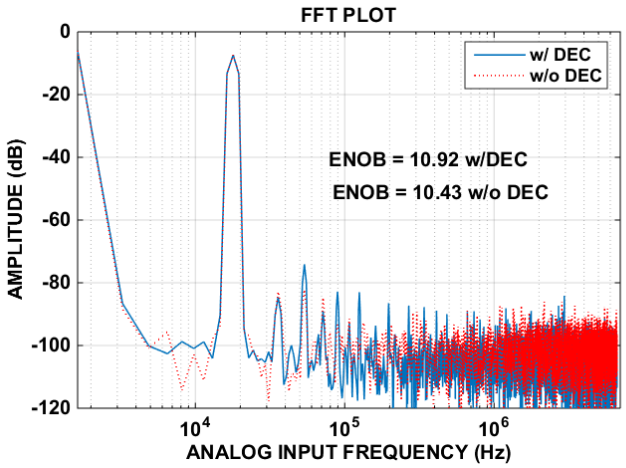
Fig. 5 Simulation results of static and dynamic linearity from 100 Monte Carlo runs for SAR ADCs using MATLAB, with ±1/32 random comparator offsets and incomplete settling errors: (a) worst case INL of SAR ADCs with and without using the DEC method. (b) ENOB of SAR ADCs with and without using the DEC method

B. Linearity of CIS

To verify the performances of the CIS (pixel and PGA readout by the column-level SAR with DEC), transistor level simulations have been performed in Cadence Virtuoso Environment. Under TT simulation corner, the telescopic opamp shown in Fig. 4 has a gain and UBW of 80 dB and 230 MHz with a load capacitor of 400 fF, which is the value of the PGA input capacitor C_1. The sampling time T labelled in Fig. 3 is 100 ns, which equals a column frequency of 10 MHz. The photodiode is modelled as a current in parallel to an ideal capacitance C_{FD} of 20 fF and increased linearly from 20 pA to 25 nA, in 1024 steps. This modelled photo current is converted into a pixel output voltage V_{PIX}, shown in Fig. 2 and amplified by the PGA into V_{PGA} shown in Fig. 4 (the nominal PGA gain is set to be 1). V_{PGA} is connected to V_{IN}, the SAR ADC input, as shown in Fig. 1 (b). Simulated SAR ADC outputs and their errors are shown in Fig. 7, indicating that the whole CIS has nonlinearity within ±0.07 %. In Fig. 7, the consistent ripples during shorter x-axis intervals are due to the quantization noise (errors) of the SAR ADC; while the curve trend is caused by the nonlinearity and increase of C_{GS} versus V_{PIX} (Fig. 4). However, in practice, C_{PD} decreases as V_{PD} increases.



(a)



(b)

Fig. 6 Simulation results of static and dynamic linearity using Cadence transistor level designs. (a) INL of SAR ADCs with and without using the DEC method. (b) Spectral response of SAR ADCs with and without using the DEC method

IV. Conclusions & Future Works

This paper proposes a CIS with 33% improved readout speed by applying DEC to its column-level SAR ADC. An alternative DEC method than the previous publications is proposed to correct for incomplete settling and comparator dynamic offset errors. It facilitates a 3 dB improvement in SNDR (from 64.5 dB to 67.5 dB) and missing code removal, when keeping the sampling rate, in transistor-level simulation results. It retains the straightforward timing diagram and digital logic as in a conventional binary SAR ADC and needs no digital compensation for any offset. The CIS as a whole, equipped with a 3T image pixel and a two-stage cascade PGA, and a column-level SAR ADC with DEC, is simulated to achieve nonlinearity less than 0.07 % within a dynamic range larger than 62 dB. Thanks to the proposed column SAR ADC, the CIS has a column readout rate of 10 MHz, which is faster than those around 2 MHz reported in previous publications [1][2], with a higher number of bits in ADCs, as shown in Table I. Although the proposed design has a smaller array, increasing the column or row count would never decrease the column readout rate, which is determined by the ADC conversion speed. The proposed CIS has been layout and submitted for fabrication in 0.18 µm CIS technology, and its single column occupies an area of 11 µm × 3000 µm, as shown in Fig. 8. With a power supply voltage of 3.3 V, the comparator in the SAR and two cascade opamps in the PGA consume a current of 130 µA and 145 µA, respectively. Further power saving can be obtained by lowering power supply level and using inverter based opamps, etc. The 4 redundant capacitors can be reduced to 2, using a more elaborate switch architectures that could connect them either to *GND*, V_{REF} or V_{CM}. The speed of the proposed SAR (or, the CIS) can be improved (scaled) further by using smaller capacitors or larger switches, which altogether lead to smaller τ, as the switches B0~B13's charge injection (absorption) will not add to *Vx*, while keeping the proposed DEC method. However, smaller capacitors would trade speed with noise, mismatches and calibration efforts. The pixel readout noise is simulated to be around 150 µV, mainly contributed by the SF's flicker noise and lower than the ½ LSB (~500 µV) of the 10-bit ADC.

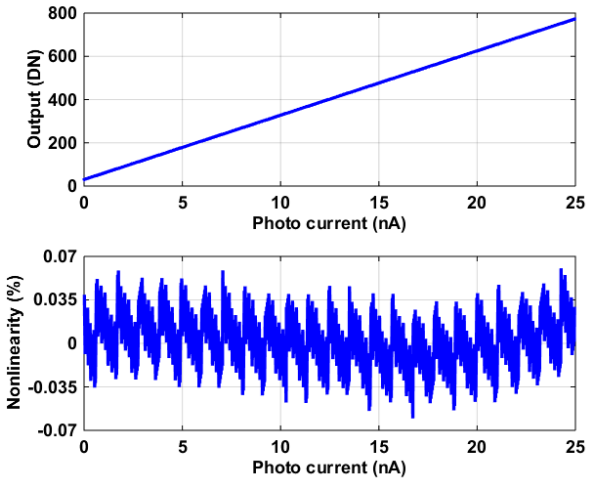


Fig. 7 Simulated linearity of the CIS, with the pixel output amplified by the PGA and then quantized by the proposed column bridged SAR with DEC.

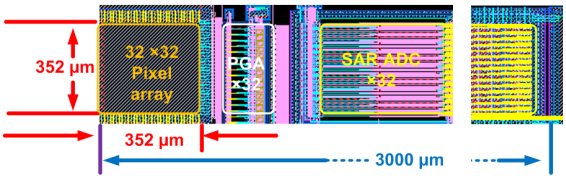


Fig. 8 Layout view of the proposed CIS.

Table I

	This work	[1]	[2]
Process	0.18 µm CIS 1P4M	0.15 µm CIS 1P3M	0.18 µm CIS 2P4M
Pixel pitch	11 µm	6 µm	32 µm
Array size	32 x 32	2560x 1440	400 x 250
Column rate	10 MHz	2 MHz	2 MHz
ADC speed	11 MHz	2 MHz	2 MHz
ADC resolution	10 bit	8 bit	N/A

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