sensors

MDPI

Article

Compensation for Process and Temperature Dependency in a CMOS Image Sensor

Shuang Xie [1,*] and Albert Theuwissen [1,2]

[1] EI Lab, Delft University of Technology, 2628 CD Delft, The Netherlands
[2] Harvest Imaging, 3960 Bree, Belgium; albert@harvestimaging.com
* Correspondence: s.xie@tudelft.nl

Received: 27 January 2019; Accepted: 17 February 2019; Published: 19 February 2019

Abstract: This paper analyzes and compensates for process and temperature dependency among a (Complementary Metal Oxide Semiconductor) CMOS image sensor (CIS) array. Both the analysis and compensation are supported with experimental results on the CIS's dark current, dark signal non-uniformity (DSNU), and conversion gain (CG). To model and to compensate for process variations, process sensors based on pixel source follower (SF)'s transconductance $g_{m,SF}$ have been proposed to model and to be compared against the measurement results of SF gain A_{SF}. In addition, A_{SF}'s thermal dependency has been analyzed in detail. To provide thermal information required for temperature compensation, six scattered bipolar junction transistor (BJT)-based temperature sensors replace six image pixels inside the array. They are measured to have an untrimmed inaccuracy within ±0.5 ^{0}C. Dark signal and CG's thermal dependencies are compensated using the on-chip temperature sensors by at least 79% and 87%, respectively.

Keywords: temperature sensors; delta-sigma (Δ-σ) modulator; CMOS image sensor (CIS); thermal compensation; dark current; dark signal non-uniformity (DSNU); process variability; process variations; conversion gain (CG)

1. Introduction

The pixels in a CMOS image sensor (CIS) array, as all semiconductor devices, are sensitive to process, voltage, and temperature (PVT) variations, which give rise to (Fixed Pattern Noise) FPN, including dark current or degraded conversion gain (CG) with temperature [1]. Voltage supply dependency and mismatches among source follower (SF)'s threshold voltages (V_{TH}) can be eliminated by correlated double sampling (CDS), a state-of-the art technique in CIS [1]. However, CDS cancels the offset rather than the gain mismatches. Earlier efforts to further suppress FPN's gain mismatch have been reported in [2], which adjusts both the gain and the offset in each digital pixel containing a 10 bit analog-to-digital converter (ADC). However, its 50 μm pixel pitch excludes its general usage in CIS and it does not consider any thermal effect on dark current or CG. To sense temperature inside a pixel array, previous publications [3,4] integrate seamless temperature sensors inside a CIS array despite no dark compensation being performed. Meanwhile, it is reported in [5] that the CG decreases with temperature, although the virtual mechanisms that contribute to the temperature dependency of pixel SF are not clearly defined. Besides, the work in [5] is incapable of compensating on-the-fly for linearity degradation with dynamic temperature change, not only because it has no temperature sensor on-chip, but also due to its linearity compensation method. In addition, [5] requires an accurate input light or voltage source for its algorithm. Reference [6] discusses the thermal dependence of Pinned Photodiode (PPD). In contrast to the aforementioned publications, this paper explores the possibilities to predict and compensate for process and temperature dependency without requiring any accurate input voltage or light source, in the following aspects: (1) Process

sensors based on pixel SF's transconductance $g_{m,SF}$ have been analyzed and measured, using column current biasing circuits with dynamic element matching (DEM). (2) SF's voltage gain A_{SF} is modeled based on the measured $g_{m,SF}$ from the process sensors in (1) and compared against its measurement results. Particularly, the mechanisms that contribute to the thermal and process dependency of A_{SF} have been fully analyzed and quantized, supported with its measurement results and extractions, using constant current and constant g_m biasing, respectively. (3) The CIS's CG and dark current's temperature dependency are measured and dynamically compensated using in-pixel temperature sensors. Using the six temperature sensors which are measured to have untrimmed inaccuracy within ±0.5 °C, the average dark signal's temperature dependency is compensated by at least 79%, and the CG by 87%. In general, this paper proposes self-calibrating the CIS using SF's own process element–$g_{m,SF}$, when employing DEM, thus eliminating any need for an accurate external voltage or light source. In other words, each of the image pixel's SF serves as a process sensor. The column readout circuits are 14 bit 1st-order delta-sigma ADCs (DSADC), which are less sensitive to process and temperature variations, due to their feedback loop, equaling their digital bit stream (bs) outputs to the analog inputs. Both the resolution and noise of the DSADC are less than 10 μV.

This paper is organized as follows. Section 2 discusses the theoretical thermal and process dependency of pixel SF's gain A_{SF} and transconductance $g_{m,SF}$, along with the process and the temperature sensors. Section 3 shows the measurement results of the temperature and the process sensors, and models the SF's A_{SF} using the process sensors' measured $g_{m,SF}$. The modeled A_{SF} is compared against A_{SF}'s measurement results, in relation to temperature and process variations. Section 4 shows the measurement results of CG and dark signal non-uniformity (DSNU), along with their thermally compensated results using the proposed in-pixel temperature and process sensors. Section 5 concludes this paper.

2. Pixel SF's Temperature and Process Dependency, Process Sensor, and Temperature Sensor

2.1. Pixel SF's Temperature and Process Dependency

Figure 1 shows a four-transistor pinned-photodiode (4T PPD) CIS pixel. In most CIS technologies, a pixel SF is different from its alternative outside the array, as each employs different mask layers from the other. For this reason, the product design kits (PDK) intended for SF outside the array were unsuitable to simulate the in-pixel SF. This statement will be supported with the measurement results of SF's V_{TH}, which were much lower than the normal value of around 700 mV, as will be shown in Section 3. The analysis in this section includes two types of biasing circuits for pixel SF: constant current and constant g_m biasing.

A pixel SF's gain A_{SF} can be expressed as [7]

$$A_{SF} = \frac{g_{m,SF}}{\left(g_{m,SF}+g_{mb,SF}\right)+\frac{1}{R_L}}, \quad (1)$$

where

$$g_{mb,SF} = \frac{\gamma \cdot g_{m,SF}}{2\sqrt{2\Phi_F+V_{SB}}}, \quad (2)$$

while source-body voltage $V_{SB} = V_{PIX}$ if neglecting the voltage drop on the Row Select (RS) switch, and V_{PIX} is positively correlated with the level of $g_{m,SF}$ [5]. R_L is the output impedance of the current source that provides I_1 in Figure 1. γ is often called the body-effect constant, and Φ_F is the Fermi potential of the body. $g_{mb,SF}$ is the transconductance associated with body effect. If neglecting $1/R_L$ in Equation (1), A_{SF} decreases as $g_{m,SF}$ falls, as $g_{mb,SF}$ decreases in a much slower rate than that of $g_{m,SF}$ due to the existence of Φ_F. The CG of a CIS can be expressed as

$$CG_{CIS} = CG_{FD} \cdot A_{SF}, \quad (3)$$

where $CG_{FD} = q/C_{FD}$, where C_{FD} is the total floating diffusing capacitance. Thus, the temperature and process dependency of A_{SF} can convert into that of the total conversion gain CG_{CIS}. Its process variations can cause FPN, such as DSNU. $g_{m,SF} = \sqrt{}(2\mu_n C_{ox} W/L \cdot I)$ where μ_n is the surface carrier

mobility, C_{ox} is the gate capacitance per unit area, W, L, and I are the width, length, and current of the SF, respectively. If the current I is designed to be constant, $g_{m,SF}$ decreases with temperature, as the thermal coefficient of the surface carrier mobility $\mu_n = \mu_0(T/T_0)^{-\alpha}$ where α is usually from 1.5 to 3 [8] and μ_0 is its value at absolute zero temperature. As a result, A_{SF} decreases with temperature as well. Therefore, if the A_{SF} can be predicted based on a simple measurement of the SF alone, it would help to define the CG_{CIS}'s temperature coefficient as well as its process variations in each pixel. For this reason, we propose a process sensor based on (i) the measurement of $g_{m,SF}$ and (ii) circuit simulation results of $1/R_L$. R_L is located outside the pixel array so has its PDK model, unlike those transistors inside the image pixel. Then, A_{SF} can be figured out using the aforementioned steps (i) and (ii).

2.2. Process Sensors

To calibrate A_{SF} as mentioned in Section 2.1, the proposed process sensor was based on the pixel SF itself, as shown Figure 1. Its timing diagram is shown in Figure 2. Between $t_1(0)$ to $t_1(T)$ is one conversion cycle; the same applies to $t_2(0)$ to $t_2(T)$, etc. During $T_{ADC,1}$ and $T_{ADC,2}$, the output voltage V_{PIX} that corresponds to $V_{GS,1}$ and $V_{GS,2}$, was quantized, sequentially. The row reset RST has to be on and its voltage level has to meet the condition of: $V_{RST} > V_{PIX} + V_{TH}$ (V_{TH} is the threshold voltage of M_{RST}) during the calibration mode. Then, the M_{SF} gate voltage V_{FD} equals that of V_{PIX_SUP} and the pixel output voltage $V_{PIX} = V_{PIX\_SUP} - V_{GS}$ (V_{GS} is the gate-source voltage of M_{SF}) if ignoring the voltage drop on M_{RS}. One has to ensure that TG is off to avoid disturbance into the V_{FD} node from any charge in the PPD.

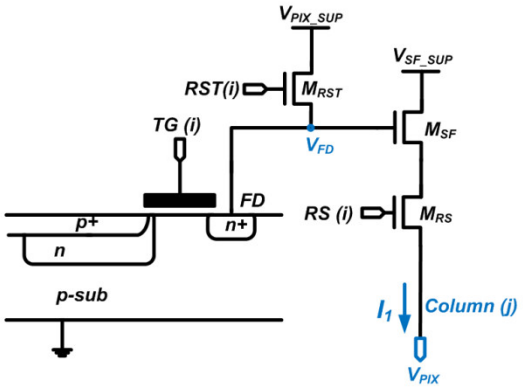

Figure 1. Schematic of four-transistor pinned-photodiode (4T PPD) image pixel based process sensor.

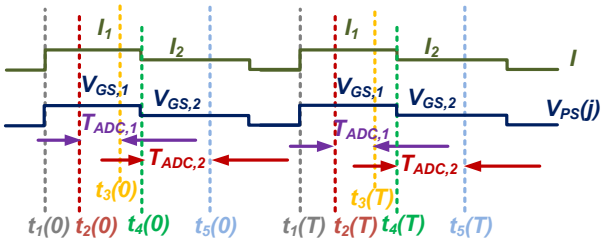

Figure 2. Proposed process sensor's timing diagram.

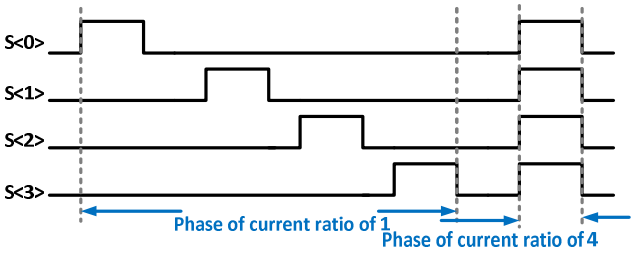

Figure 3. The dynamic element matching (DEM)'s timing diagram.

Therefore, the differential pixel output voltage ΔV_{PS} at V_{PIX}, when biased at sequential ratiometric currents $\Delta I = I_1 - I_2$, as shown in Figure 2, is

$$\Delta V_{PS} = V_{GS,2} - V_{GS,1} = \frac{\Delta I}{g_{m,SF}} \quad (4)$$

where $V_{GS,1,2}$ are the gate-source voltages of the SF during the ratiometric current biasing, respectively. From Equation (4), the value of $g_{m,SF}$ can be figured out through ΔV_{PS}, as shown in Figure 2. During $T_{ADC,1}$ and $T_{ADC,2}$, $V_{GS,1}$ and $V_{GS,2}$ were quantized by the column ADC, respectively, through the pixel output V_{PIX_SUP}–$V_{GS,1,2}$ instead of $V_{GS,1,2}$. To enhance the calibration accuracy of $g_{m,SF}$, a DEM current biasing was implemented, so that the SF can be biased with an accurate current level from 1 to 4. That is to say, the timing diagram shown in Figure 2 is simplified, as the practical calibration requires at least 15 phases to perform DEM with a ratio from 1 to 4. It was the DEM algorithm rather than the exact biasing current or voltage level that determined the accuracy of the calibration, as indicated by Equation (4). As a result, the calibrated $g_{m,SF}$ depends solely on the SF itself rather than on its biasing currents. For the next step, each pixel's current I_1 level will be calibrated without using the DEM. The calibration outputs from the two steps were combined together to compensate for process variations. The DEM's timing diagram is shown in Figure 3, with a DEM ratio of 4, for illustration purposes only. The practical DEM needs at least 15 phases. As the pixel output voltage (V_{PIX_SUP}–$V_{GS,1,2}$) changes with its biasing current, during I_1 and I_2, as shown in Figure 2, the SF's V_{TH} changes, due to its body effect. This change of SF's V_{TH}, ΔV_{TH}, was simulated to be around 10 mV at room temperature, and translates to 0.5% at an output voltage of 2 V. However, for two reasons this effect was made negligible. First of all, V_{TH} affects the process sensor in a closed loop manner with g_m and g_{mb}, both of which are functions of V_{TH}, as indicated in Equations (1) and (2). Secondly, both the process and the image sensors share the same SF. Therefore, the former can calibrate and compensate the latter.

2.3. Temperature Sensors

As discussed in Section 2.1, A_{SF} has a temperature coefficient. Therefore, a few (six, in this design) temperature sensors were implemented inside the pixel array to sense the temperature locally. It was initially proposed in [9] that a single bipolar junction transistor (BJT) device, as shown in Figure 4, can serve as a test circuit on-chip and upon this principle many publications are made [3,4,10]. This structure is ideal for an incorporated temperature pixel inside a CIS array, being small sized and insensitive to device mismatch (for only a single BJT). The above advantage, however, is paid at the expense of a degraded thermal sensing coefficient at higher temperatures, due to BJT's reverse Early effect, as mentioned in [9]. Nevertheless, this concern can be alleviated, as in this paper the temperature range of interest was until 80 °C, considering its application target in consumer electronics and its target sensing accuracy was 1 °C. As indicated in Figure 4, the differential pixel output ΔV_{BE} at column (j), when biased at sequential ratiometric currents, is

$$\Delta V_{BE} = \frac{kT}{q} ln(N) \quad (5)$$

where N is 4 in this design, which is the current ratio ensured by the DEM circuits shown in Figure 4. Compared to the previously published work in [3,4], the pMOS-based source follower (SF, for Q1) has been removed in this design for three purposes. First of all, Q1 or the entire cell's output impedance was approximately $1/g_{mQ}$, where g_{mQ} is the transconductance of Q1 and is normally at least 10 times larger than that of a MOS based SF of a similar current level. Secondly, the total temperature pixel area has been reduced to that of 1 pixel pitch, compared to 2 in [3,4]. Last but not least, a pMOS SF implemented in an n-well was acting as a parasitic photodiode and was lowering the quantum efficiency (QE) of the pixels. Specifically, a reverse biased diode (or, photodiode) existed between the n-well and the p-substrate, when the n-well was biased at a relatively high positive voltage. Furthermore, this parasitic photodiode gave rise to parasitic light sensitivity (PLS). Positive correlations between 1/PLS and QE were observed in [11]. Also, different from [3,4], in this work the BJT temperature pixels were readout by DSADCs, which are the state-of-the-art quantization

circuitries for temperature sensors. Compared with the programmable gain amplifier (PGA)/CDS readout circuits employed in [3,4], the DSADC alternative in this paper has much less thermal curvature as well as noise, with the additional benefits of oversampling and noise shaping and a similar if not smaller area.

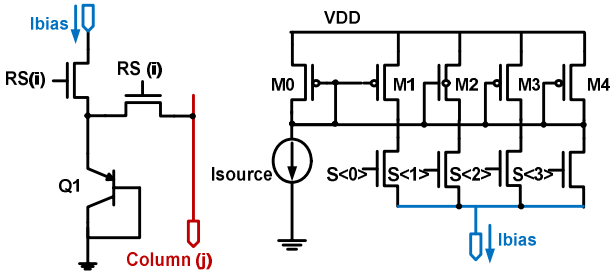

Figure 4. Schematic of in-pixel bipolar junction transistor (BJT)-based temperature sensor and its current biasing with DEM. M0~M4 are in practice cascode devices.

3. Measurement Results of SF's Temperature and Process Dependency, Temperature, and Process Sensors

The measurements in this paper were performed on a 64 × 64 image pixel array prototype, as shown in Figure 5, fabricated in a 0.18 μm CIS technology. However, for reasonable results on process variability, only the center 32 × 52 pixels were used for data processing.

3.1. Pixel SF's Temperature and Process Dependency

The pixel SFs' transconductance $g_{m,SF}$ were measured using the process sensors described in Section 2.2, with constant current biasing. The measurement results of average $g_{m,SF}$ of all pixels are shown in Figure 6, from which several observations can be made, as follows. (1) The $g_{m,SF}$ decreases with temperature and increases with current biasing. (2) The $V_{GS,SF}$ increases with temperature. Both observations were mainly due to degradation in surface carrier mobility μ_n with temperature: (1) can be explained by $g_{m,SF} = \sqrt{(2\mu_n C_{ox} W/L \cdot I)}$, (2) was caused by $V_{GS} - V_{TH} = \sqrt{[2I/(\mu_n C_{ox} W/L)]}$. Here one might notice that V_{TH} normally has a negative temperature coefficient. However, a pixel SF V_{TH}'s temperature dependence is negligible (at least in our design), compared to that of μ_n, as shown in the extraction of Figure 7, especially when the current I is reasonably large (which is often the case as speed is crucial for a CIS pixel). In Figure 7, the threshold voltage V_{TH} was extracted using 2nd order best curve fitting of the I-V curve and $\mu_n C_{ox} W/L$ is exacted assuming $I = 1/2\mu_n C_{ox} W/L \cdot (V_{GS} - V_{TH})^2$, both using the results shown in Figure 6. What is also shown in Figure 7 is the 3 sigma (σ) process variability for both parameters. Figure 8 shows the thermal and process dependency of $g_{m,SF}$, V_{TH}, and $\mu_n C_{ox} W/L$.

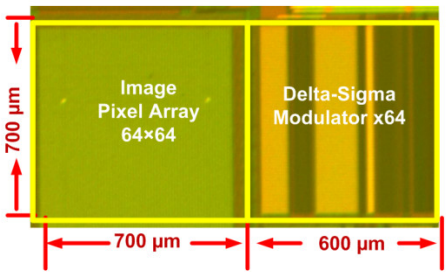

Figure 5. Chip micrograph of the CMOS image sensor (CIS) under test.

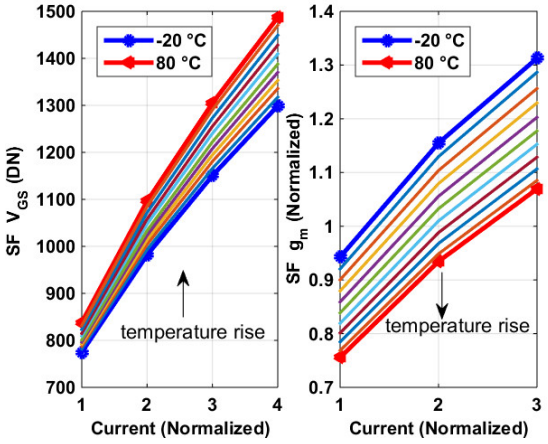

Figure 6. Measurement outputs of the process sensors (**left**) and their extracted $g_{m,SF}$'s temperature dependency (**right**), with constant current biasing.

The SF's transconductance $g_{m,SF}$ was also measured with a different type of current biasing–constant g_m, whose results are shown in Figure 9. Compared to its alternative using constant current biasing, this measurement, which has identical pixel architecture, has the following characteristics: (1) The temperature coefficient of the $g_{m,SF}$ is slightly positive. This agrees with the circuit design of constant g_m biasing. (2) The $V_{GS,SF}$ increases with temperature. Compared to the alternative using constant current biasing, its $V_{GS,SF}$'s temperature coefficient must be larger. The constant g_m biasing's actual current level and temperature coefficient were extracted based on the following assumptions: when biased with the same amount of current at the same temperature, the pixel output voltage should be the same for both measurements (constant current and constant g_m), as the SFs themselves (as well as the image pixels) were of identical design and layout. Figure 10 shows the experimental extracted current which more than doubles over the temperature range of –20 to 80 °C.

3.2. Process Sensor and SF Voltage Gain A_{SF}

The SF voltage gain A_{SF} was modeled using the on-chip process sensors' measurement results (the extracted g_m as shown in Figures 6 and 8), with the additional aid of the transistor-level simulated output impedance R_L from Cadence, for the constant current and constant g_m biasing, respectively. They were compared against the measurement results of A_{SF}, which were obtained with decreasing V_{PIX_SUP} voltage, as shown in Figure 11. It should be noted that the measurement of A_{SF} was not essential to the function of the proposed process sensors, but being so enabled the verification of the process sensors' functions. It can be seen, from the measurement results shown in Figure 11, that the proposed process sensors can model A_{SF} as accurately as 99%.

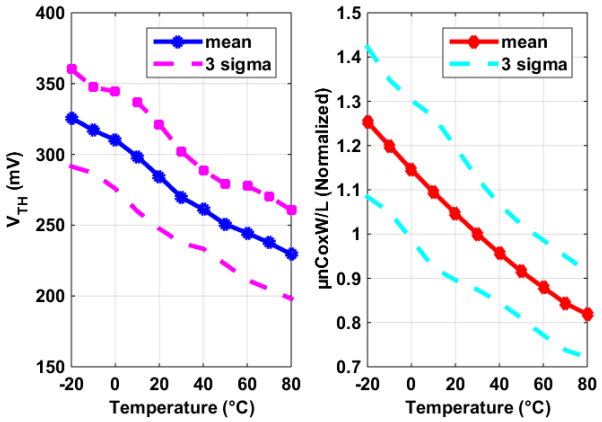

Figure 7. Extracted threshold voltage V_{TH} (**left**) and $\mu_n CoxW/L$ (**right**), from the measurement results of Figure 6.

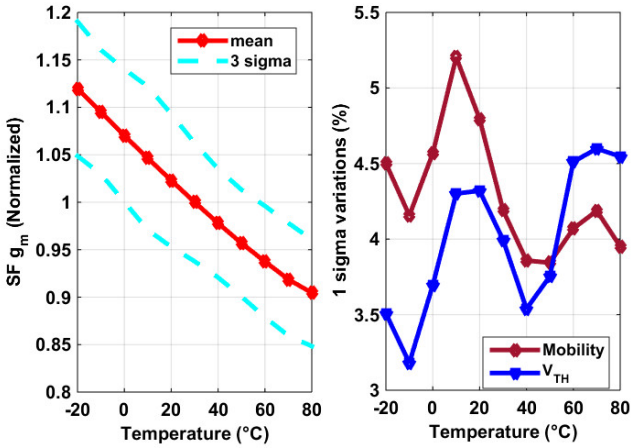

Figure 8. Measurement results of the SF $g_{m,SF}$'s temperature dependency (**left**) and the process variability of threshold voltage V_{TH} and $\mu_n CoxW/L$ (**right**) in Figure 7, using constant current bias.

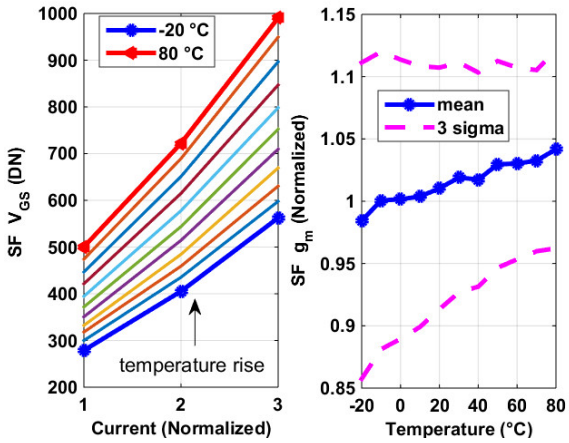

Figure 9. Measurement results of the SF $g_{m,SF}$'s temperature dependency (**left**), with constant g_m biasing (**right**).

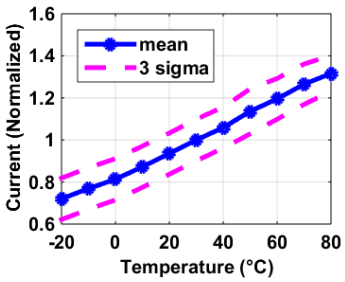

Figure 10. Extracted current level and temperature dependency in a constant g_m biasing circuit using the measurement results of the SF's $g_{m,SF}$ in Figures 6 and 9.

The fact that a temperature dependency of 20% of $g_{m,SF}$ in Figure 6 translates to that of 0.2% of A_{SF} in Figure 11 is not surprising, considering the loop gain $(g_{m,SF} + g_{mb,SF}) \cdot R_L$ in Equation (1) is normally larger than 100 with cascode bias (e.g., 130 in our design at room temperature). The degradation of A_{SF} in the closed loop is mainly from two sources. First, the decrement of R_L for both biasing conditions. $R_L \approx g_m \cdot r_o^2$ (where g_m and r_o are the transconductance and output impedance of the cascode

and of both transistors in the biasing, respectively). For constant I biasing, the degradation in R_L was mainly due to that in g_m (lower μ_n as temperature rises) and for constant g_m biasing, mostly caused by that in r_o (due to increased current with temperature, as shown in Figure 10). Second, the relative increment of g_{mb} to g_m, due to decreased V_{SB} in Equation (2), was caused by increased V_{GS}. The process variability of A_{SF}, as shown in the right graph of Figure 11 decreases with temperature for both biasing conditions. The explanations are the increment of (V_{GS}–V_{TH}) with temperature decreases mismatches in the biasing circuits as in a current source [12], for both cases. This explanation was further validated by the fact that in Figure 11 the constant g_m biasing's process variations decrease faster at higher temperatures, due to the same trend in its (V_{GS}–V_{TH}), compared to its constant current alternative.

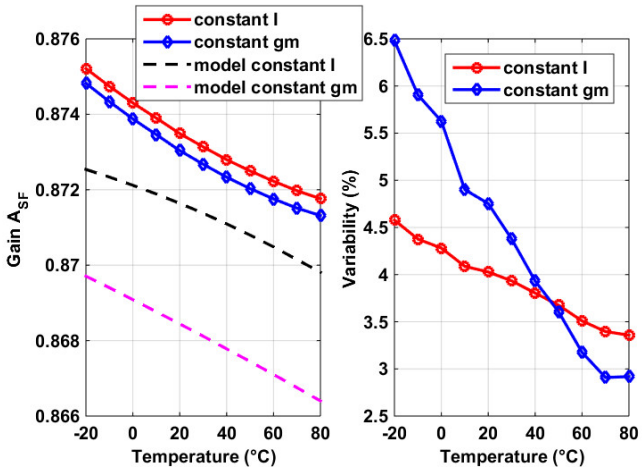

Figure 11. (**Left**): Measurement results of the A_{SF} and its temperature dependency (**left**), compared with its modeled results using the process sensors' $g_{m,SF}$, for the constant current and constant g_m bias circuits, respectively. (**Right**): The 1 σ process variability of measured A_{SF}

3.3. Measurement Results of BJT Based Temperature Sensors

The measurement results of the six in-pixel BJT based temperature sensors are shown in Figure 12. Each, untrimmed (uncalibrated) and upon a 2nd order master curve fitting, achieves measured inaccuracies within ±0.5 °C. The 3 σ inaccuracies of all sensors were within ±1.1 °C.

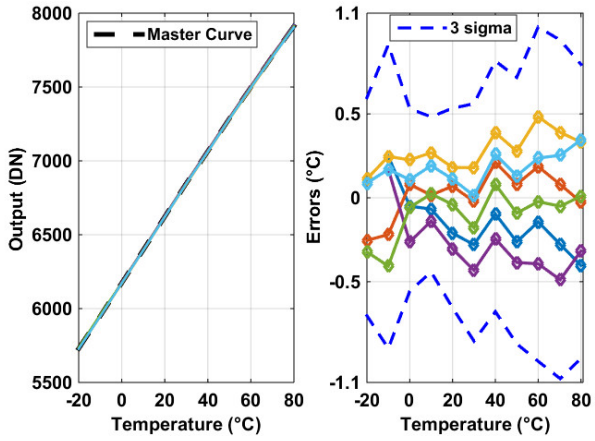

Figure 12. Measurement results of the six incorporated BJT-based temperature sensors inside the pixel (**left**) and their untrimmed errors, with 3 σ inaccuracies, upon a global 2nd order curve fitting (**right**).

3.4. PGA/CDS and Constant Voltage Bias

In this design, the column readout circuit was a DSADC, which has a minimum temperature dependency. However, in many other CISs, the readout circuits, e.g., the PGA/CDS circuits may be subject to a temperature dependency as well. Nowadays, the biasing circuits are mostly constant g_m ones. Therefore, for an open loop opamp, its input pair's g_m may stay almost constant, but its output impedance drops, due to the increased biasing current level to accommodate for the constant g_m at higher temperature, analogous to that shown in Figure 10. The usual consequences are the opamp's open loop gain decreases with temperature [13]. Our chip has also implemented some column-level PGA/CDS circuits, which were not employed for any measurement in this paper except in Figure 13 which shows its temperature dependency was negative. This was because the closed loop PGA gain drops as temperature increases. However, the level of any opamp's thermal dependency is subject to its architecture (e.g., telescopic, folded cascode), design parameters, as well as how well the closed loop opamp settles within the measured time. In addition, the closed loop gain was proportional to feedback factor β, which is the 1/Gain,PGA, where Gain,PGA is the PGA gain (e.g., 8 or 18 dB). Therefore, the larger the PGA gain, the faster the closed loop gain degrades with temperature, for identical opamp design and settling time. Meanwhile, its closed loop unity-gain bandwidth (UBW) decreases (with feedback factor β) so the settling errors within the same period increases, at the same time the closed loop gain drops, when temperature rises.

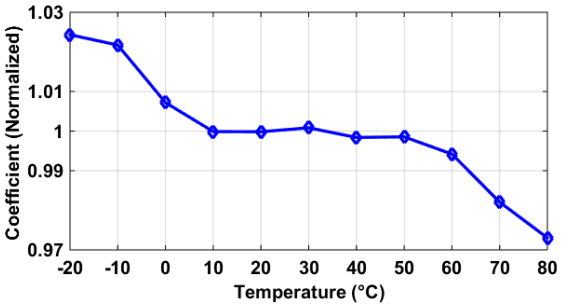

Figure 13. Measured temperature coefficient of a programmable gain amplifier (PGA)/correlated double sampling (CDS) circuits implemented on the same CIS chip, with a PGA gain of 8, a settling time of 1 μs, and an unity-gain bandwidth (UBW) of 10 MHz at room temperature. This PGA/CDS circuit was not used for any other measurement in this paper.

Another concern was when the pixel SF was biased by a constant voltage common source transistor as in [5]. Generally speaking, as the constant voltage V_{GS} of an nMOS transistor increases, its current's temperature dependency changes from positive to negative [14], as shown in Figure 14. This is because $I = 1/2\mu_n C_{ox} W/L\ (V_{GS}-V_{TH})^2$, where the mobility μ_n and threshold V_{TH} are against each other in their thermal effects on I. When V_{GS} is small, the portion of $(V_{GS}-V_{TH})$'s thermal influence is larger than that of μ_n and vice versa. An extreme condition is that for a logic delay line, where $V_{GS} = V_{DD}$, the biasing current's temperature coefficient is negative (with reasonably large V_{DD}), and its propagation delay (affected by biasing/charging currents) generally increases with temperature [8]. The situations of bias currents having zero or positive temperature dependencies have been discussed in Section 3.1, and its SF gain A_{SF} decreases slightly, to be around 0.3% over 100 °C of temperature rise, using cascode current sources.

In general, the loop gain of common source bias $g_{m,SF} \cdot r_o = 2/\lambda(V_{GS,SF} - V_{TH})$ decreases with temperature. Since $g_{m,SF} = 2I/(V_{GS,SF} - V_{TH})$, and $r_o = 1/\lambda I$ (λ is output impedance constant), so the open loop gain of single transistor common source bias $g_{m,SF} \cdot r_o = 2/\lambda(V_{GS,SF} - V_{TH})$. The reason for the negative thermal dependency of loop gain is that $V_{GS}\text{-}V_{TH} = \sqrt{[2I/(\mu_n C_{ox} W/L)]}$ increases with temperature due to decreased μ_n, invariant of the type of current source, unless the temperature coefficient of I is larger than that of μ_n, which can rarely be the case, for the following reasons. Increased V_{GS} level in the current source transistor raises the minimum saturation level of the pixel. In other words, a higher V_{GS} level limits the linear dynamic range. Also, at least in our design, the fact that the thermal coefficient of V_{TH} in the bias transistor was much larger than the pixel transistor makes it less possible for the thermal coefficient of I to be more negative than that of μ_n. Therefore, the temperature

dependence of A_{SF} was almost always negative, despite the variations in bias circuit type. If the bias circuit is a cascode current mirror, the loop gain $(g_{m,SF} + g_{mb,SF}) \cdot R_L \approx g_m^2 \cdot r_o^2$ is normally around 100, by which factor the thermal coefficient of $g_{m,SF}$ is suppressed when it constitutes A_{SF}, which ends up having a temperature dependency of less than 0.4% negatively. However, if the bias current circuit is a single rather than a cascode transistor, as in [5], the thermal coefficients of Equation (1) can be 10 times as large, to be around –3% or –5% over 100 °C. In addition, when there is a PGA that follows the pixel outputs, CG can degrade faster with temperature, especially with a larger PGA gain.

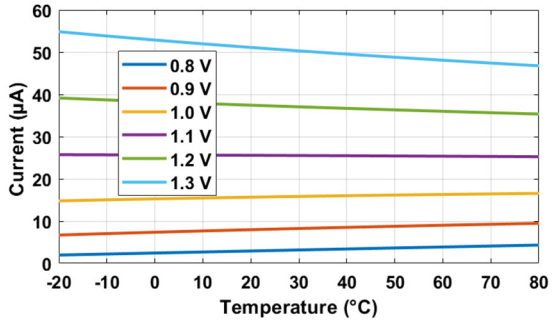

Figure 14. Simulation results of the current in an nMOS transistor biased with constant V_{GS} voltage: when V_{GS} increases from 0.8 V to 1.3 V, its current's temperature coefficient goes from positive to negative.

4. Measurements and Compensation of Process and Temperature Dependency in a CIS

4.1. Conversion Gain (CG)

The CG of a CIS as a function of temperature, using the constant current SF biasing, was measured and shown in Figure 15. The measured thermal dependency was around negative 5% over the measured temperature range of 100 °C. Taking into consideration that the thermal dependencies of SF were around 0.4% (last section), the 5% negative thermal coefficient of CG was mostly contributed by the positive thermal coefficient of the C_{FD}, due to increased $1-A_{SF}$ that raised the miller capacitance associated with SF. However, various parasitic capacitors that are thermally sensitive constitute C_{FD} [5]. In addition, the charge transfer was a transient process depending on temperature-dependent voltage levels related to Pinned Photodiode (PPD), Floating Diffusion (FD), and Transmission gate (TX) [5,6]. On the other hand, this paper specifically focuses on the thermal dependency of the SF transistor rather than all pixel voltage nodes' thermal dependency. The reason is that this part–SF has a strong correlation with column process variability and is thermally predictable, so that can be compensated despite batch, process, or design parameter variations, compared to the rest. In this design, the thermal coefficient of CG can be modeled by an accuracy as fine as 0.5%, as shown in the bottom figure in Figure 15.

To test the design's capability to compensate for dynamic temperature change, both the temperature and the image pixels were measured at the same time. Figure 16 shows the measurement results of the aforementioned experiments. Measurements were done while all sensors were heated up from 20 to 60 °C in a temperature chamber, gradually. The image sensors' outputs drop with time, caused by temperature drift, giving rise to more than 2% of non-linearity, which has been compensated using the thermal information provided by the temperature sensors whose outputs increase with time.

Among the 2.3% of thermal induced nonlinearity, 2% was corrected, to be less than 0.3% eventually. That was an 87% improvement, compared to the case without using the on-chip temperature sensors for dynamic thermal compensation.

4.2. Dark Current and DSNU

On one hand, the DSNU in a 4T PPD pixel is caused by variations among dark currents from pixel to pixel [1]. On the other, the average dark current dependency on the temperature of a CIS array fabricated using the same pixel architecture and readout circuits can be predicted by an exponential fit ($y = a{\cdot}exp(b{\cdot}T)$), where T refers to the temperature and a, b are constants. Figure 17 shows the measured average dark current from three chips and their global exponential fit. It also shows the derivations between the measurements and their fit were within in ±17% for three chips. In this way, the average dark current can be predicted and compensated with an accuracy of at least 83%. The average dark current was measured to be around 30 e^-/s at room temperature and doubled almost for every 6 °C of temperature rise.

Figure 18 shows the dark signal histogram when a dark frame was taken at 60 °C and 250 ms. Originally, the average dark signal and DSNU were 2118 DN and 141 DNrms. Upon cancelling the image offset with a reference image taken at room temperature, the DSNU was reduced by 10 DNrms to 131 DNrms. With the additional aid of the average dark signal's temperature fit shown in Figure 17, dark signal was reduced by 79% to 446 DN. The method of "w/temp comp", facilitated with in-pixel temperature sensors and with an additional aid of a dark frame captured at room temperature, eliminated the need to capture a dark frame before each image, thus improving the readout speed and getting rid of a physical shutter.

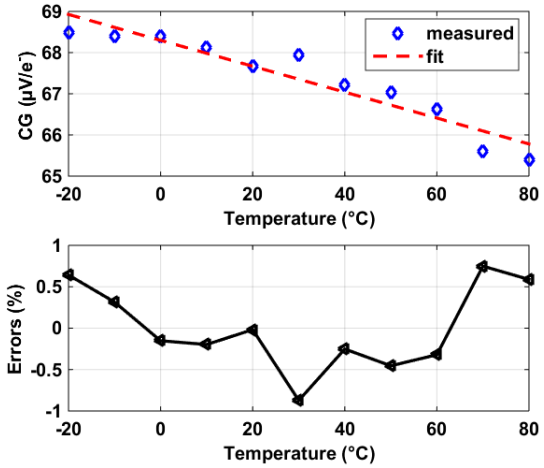

Figure 15. Measured conversion gain (CG) versus temperature in our CIS (**top**) and the deviations between the measurements and their fit (**bottom**).

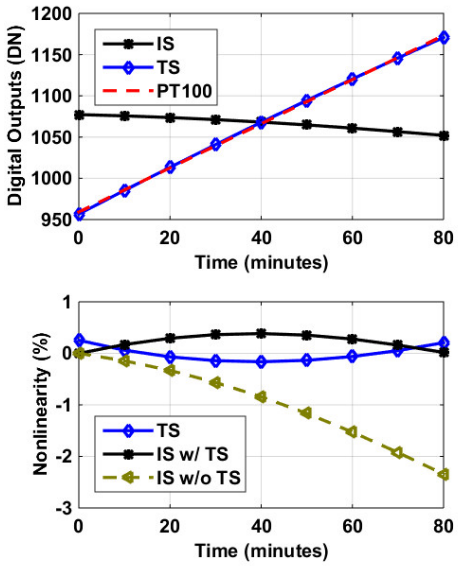

Figure 16. Top: Measured image sensor (IS) and temperature sensor (TS) outputs versus time, along with a reference temperature sensor (PT100). Bottom: when the temperature changes from 20 to 60 °C gradually in a temperature chamber, nonlinearity caused by the thermal drift (IS w/o TS) was corrected with the temperature information provided by the on-chip TS (IS w/TS). The correction was done digitally and on-the-fly.

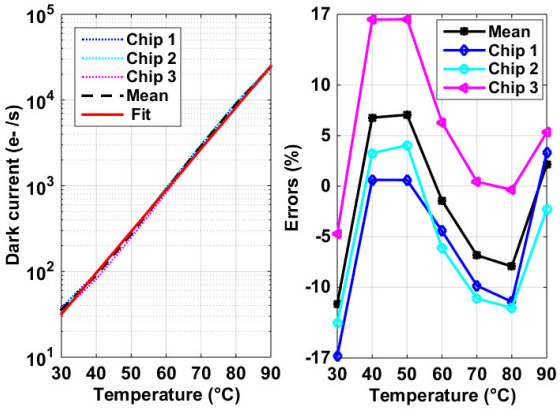

Figure 17. Measured average dark current for three chips and their exponential fit (**left**) and deviations from the exponential fit (**right**).

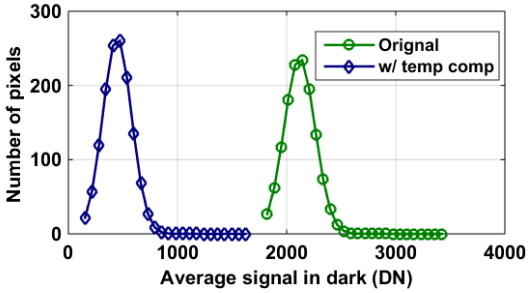

Figure 18. Histogram of measured dark signal and dark signal non-uniformity (DSNU). Original: measured at 60 °C and 250 ms, averaged 100 frames; w/ temp comp: compensation by subtracting the reference dark current at room temperature, along with predicted dark current using temperature information (as shown in Figure 17).

5. Conclusions

This research paper analyzes and compensates for the process and the temperature dependency in a CIS image sensor, facilitated with the temperature and the process sensors implemented inside the image pixel array. Compared to previous publications, the new features of this paper are as follows. (1) The proposed process sensors were based on measuring the imager pixel's SF $g_{m,SF}$ and were verified against the measurement results of A_{SF}, in a 32 × 52 pixel array. (2) The process and thermal variations of A_{SF} were measured while those of V_{TH}, $g_{m,SF}$, and A_{SF} were extracted using measurement results. Especially, the sources contributing to thermal dependence of A_{SF} have been analyzed, for various cases, from constant current and constant g_m biasing current sources, to the general situation of a constant voltage bias. The conclusions are that if one can afford a cascode current biasing, A_{SF}'s temperature dependency would be less than 0.5% over a temperature range of 100 °C, due to the loop gain around 100 that biases the SF. Otherwise, if a single transistor is employed as a current source, A_{SF}'s temperature dependency can be ten times as large, to be negative 5% over the same temperature range. (3) The thermal dependency of CG was measured to drop around 5% over 100 °C of temperature change, mainly attributed to that of C_{FD} rather than that of A_{SF}. (4) The proposed incorporated BJT-based temperature sensor occupies an area of 11 × 11 μm, and provides an untrimmed accuracy better than ±0.5 °C over the temperature range between −20 and 80 °C.

Compared to previous publications on temperature sensors as listed in Table 1, the advantages of our temperature sensors are a much smaller area, better untrimmed accuracy, and reasonable figure of merit (FOM) [17]. Using the temperature information provided by the temperature sensor, the non-linearity of the CIS outputs caused by thermal drift of CG can be corrected by more than 87%. The average dark current can be predicted by at least 83% and dark signal can be compensated by at least 79%, respectively.

In summary, the measurement results obtained, and the methods proposed in this paper may serve as guidelines, rather than the ultimate solutions to compensate for thermal and process dependencies for CIS. Figure 19 shows an image taken by our low-resolution prototype CIS. In the future, a larger size array is planned to be measured for better understanding of process variability in practical image sensors.

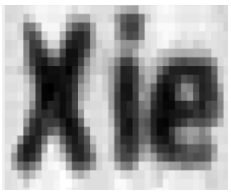

Figure 19. An image taken by part of the CIS (64 × 27), with constant current bias.

Table 1. Summary of performances

	This work	**[15]**	**[16]**
Sensor Type	BJT	BJT	MOS
CMOS Technology	0.18 μm	0.13 μm	28 nm
Area (μm²)	121	60,000	1000
Temperature Range	−20 °C to 80 °C	−20 °C to 100 °C	−5 °C to 85 °C
3 σ accuracy	±1.1 °C	−1.7/1.26 °C	−3.3/1.9 °C
Calibration	Un-trimmed	Two-point	One-point
Power Consumption (μW)	36	744	56
Conversion Time (ms)	16	13.3	0.036
Resolution (°C)	0.09	0.187	0.76
Resolution FOM (nJ·K²)[a]	4.6	346	1.2
Rel.IA (%)[b]	2.2	2.4	5.8

[a] Energy/Conversion × (Resolution)², in reference to [17], [b] 3 σ accuracy/temperature range, in reference to [17].

Author Contributions: Conceptualization, S.X. and A.T; methodology, S.X.; software, S.X.; validation, S.X., formal analysis, S.X.; investigation, S.X.; resources, S.X. and A.T.; data curation, S.X.; writing—original draft preparation, S.X.; writing—review and editing, A.T.; visualization, S.X.; supervision, A.T.; project administration, A.T.; funding acquisition, A.T.

Funding: The research is part of the CISTERN and EXIST project, funded by the Dutch government through the Horizon 2020 and Penta EU-initiatives.

Acknowledgments: The authors acknowledge the support of TowerJazz in realizing the prototype CIS devices. The authors would like to thank Prof. Makinwa for advice, Xiaoliang Ge for image pixel design, Accel Abarca Prouza for the test PCB, Zuyao Chang and Lukasz Pakula for the measurement setups. We would like to thank the editors and reviewers for their valuable comments.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Wang, X. Noise in Sub-Micron CMOS Image Sensors. Ph.D. Thesis, TU Delft, Delft, The Netherlands, 2008; pp. 46–68.
2. Margarit, J.M.; Vergara, G.; Villamayor, V.; Gutiérrez-Álvarez, R.; Fernández-Montojo, C.; Terés, L.; Serra-Graells, F. A 2 kfps Sub-μW/Pix Uncooled-PbSe Digital Imager With 10 Bit DR Adjustment and FPN

Correction for High-Speed and Low-Cost MWIR Applications. *IEEE J. Solid-State Circuits* **2015**, *50*, 2394–2405, doi:10.1109/JSSC.2015.2464672.
3. Xie, S.; Abarca, A.; Markenhof, J.; Ge, X.; Theuwissen, A. Analysis and calibration of process variations for an array of temperature sensors. In Proceedings of 2017 IEEE SENSORS, Glasgow, Scotland, UK, 29 October–1 November 2017; pp. 1–3.
4. Abarca, A.; Xie, S.; Markenhof, J.; Theuwissen, A. Integration of 555 temperature sensors into a 64 × 192 CMOS image sensor. *Sens. Actuators A Phys.* **2018**, *282*, 243–250, doi:10.1016/j.sna.2018.09.029.
5. Wang, F.; Theuwissen, A.J.P. Temperature Effect on the Linearity Performance of a CMOS Image Sensor. *IEEE Sens. Lett.* **2018**, *2*, 1–4, doi:10.1109/LSENS.2018.2860990.
6. Sarkar, M.; Büttgen, B.; Theuwissen, A.J.P. Temperature Effects on Feedforward Voltage in Standard CMOS Pinned Photodiodes. *IEEE Trans. Electron Devices* **2016**, *63*, 1963–1968, doi:10.1109/TED.2016.2544814.
7. Wang, F.; Han, L.; Theuwissen, A.J.P. Development and Evaluation of a Highly Linear CMOS Image Sensor With a Digitally Assisted Linearity Calibration. *IEEE J. Solid-State Circuits* **2018**, *53*, 2970–2981, doi:10.1109/JSSC.2018.2856252.
8. Ha, D.; Woo, K.; Meninger, S.; Xanthopoulos, T.; Crain, E.; Ham, D. Time-Domain CMOS Temperature Sensors With Dual Delay-Locked Loops for Microprocessor Thermal Monitoring. *IEEE Trans. Very Large Scale Integr. Syst.* **2012**, *20*, 1590–1601, doi:10.1109/TVLSI.2011.2161783.
9. Pertijs, M.A.P.; Huijsing, J.H. *Precision Temperature Sensors in CMOS Technology*; Springer: Dordrecht, The Netherlands, 2006; pp. 213–225.
10. Vosooghi, B.; Lu, L. 5 × 5 scattered temperature sensor front-end based on single-diode with non-trimmed ±0.7°C 3σ relative inaccuracy. *Electron. Lett.* **2014**, *50*, 1806–1808, doi:10.1049/el.2014.2915.
11. Yokoyama, T.; Tsutsui, M.; Suzuki, M.; Nishi, Y.; Mizuno, I.; Lahav, A. Development of Low Parasitic Light Sensitivity and Low Dark Current 2.8 μm Global Shutter Pixel. *Sensors* **2018**, *18*, 349, doi:10.3390/s18020349.
12. Carusone, T.C.; Johns, D.A.; Martin, K.W. *Analog Integrated Circuit Design*; Wiley: Hoboken, NJ, USA, 2012; pp. 100–101.
13. Zhang, M.; Noh, K.; Fan, X.; Sánchez-Sinencio, E. A Temperature Compensation Technique for a Dynamic Amplifier in Pipelined-SAR ADCs. *IEEE Solid-State Circuits Lett.* **2018**, *1*, 10–13, doi:10.1109/LSSC.2018.2794783.
14. Xie, S.; Ng, W.T. A 0.02 nJ self-calibrated 65nm CMOS delay line temperature sensor. In Proceedings of the 2012 IEEE International Symposium on Circuits and Systems (ISCAS), Seoul, Korea, 19–23 May 2012; pp. 3126–3129.
15. Tang, Z.; Tan, N.N.; Shi, Z.; Yu, X. A 1.2V Self-Referenced Temperature Sensor with a Time-Domain Readout and a Two-Step Improvement on Output Dynamic Range. *IEEE Sens. J.* **2018**, *18*, 1849–1858, doi:10.1109/JSEN.2017.2786735.
16. Cochet, M.; Keller, B.; Clerc, S.; Abouzeid, F.; Cathelin, A.; Autran, J.; Roche, P.; Nikolić, B. A 225 μm2 Probe Single-Point Calibration Digital Temperature Sensor Using Body-Bias Adjustment in 28 nm FD-SOI CMOS. *IEEE Solid-State Circuits Lett.* **2018**, *1*, 14–17, doi:10.1109/LSSC.2018.2797427.
17. Makinwa, K. Smart Temperature Sensor Survey. Available online: https://ei.tudelft.nl/smart_temperature/ (accessed on 10 September 2018).