Pixel Optimizations and Digital Calibration Methods of a CMOS Image Sensor Targeting High Linearity

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***Abstract*— In this paper, different methodologies are employed to improve the linearity performance of a prototype CMOS image sensor (CIS). First, several pixel structures, including a novel pixel design based on a capacitive trans-impedance amplifier (CTIA), are proposed to achieve a higher pixel-level linearity. Furthermore, three types of digital linearity calibration methods are explored. A prototype image sensor designed in 0.18-μm, 1-poly, and 4-metal CIS technology with a pixel array of 128 × 160 is used to verify these linearity improvement techniques. The measurement results show that the proposed CTIA pixel has the best linearity result out of all pixel structures. Meanwhile, the proposed calibration methods further improved the linearity of the CIS without changing the pixel structure. The pixel mode method achieves the most significant improvement on the linearity. One type of 4T pixel attains a nonlinearity of 0.028% with pixel mode calibration, which is two times better than the state of the art. Voltage mode (VM) and current mode (CM) calibration methods get rid of the limitation on the illumination condition during calibration operation; especially, CM calibration can further suppress the nonlinearity caused by the integration capacitor C_{FD} on the floating diffusion node, which is remnant in VM.**

***Index Terms*— CMOS image sensor, pixel, linearity, CTIA, calibration.**

I. Introduction

HIGHLY linear image sensors are important for a broad range of applications, such as medical and scientific imaging [1]–[3]. In the past few years, many studies have been conducted on linearizing the radiance response of a CMOS image sensor [4]–[9].

In previous studies, the factors which contribute to the nonlinear errors of the CIS are discussed [10]. The nonlinearity of the pixel usually dominates the nonlinear errors of the CMOS image sensor as a whole. In a traditional 4T pixel, the nonlinear gain of the source follower (SF) and the voltage dependency of the integration capacitor C_{FD} on the FD node contribute the most to the nonlinearity of the pixel [10].

Pixel-level linearity optimization is the most direct way of reducing the nonlinearity of the CIS. A novel pixel design is proposed in [6], which uses a single stage differential amplifier, in place of the source follower, to drive the load circuits. This new pixel structure can reduce the nonlinearity of the SF by canceling the body effect of the SF transistor. However, more transistors are introduced in the pixel at the cost of other characteristics such as noise and fill factor.

Without adopting any special pixel structure design, more research is focused on the improvement of linearity at the system-level. Off-chip calibration algorithms are commonly employed to calibrate the sensor's output [11], [12], which will consume extra power and operation time. In [6], an on-chip digital calibration method is employed to improve the linearity of the CIS without adding any cost to chip area or power consumption. After recording the digital output of the image sensor with an increasing integration time, the input of the 10-bit ADC is pre-distorted to compensate for the nonlinear errors of the imaging system [6]. This calibration method drastically reduces the nonlinearity of the 4T structure pixel from a value of 0.42 % to 0.06 %. However, a calibrated ramp signal of the image sensor needs to be first captured with a constant illumination condition. It is not always convenient to capture the imager's transfer curve with a fixed illumination.

In this paper, more techniques are discussed to further minimize the nonlinearity of the image sensor and to overcome the drawbacks of the previously presented calibration method. First, several types of pixel structures aimed for linearity optimization are explored and compared. Similar to the proposed buffer pixel in [6], a type of 4T pixel which uses a pMOS SF transistor with connected source and bulk cancels the body factor of the SF; thus a better linearity result is achieved. Furthermore, a pixel design based on a capacitive trans-impedance amplifier is also introduced, achieving an outstanding linearity result while maintaining a relatively high fill factor by sharing most transistors in a column.

Then based on the pixel mode calibration method presented in [6], two other calibration methods, voltage mode and current mode are proposed to improve the sensor's linearity without the needs for constant illumination. Notably, the current mode calibration method can calibrate the nonlinearity caused by the nonlinear integration capacitor of the pixel, significantly improving the linearity of the CIS.

The pixel optimizations and the digital calibration methods are experimentally verified with a prototype CIS fabricated in a 0.18 μm commercial CMOS image sensor technology.

This paper is organized into six sections. Section II introduces the pixel-level linearity optimization of the image sensor.

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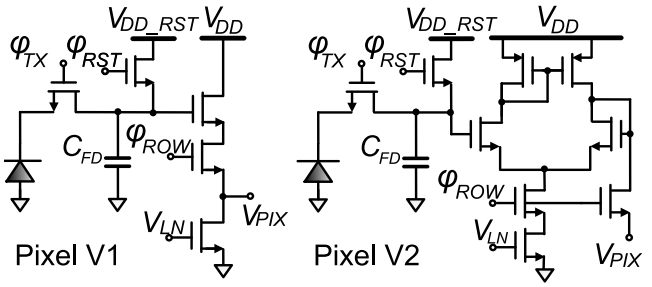

Fig. 1. The schematic of the pixel V1 and V2.

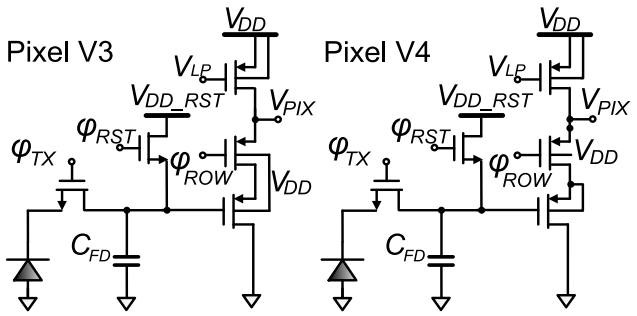

Fig. 2. The schematic of the pixel V3 and V4.

Several pixel structures including the buffer pixel structure presented in [6] are introduced and compared. Section III describes the architecture of the prototype image sensor and Section IV presents three different calibration methods. Section V presents the measurement results of the test chip, and Section VI summarizes the paper.

II. Pixel Design

For a traditional 4T pixel, the accumulated photo-generated charge is converted to an analog voltage and read by means of a source follower, shown in Fig. 1. The gain of the SF varies with the output voltage of the SF V_{PIX}, which deteriorates the linearity performance of the pixel [10]. Futhermore, the nonlinear C_{FD} also affects the linearity of the pixel. C_{FD} consists of several different types of capacitances, of which primarily the junction capacitances vary with the voltage on the FD node, which makes the total capacitance nonlinear [10], [13]. In Fig.1, the bias voltage V_{LN} controls the value of the bias current in the pixel; and the bias current is shared by the pixels in one column. The power supplies of the pixel V_{DD} and of the RST transistor V_{DD_RST} are separated.

To reduce the nonlinear effects caused by the SF in the 4T pixel, a type of buffer pixel, V2, has been proposed in [6]. Pixel V2 uses a single-stage amplifier in unity gain configuration as an analog buffer to drive the loading circuits. In a closed loop configuration, the body effect is canceled, and the linearity is improved at the cost of a smaller fill factor and a larger noise [6].

In this prototype chip, more pixel structures targeting a better linearity are presented while pixels V1 and V2 are still included to make a comparison. First, two pixel structures V3 and V4 using a pMOS SF transistor are introduced, as shown in Fig. 2. In pixel V3, the bulks of the SF and row select transistors are connected to the power supply, so the body effect of the pMOS SF is still present. In pixel V4, the bulk of the pMOS SF is tied to the source in a separated n-well, which cancels the body effect of the pMOS SF. Without using a complicated analog buffer design as pixel V2, pixel V4 achieves a unity gain with one transistor. Thus this type of pixel could realize a higher conversion gain without a noise penalty; however, the row select and source follower transistors of pixel V4 use separated n-wells; the minimal distance between different n-wells is constrained by the design rules, which limits the fill factor. Pixel V3 has a fill factor of 60% while that of pixel V4 is 48%. Compared with the traditional 4T pixel employing the nMOS type SF, the pixels V3 and V4 using pMOS type SF achieve a lower noise especially flicker noise. In Fig.2, the bias current of the pixels is variable by changing the bias voltage V_{LP}.

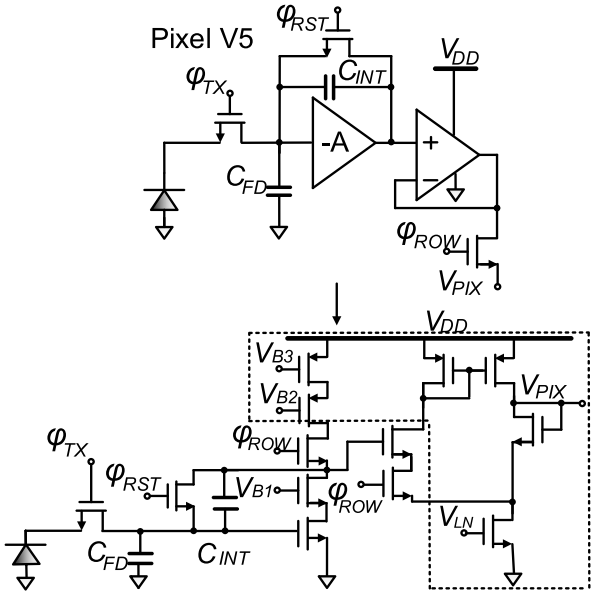

Fig. 3. The schematic of the pixel V5.

Although pixels V2 and V4 can mitigate the nonlinearity caused by the SF and thus achieve better linearity result, the nonlinear C_{FD} still contributes to the nonlinear behavior of the pixel. Further solutions can be used to reduce the nonlinear errors due to the nonconstant capacitance.

A novel pixel based on a CTIA structure is employed to reduce the nonlinearity caused by the C_{FD}. Fig. 3 shows the schematic of this CTIA pixel V5, which consists of an operational amplifier (OPA), a feedback capacitor, a reset switch and an analog buffer. A single-ended input telescopic cascade amplifier structure is adopted for the OPA to achieve a high gain on a small area due to the limited pixel size [9]. Compared with the differential-input amplifier structure, this single-ended structure has the advantage of a higher fill factor and low noise. The OPA has a voltage gain of 82dB and consumes 1μA. The feedback capacitor in the pixel is implemented by a Metal-Insulator-Metal (MIM) capacitor C_{INT} (about 4fF), which has an ultra-low voltage coefficient. With the amplifier achieving

a high voltage gain, the closed loop forces the integration of the photocurrent on C_{INT}. A highly linear output from the CTIA pixel is thus obtained. The cascode output stage of the amplifier has a higher output impedance than the source follower in the traditional 4T pixel. Therefore, an analog buffer is added after the trans-impedance amplifier. The output of the pixel can be written as (1),

$$V_{PIX} = -\frac{1}{C_{INT}} \int I_{PD} dt \cdot \frac{A_{OPA}}{1 + A_{OPA}} \tag{1}$$

where I_{PD} is the photocurrent and A_{OPA} is the open-loop gain of the analog buffer.

As shown in Fig. 3, the whole pixel contains seven nMOS transistors, while the pMOS and other nMOS transistors inside the dotted line are shared by all pixels in a column, this leads to a fill factor of 36% with a pixel size of 12 μm $\times$ 10 μm. The bias voltages $V_{B1} \sim V_{B3}$, V_{LN} are generated outside the pixel. The conversion gain (CG) of the CTIA pixel is mainly determined by the value of the MIM capacitor C_{INT}. The reset voltage of the pixel is equal to the gate-source voltage of the amplifier's input transistor, which is sensitive to the process variation. However, the following correlated double sampling (CDS) circuit can reduce this type of noise [9].

In theory, the CTIA pixel can achieve a good linearity. However, the complex pixel structure leads to a smaller fill factor compared to other pixel structures. Furthermore, the CTIA pixel has a worse noise performance. In the CTIA pixel, the main temporal noise sources include the noise of the OPA, reset noise caused by the reset transistor and the noise of the analog buffer. The reset noise and most of the flicker noise of the amplifiers can be further canceled by the following CDS circuit [14], [15].

The output-referred noise power of the trans-impedance amplifier [14] is shown in (2), where C_{PD} is the capacitance of the photodiode and C_L is the load capacitance of the amplifier; k is Boltzmann's constant and T is the absolute temperature; α is a noise constant depending on the amplifier structure [14].

$$\overline{V_{n,o}^2} = \frac{akT}{(\frac{C_{INT}}{C_{INT}+C_{PD}})(C_L + \frac{C_{PD}C_{INT}}{C_{INT}+C_{PD}})} \tag{2}$$

The thermal noise contributed by the following analog buffer in the pixel [16] is shown in (3), where b is the transconductance ratio of the load and input transistors in the buffer; $C_{L,ota}$ is the load capacitance of the analog buffer.

$$\overline{V_{n,ota}^2} = \frac{4}{3}(1+b)\frac{kT}{C_{L,ota}} \tag{3}$$

To illustrate and verify the current mode calibration method proposed in Section III, two further pixels V6 and V7 are adapted in this paper based on the 4T pixel structures V1 and V3. These pixels are shown in Fig. 4. Compared with the 4T pixels V1 and V3, an extra transistor is added on the FD node of the pixel V6 and pixel V7. The source of that extra transistor is connected to a calibration current sink circuit and the gate of the transistor is control by the signal φ_{IIN}. When the signal φ_{IIN} is turned on, the FD discharges into the out-pixel current sink, where an ultra-low current I_{IN} imitates the photocurrent converted by the photodiode. I_{IN} can be used to capture the electron-voltage transfer curve of the image sensor and further to calibrate the image sensor.

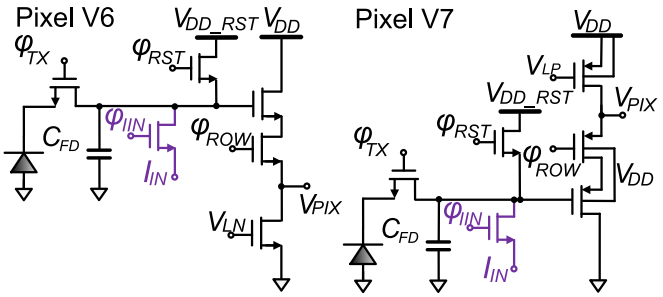

Fig. 4. The schematic of the pixel V6 and V7.

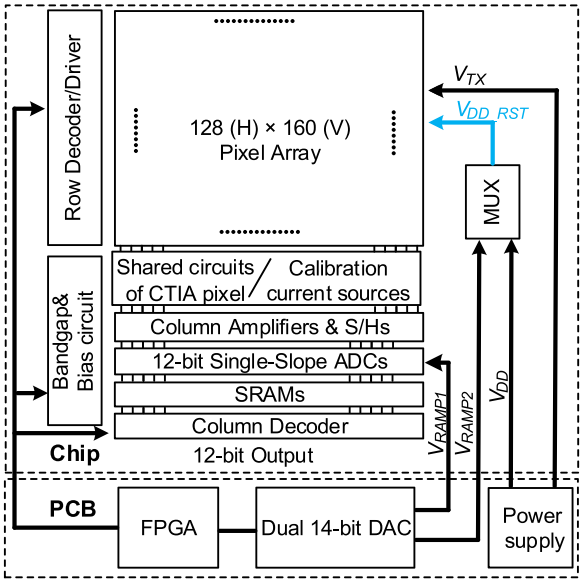

Fig. 5. The diagram of the readout channel.

III. Chip Architecture

In this paper, a prototype CMOS image sensor containing different pixel structures is presented. Fig. 5 shows the overall architecture of the image sensor. The pixel array consists of 128×160 pixels with a pitch of 12μm. The shared parts of the CTIA pixel circuits and the circuits of the calibration current source used in the CM calibration are placed between the pixel array and readout circuits. The column-parallel analog chain contains a column amplifier, a sample and hold circuit (S/H), a 12-bit Single-Slope Analog-to-Digital Converter (SS-ADC), and a SRAM array. The column amplifier realizes an analog CDS function and provides a programmable gain up to 8$\times$ to suppress the read noise. An onboard dual 14-bit digital to analog converter (DAC) is employed to provide a ramp signal $V_{RAMP1}$for the ADCs as well as a periodic ramp signal V_{RAMP2}as the in-pixel reset transistor's power supply (V_{DD_RST}) for voltage mode calibration. In the other modes, V_{DD_RST} is constant and provided by the onboard power supply.

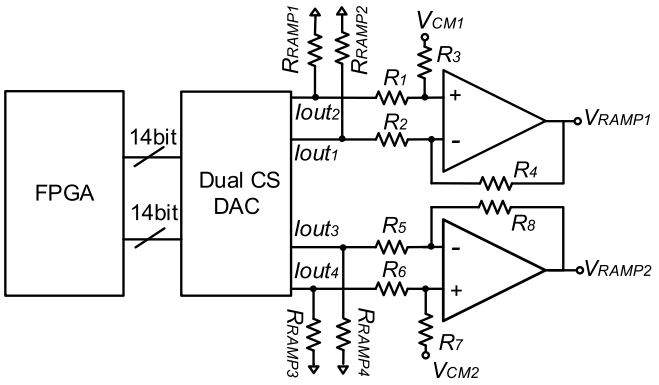

Fig. 6. The schematic of the ramp generator based in a dual current steering DAC.

For the ramp generation circuit, as shown in Fig. 6, a current steering DAC structure is chosen considering its advantages on high resolution and high speed performance. Digital signals from the FPGA are converted into two groups of differential current outputs by the dual current steering DAC, which are conveyed by the load resistors $R_{RAMP1}\sim R_{RAMP4}$ to two differential voltage outputs. Subsequently, together with the resistors $R_1\sim R_8$, two operational amplifiers which have a large input and output swing convert the differential voltages to two single-ended ramp signals V_{RAMP1} and V_{RAMP2}.

IV. Calibration Methods

In the proposed pixel structures especially the CTIA, pixel-level linearity optimizations can improve the linearity performance of the pixel. However, the readout circuit still contributes to the nonlinear errors of the image sensor.

Previously, the pixel mode calibration has been presented in [6] to calibrate the nonlinear errors of the image sensor. In this prototype chip, the resolution of the ADC has been upgraded from 10-bit to 12-bit to achieve a better calibration effectiveness. Furthermore, two other calibration methods are explored and proposed to overcome the first method's deficiency.

The 4T pixel V3 is used to illustrate the operating principles of the first calibration method: pixel mode calibration. As shown in Fig. 7, V_{DD_RST} is constant; the photodiode is first reset by pulsing φ_{TX} and φ_{RST}, then the pixel is read out conventionally; the adjacent falling edges of the signal φ_{TX} determines the exposure time T_{EXP} of the pixel. The signal φ_{RST} is activated again to enable the readout of the V_{RST}, which is pixel's reset signal; at the same time, the control signals φ_{AMP_RST} and φ_{ADC_RST} are sequentially activated, and the column amplifier and ADC realize auto-zeros. Afterward, the signal φ_{TX} is activated, the accumulated electrons of the photodiode during the integration phase will be transferred to the FD. Further, the differential value of the pixel's reset and signal value is sampled on the capacitor C_{SH} by the digital signal φ_{SH} and digitalized by the column ADC. The timing of the other control signals for the image sensor are the same as the timing scheme introduced in [17].

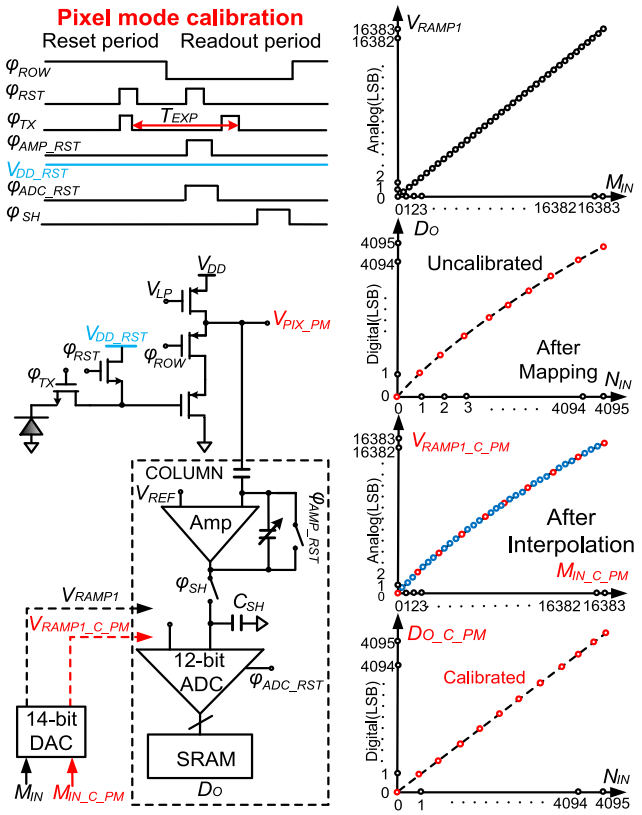

Fig. 7. Pixel mode calibration operation and its timing diagram.

The principle of the pixel mode calibration method is to capture the nonlinear transfer function between the number of incoming photons and the final digital output (D_O) of the ADC; then the data is used to modify the ADC's ramp to compensate for the original nonlinear behavior of the CIS [6]. The resolution and linearity performance of the DAC decides the effect of the calibration method [17]. The resolution of the DAC is upgraded to 14-bit since the resolution of the ADC employed in this paper is 12-bit.

There are two ways to increase the number of impinging photons of the pixel. The first way fixes the exposure time of the image sensor and varies the intensity of a light source linearly; another way is much simpler: by increasing the exposure time of the sensor at a fixed light condition. In this paper, the second method is adopted.

During the PM calibration, the exposure time is increased from 1 $\times T_{EXP}$ to 4096 $\times T_{EXP}$ with a fixed light intensity. The digital input code of the DAC M_{IN} increases from 0 to 16383($2^{14}-1$) and generates a linear ramp signal V_{RAMP1}. The digital output of the ADC is captured and stored in the SRAM for each exposure time. The mapping process removes the offset and gain errors from the data. The data is then interpolated from 12-bit to 14-bit to match the resolution of the DAC. The final data sequence $M_{IN\_C\_PM}$ is sent to the input of the DAC to generate a calibrated ramp signal $V_{RAMP1\_C\_PM}$, containing the information of the nonlinearities of the pixel and the readout circuit. By applying the nonlinear ramp signal, the original nonlinearities of the image sensor are canceled out.

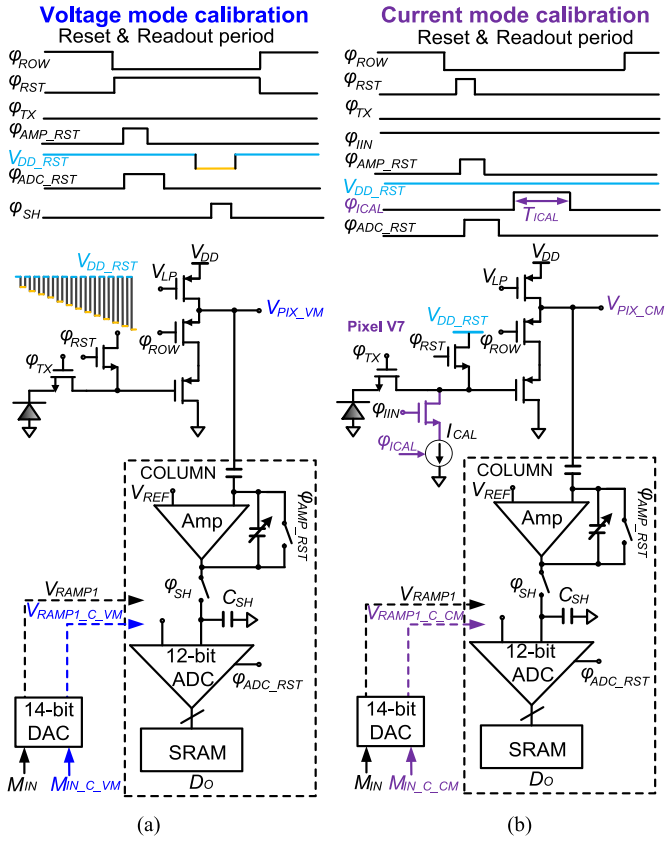

Fig. 8. (a) Voltage mode calibration operation and its timing diagram; (b) Current mode operation and its timing diagram.

Pixel mode calibration can compensate the nonlinearity caused by the readout circuitry as well as the pixel circuit; thus it drastically improves the linearity performance of the image sensor without extra penalty on power consumption, chip size and speed. However, the transfer function of the image sensor needs to be captured with a constant illumination.

In this paper, VM and CM calibration methods are proposed to eliminate the dependency on the light condition. Fig. 8 (a) introduces the voltage calibration method, where the TX transistor remains off and the photodiode is not used. The transfer curve of the image sensor is measured in a dark environment. Instead of increasing the exposure time, a decremental periodic ramp signal V_{RAMP2} is applied to the drain of the RST transistor. V_{RAMP2}, generated by the DAC, imitates the voltage on the floating diffusion node in pixel mode. V_{RAMP2} has two values, representing the two different phases of a conventional pixel operation. A monotonic increasing output signal is achieved by means of the subsequent CDS circuit. Digitized by the on-chip ADC, the final digital output contains the nonlinear information of the SF and readout circuit. Similarly, based on the voltage transfer function between the input ramp signal V_{RAMP2} and the final digital output, the voltage mode calibration records the nonlinear information of the SF and readout circuitry. After mapping and interpolation, the incremental sequence $M_{IN_C_VM}$is converted by the DAC into a new ramp signal $V_{RAMP1\_C\_VM}$, which will be used to compensate the original nonlinearities of the SF and readout circuit.

Compared with the PM calibration method, the power consumption and size of the system will increase with the VM method since the second DAC is needed to generate the periodic ramp signal V_{RAMP2} for the pixel. Furthermore, the voltage mode calibration technique is unable to obtain the information of the photodiode and the Capacitance-Voltage characteristics of the C_{FD}; as such, the nonlinearity caused by C_{FD} cannot be calibrated and the improvement is less effective when compared to the PM calibration. The third type of calibration method: current mode calibration is thus proposed.

The process of the CM calibration is illustrated with pixel V7, where the additional calibration transistor is used to convey the calibration current. As shown in Fig. 8(b), during the CM calibration, the photodiode is also disabled. The added transistor avoids the influence on the other group of pixels with different pixel structure in the same column. Signal φ_{ICAL} controls the operation time T_{ICAL} of the calibration current. The calibration current is maintained constant while the period of T_{ICAL} is changed incrementally. The output voltage of the pixel is proportional to the period of T_{ICAL}. If the nonlinearity caused by the transformation of photons to electrons is negligible, this method should calibrate the nonlinearity caused by the pixel and readout circuit. The basic operation of the CM is the same as the operation in pixel mode. By increasing the operation time of φ_{ICAL}, the transfer curve between the calibration charge and the final digital output can be obtained. Like other calibration modes, the updated ramp signal is employed to calibrate the nonlinearity of the image sensor.

CM calibration can improve the calibration effect compared to VM calibration. The most prominent challenge of the current mode calibration is the design of a small calibration current source. The current of the photodiode is usually in the range of fA$\sim$pA, depending on the intensity and wavelength of the light source [18], [19]. It is difficult to design such a small current source to imitate the photocurrent generated by the photodiode. In this paper, all 64 pixels in a column share one generated calibration current. There are two types of structures to realize a stable current reference. The first type of current reference is based on a β multiplier [20], [21], while another type employs a reference voltage and a resistor [22], [23].

In this test chip, a reference current generated by a conventional voltage-to-current converter is mirrored to feed the FDs in the pixels as shown in Fig. 9. A folded cascode amplifier is used in the voltage-to-current circuit. A negative feedback loop forces the current flow through the nMOS transistor which is equivalent to the input voltage V_{REF} divided by the resistor R_{IN}. V_{REF} is the output voltage of a programmable bandgap circuit. The current through the resistor R_{IN} is mirrored to generate the 32 calibration currents, one per column. To achieve a sub-nA current, the resistor must be in the order of GΩ, which would cover a large chip area. In [24], the resistor is realized by a switched capacitor. In this design, an off-chip resistor R_{IN} is selected to save chip area and to facilitate the adjustment of the current. The reference current is adjustable by changing the voltage value of V_{REF} or the resistor value of onboard resistor R_{IN}. The absolute value of the

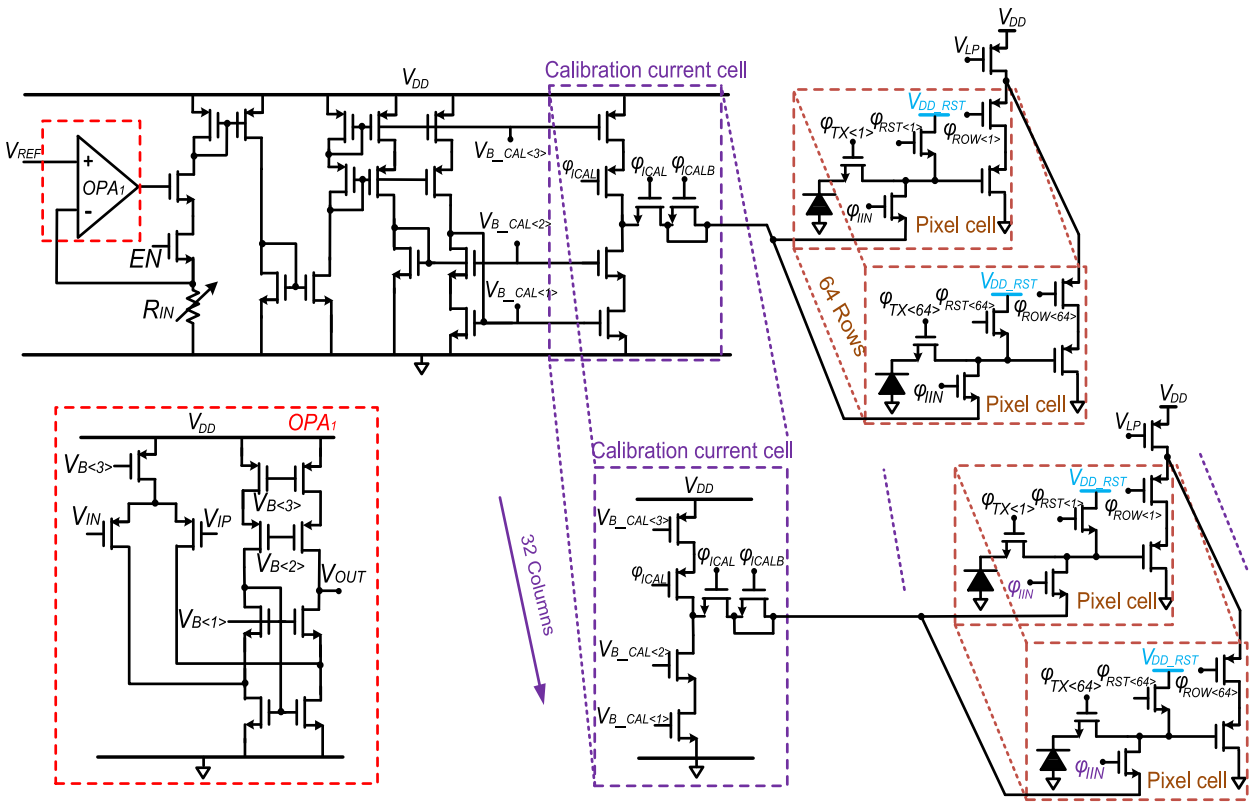

Fig. 9. The schematic of the calibration current generator.

calibration current is not so critical as long as the calibration current is stable. By lengthening the operation time of T_{ICAL}, a decremental output of the pixel can be attained. The value of the R_{IN} follows (4), where I_{ICAL} is the calibration current; T_{ICAL_MAX} is the maximum operating time of calibration current; N_{ROW} is the number of the shared pixels in a column and ΔV_{FD} is the voltage range on the FD.

$$C_{FD}\Delta V_{FD} = I_{ICAL}T_{ICAL\_MAX} = \frac{V_{REF}}{R_{IN}}/N_{ROW}T_{ICAL\_MAX} \quad (4)$$

Dummy switches, driven by φ_{ICALB} which is the inverted control signal of φ_{ICAL}, are added to the circuit to reduce the charge injection and clock feedthrough. Based on simulations, the dummy switches can reduce the corresponding errors from 2.9 mV to 0.51 mV.

V. Measurement Results

The proposed CMOS image sensor has been fabricated in a commercial 0.18-μm CIS process technology. Fig. 10 shows the micrograph of the fabricated chip. The chip size is 3.1 mm × 5.0 mm while the core area of the pixel array is 1.54 mm × 1.60 mm. An Altera Cyclone FPGA is used to provide the digital control signals and to capture the output data of the image sensor. A 56 kb (14b × 4096) memory in the FPGA is allocated to store the data.

The nonlinearity of the column ADC is an important nonlinear error source of the readout circuitry. There are several methods to measure the nonlinearity of the ADC [25]–[27]. The histogram test method is the most popular one. By applying a ramp voltage signal generated by a higher resolution DAC or a low-frequency sinusoidal wave to the input of the ADC, the static performance of the ADC can be characterized. In this design and in accordance with the calibration method adopted, a linear voltage ramp generated by the same DAC is used to measure the nonlinearity of the column ADC. The measured nonlinearity results contain the nonlinearity of the ADC as well as the DAC. In this design, the employed DAC device (DA5672) has an excellent linearity performance (DNL<0.7 LSB and INL<1.1 LSB). The clock frequency of the 14-bit DAC is 100MHz while that of the 12-bit ADC is 25MHz.

For a typical column ADC, the DNL errors are −0.36/+0.37 LSB and the INL errors are −0.88/+1.97 LSB, corresponding to a nonlinearity of 0.034% based on the calculation method proposed in the EMAV1288 measurement standard [28]. The nonlinearity performance of all column ADCs is plotted in Fig. 10. All ADCs have a nonlinearity of less than 0.05%.

The CTIA pixel is the most important pixel structure proposed in this paper to achieve an optimized linearity performance. The green signal in Fig. 12 shows the measured output signal of the CTIA pixel monitored by an oscilloscope, while the yellow signal represents the reset signal φ_{RST}. By pulsing the signal φ_{RST}, the FD node is first reset to a voltage determined by the threshold voltage of the input transistor of the amplifier, which is around 0.8V. When the reset switch opens, the charges generated by the photodiode

TABLE I
THE CHARACTERISTICS OF THE PIXELS

Pixel	Fill factor (%)	Conversion gain (μV/e-)	Full Well capacity (e-)	Noise (e-)	Dark current (e-)	FPN(%)	DR (%)	PRNU (%)	Nonlinearity (w/o calibration) (%)
V1	46.4	54	22070	3.7	26	0.25	75.5	0.26	0.41
V2	46.4	60	21040	4.5	19.7	0.29	73.4	0.55	0.24
V3	60	40	23100	3.6	60	0.44	76.0	0.76	0.68
V4	48	70	13000	2.9	36	0.46	73.0	0.89	0.35
V5	36.3	40	30610	16.3	453	0.50	65.5	0.99	0.095
V6	45	43.2	24000	4.8	32	0.26	73.9	0.30	0.45
V7	42	50	14460	2.8	58	0.45	74.2	0.80	0.75

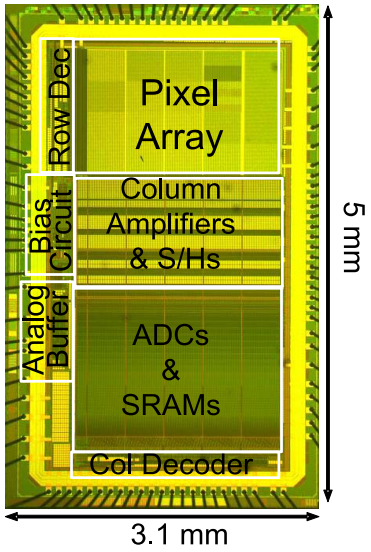

Fig. 10. Chip microphotograph.

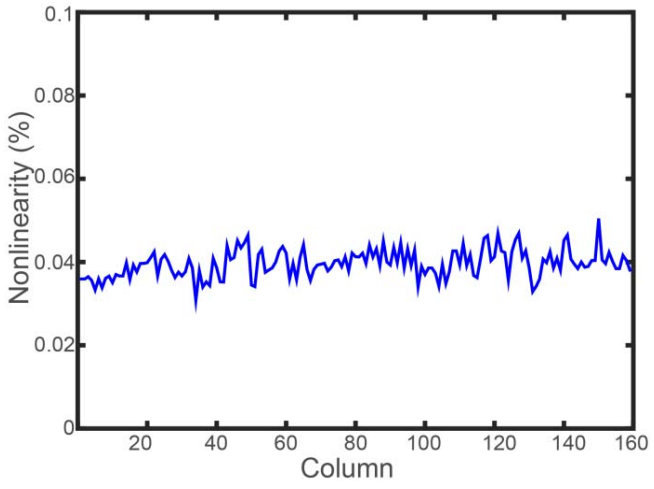

Fig. 11. Measured nonlinearity performance of SS-ADC array.

will be integrated on the MIM capacitor C_{INT}. As shown in Fig. 12, the CTIA pixel has a large linear output signal from 0.8V∼3V.

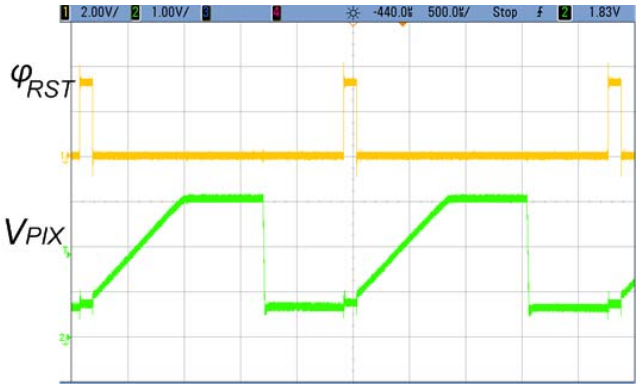

Fig. 12. The measure output waveform of CTIA pixel.

In the linearity measurement, a tungsten lamp provides a constant illumination. The exposure time increases from 0.1 μs to 409.6 μs evenly. All linearity curves are measured with 8×30 pixels and averaged over 200 frames captured while the gain of the column amplifier is set to unity. 5%∼95% of the whole output range of the pixel is chosen to calculate the nonlinearity according to measurement standard EMAV1288. In the measurement, for the pixels V3, V4 and V7, where pMOS transistors are used as the SF, V_{DD_RST} is set as 2 V. For the other pixel structures, the value of V_{DD_RST} is 2.8V. The high voltage of the transfer transistor in the pixel V_{TXH} affects the pixel's performances, including the dark current and fixed pattern noise (FPN) [29]. The value of V_{TXH} is separately set according to each pixel structures.

Table 1 shows the nonlinearity results for all type of pixel structures. The other key characteristics of the image sensor, such as fill factor, noise and dark current measured at room temperature are also given in table 1.

Without employing any calibration method, the 4T pixel V1 has a nonlinearity of 0.41 % while pixel V2 reduces the nonlinearity of the SF, which achieves a nonlinearity of 0.24 %. Furthermore, pixel V2 realizes a larger conversion gain than the 4T pixel V1 by employing the unity gain analog buffer. To fairly compare the linearity performance, pixels V1 and V2 use the same photodiode design, thus achieving the same fill factor.

Pixels V3 and V4 use the pMOS SF, whereby V4 employs the separated n-well to optimize the linearity. Pixel V3 has a

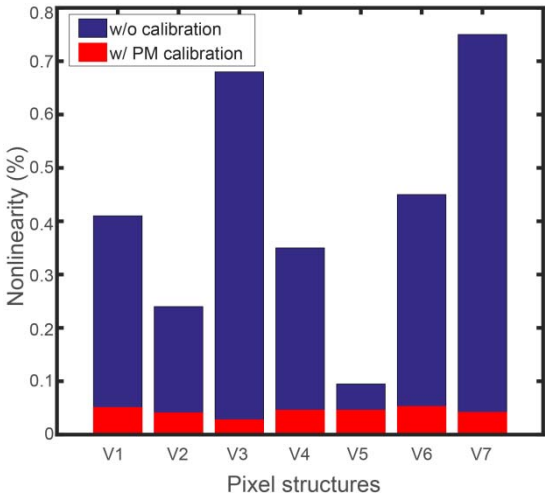

Fig. 13. Measured nonlinearity performance of all pixel structures.

nonlinearity of 0.68 % while pixel V4 improves the nonlinearity to 0.35 % by canceling the body effect of the pMOS SF. Pixel V4 also achieves a larger conversion gain and better noise in the electron domain. However, the distance between the different n-wells leads to a smaller fill factor in pixel V4.

The CTIA pixel V5 further reduces the nonlinearity caused by the nonlinear C_{FD}; it achieves the best linearity result among all types of pixels, of less than 0.1 % before calibration. Nevertheless, a small value of the MIM capacitance used in the CTIA will generate a large mismatch which leads to a larger photon response non-uniformity (PRNU). According to the capacitance model provided by the process files, a standard deviation of the MIM capacitance ($1.6\mu\text{m} \times 1.7\mu\text{m}$) is around 0.91%. The measured PRNU of the CTIA pixel is 0.99%. Furthermore, it has worse noise performance and fill factor. Most prominently, the noise contributed by the transimpedence amplifier is dominant in the CTIA pixel.

Pixels V6 and V7 have a nonlinearity of 0.45 % and 0.75 %, respectively.

As shown in Table 1, the linearity of the image sensor can be improved by the pixel-level linearity optimization. However, compared with the fundamental 4T pixel V1, pixels V2 and V5 sacrifice the other key characteristics of the image sensor including PRNU and noise. Pixels V3 and V4 employ a pMOS SF and have a smaller output swing than the traditional 4T pixel with nMOS SF. Furthermore, the readout circuit including the amplifier and ADC also contributes to nonlinear errors, which needs extra methods to improve the linearity.

In this paper, three calibration methods are thus proposed to improve the linearity of the image sensor. The verification of the calibration methods starts with the pixel mode calibration. As shown in Fig. 13, without adding any cost to the chip size or power, the pixel mode calibration method efficiently improves the nonlinearity of the image sensor. All pixel structures achieve a nonlinearity less than 0.05% after calibration.

In particular, pixel V3 achieves the best nonlinearity result with the assistance of the PM calibration, which is 0.028%. Fig. 14 (a) plots the DNL results of the image sensor with

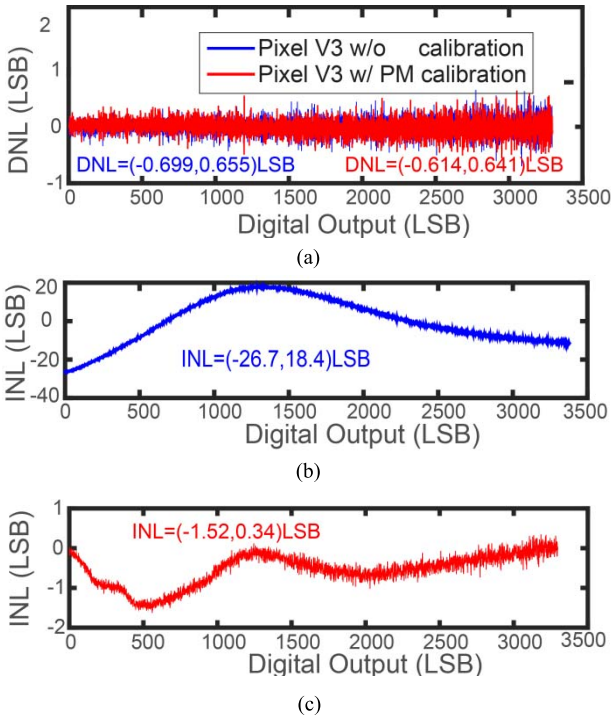

Fig. 14. The nonlinearity of pixel V3 (a) DNL; (b) INL (w/o calibration); (c) INL (w/ PM calibration).

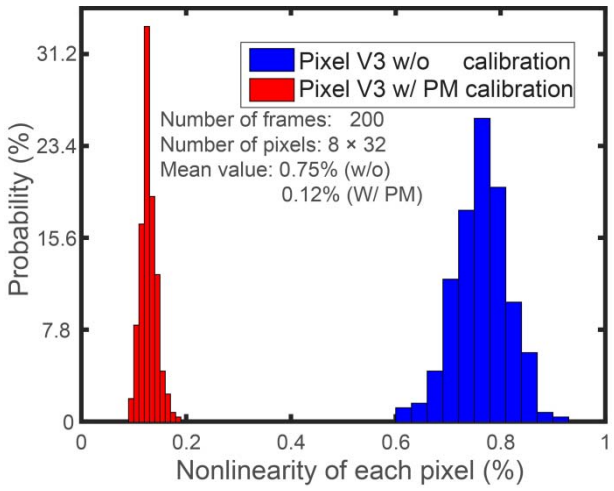

Fig. 15. Histogram of the nonlinearity in pixel V3 array.

pixel V3 while Fig. 14 (b) and (c) show the corresponding INL results. The blue lines show the measurement results without calibration, and the red lines represent those with PM calibration. As shown in Fig.14, it is clear that the PM calibration method strongly improves the linearity result of the image sensor.

Fig.15 shows the corresponding histogram of the nonlinearity results in the pixel V3 array. Without calibration, the mean value of the nonlinearity in the pixel array V3 is 0.75 %. With the assistance of the PM calibration, the mean value is improved to 0.12 %, which proves its effectiveness for each pixel.

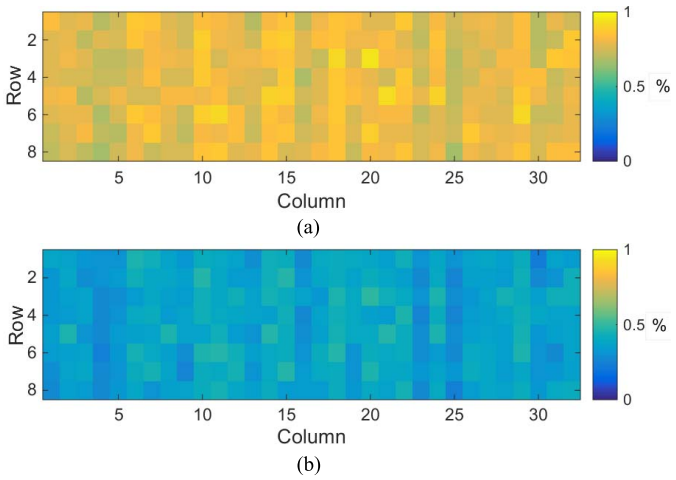

Fig. 16. The nonlinearity of pixel V3 (for each pixel). (a) w/o calibration; (b) w/VM calibration.

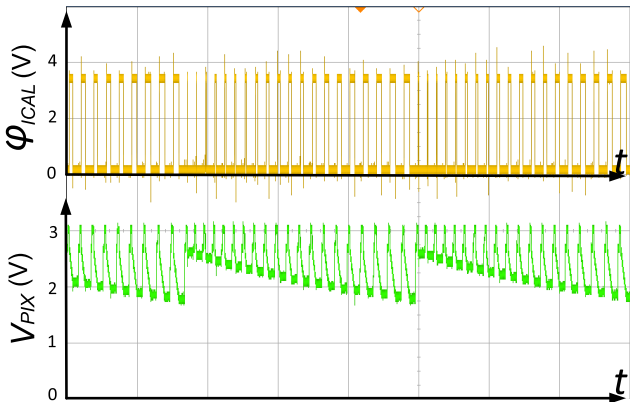

Fig. 17. Measured output voltage of the pixel V7 in CM calibration.

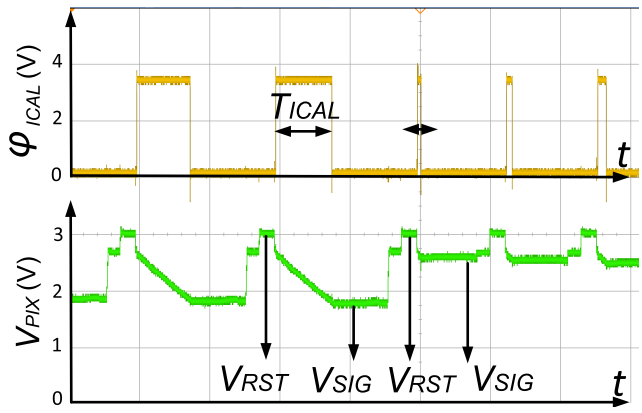

Fig. 18. Measured output voltage of the pixel V7 in CM calibration (zoomed in).

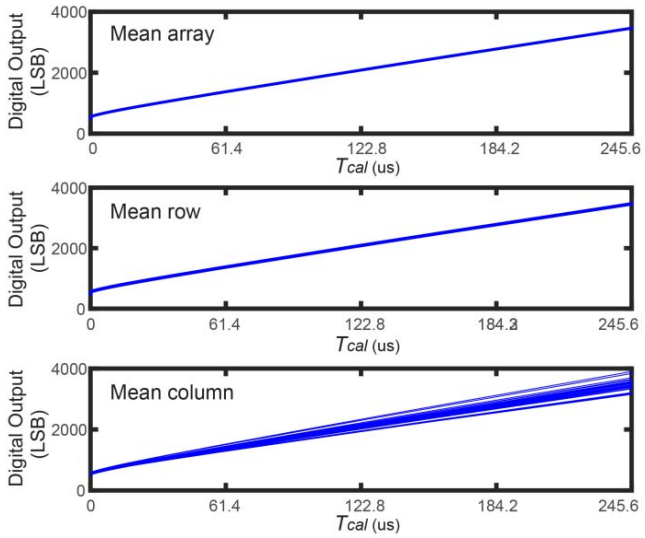

Fig. 19. Measured digital output values of the pixel V7 in CM calibration.

Next, pixels V1 and V3 are used to verify the voltage mode calibration method, which should cancel the nonlinearity caused by the SF transistor and the following readout circuitry. However, the missing information of the integration capacitance in the electron-voltage conversion of the pixel limits the effectiveness of the calibration method. The measured results show that the voltage mode calibration slightly improves the linearity performance of the pixels V1 and V3. With voltage mode calibration, the nonlinearity of the pixels V1 and V3 are improved from 0.41 % to 0.30 % and 0.68 % to 0.43 %, respectively.

Fig.16 shows the linearity improvement for each pixel with the proposed VM calibration method in the array of pixel V3.

Finally, the validity of the third calibration method, the current mode is verified through the pixels V6 and V7. Fig. 17 plots the output voltage of the pixel V7 in current mode calibration, where a decreasing pixel output signal is captured with an increasing period of the signal φ_{CAL}. As shown in Fig. 17, the period of φ_{ICAL} increases from $1 \times T_{ICAL\_unit}$ to $20 \times T_{ICAL\_unit}$ evenly in steps of 50 μs, and the signal value of the pixel V_{SIG} decreases from 2.7 V to 1.8 V.

By zooming into the waveform, the details of the signals can be seen as shown in Fig. 18. First the FD node is reset and V_{RST} is around 3V, then the signal value of the pixel V_{SIG} decreases with the width of the T_{ICAL}.

In full calibration operation, the unit integration time of the calibration current T_{CAL_unit} is set as 60 ns. The integration time T_{ICAL} increases evenly from 60 ns to 4096×60 ns in steps of 60ns.

Fig. 19 shows the measured digital output values of pixel V7 in full current mode calibration. From top to bottom, the curves represent the mean value of all pixels in the array, the mean value of all pixels in the same row, and the mean value of all pixels in the same column, respectively.

Due to the small value of the bias current used in the current source, the mismatch of the current source transistors from column to column leads to a considerable variation of the calibration currents between the columns. So here, different to the pixel mode and voltage mode calibration, the transfer curve extracted from the pixels in one column is used to calibrate all the pixels of the whole array.

The measured results show that the current calibration can improve the nonlinearity of pixels V6 and V7 from 0.45 % and 0.75 % to 0.15 % and 0.16 %, which is better than the voltage

TABLE II
PERFORMANCE COMPARISON

		[6]	[7]	[9]	[30]	[31]	This work				
Process (nm)		180	500	350	180	65	180				
Array size		128 ×128	124 × 132	144 ×144	1620×1228	4 × 4	128 × 160				
Pixel size(μm^2)		10 × 10	20.1 ×20.1	9.5 × 9.5	2.6 × 2.6	22 ×22	12 × 10				
Frame rate		60	70	60	NA	NA	40				
Structure		Buf	CTIA	CTIA	CTIA	CTIA	n-SF	Buf	p-SF	CTIA	p-SF
							pixel V1	pixel V2	pixel V3	pixel V5	pixel V7
Fill factor (%)		47	42	26	NA	14	46.4	46.4	60.0	36. 3	42.0
Conversion gain (μV/e-)		56.3	NA	76	88.2	16	54	60	40	40	50
DR (dB)		74	48	61	47	62	75.5	73.4	76.0	65.5	74.2
Peak SNR (dB)		NA	NA	49	41	NA	43.4	43.2	43.6	44.2	41.5
Read Noise (mV)		0.187	0.82	1.90	5.2	0.98	0.20	0.27	0.144	0.65	0.14
Read Noise (e-)		4.17	NA	25	59	61	3.7	4.5	3.6	16.3	2.8
Dark current (pA/cm^2)		NA	142	1540	490	NA	7.4	5.6	12.7	166.3	18.0
Full Well capacity (e-)		20960	NA	32000	13800	77500	22070	21040	23100	30610	14460
Pixel PRNU at Sat (%)		NA	0.99	1.8	1.8	0.73	0.26	0.55	0.76	0.99	0.80
Nonlinearity (%)	(w/ o calibration)	0.24	NA	NA	NA	0.57	0.41	0.24	0.68	0.095	0.75
	(w/ PM calibration)	0.058					0.050	0.042	0.028	0.048	0.04
	(w/ VM calibration)	NA					0. 30	NA	0.43	NA	0.46
	(w/ CM calibration)	NA					NA	NA	NA	NA	0.16

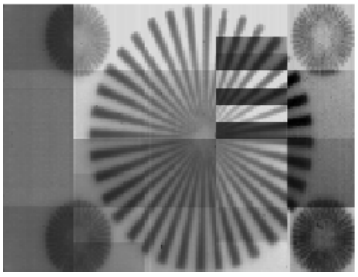

Fig. 20. Captured image.

mode calibration method. It is mainly because the information of the Capacitance-Voltage characteristics of the C_{FD} has been captured in the updated ramp signal to calibrate the nonlinear errors during the pixel's electron-voltage conversion.

Fig. 20 shows an image captured with this test chip. There are various groups with different pixel structures, which have different conversion gains and noise performances. The test chip has a non-uniform photon response due to all these variations.

The measurement results of the proposed pixels are summarized and compared with previous designs in Table II. Compared with the results of the CTIA pixels reported in other publications [7], [9], [30], [31], the CTIA pixel proposed in this design achieves an excellent trade-off between linearity and other characteristics of the pixel. Furthermore, the proposed digital calibration methods improve the linearity of the image sensor. Most notably, pixel V3 achieves a nonlinearity of 0.028%, which is two times better than the state-of-the-art.

VI. CONCLUSION

In this paper, several different pixel structures, including a buffered CTIA pixel architecture, are proposed to realize high linearity at the pixel-level. Three calibration methods further exhibit their advantages and disadvantages on improving the linearity from the system-level. The measured results on a proof-of-concept chip fabricated in a commercial 0.18-μm CIS process show the linearity improvement with all the techniques used. The CTIA pixel achieves the best linearity result out of all pixel structures. The pixel mode calibration method attains the best linearity results for all types of pixels. Voltage mode calibration method demonstrates the advantage of working without constant illumination while maintaining linearity improvements. Current calibration mode has the advantage of the voltage mode method and achieves a linearity improvement approaching that of the pixel mode method.

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