

# Development and Evaluation of a Highly Linear CMOS Image Sensor With a Digitally Assisted Linearity Calibration

Fei Wang<sup>1</sup>, Liqiang Han, and Albert J. P. Theuwissen, *Fellow, IEEE*

**Abstract**—This paper presents a highly linear CMOS image sensor (CIS) designed in a commercial 0.18- $\mu\text{m}$  CIS technology. A new type of pixel is proposed based on the linearity analysis of a conventional 4T active pixel. The new type of pixel can mitigate the nonlinearity caused by the in-pixel source follower (SF) transistor. In addition, the optimization of the pixel design, a digitally assisted calibration method is proposed to further reduce the nonlinearity of the image sensor, especially, the nonlinearity caused by the integration capacitor ( $C_{\text{FD}}$ ) on the floating diffusion (FD) node. A hybrid behavioral model is proposed to validate the calibration method. Experimental results show that the new type of pixel has a better linearity performance comparing with that of the typical 4T pixel. TCAD simulation results are used to help explain the spillback effect in the transfer transistor's channel. With the digital calibration, the linearity performances of the pixels in different settings have been improved.

**Index Terms**—Analog-to-digital converter (ADC), calibration, CMOS image sensor (CIS), linearity, pixel.

## I. INTRODUCTION

IN ALL imaging systems, there is a nonlinearity between the input luminance intensity and the digital output (Do) response. For the most commercial imaging systems, the linearity requirement is not so stringent. Sometimes, the deviations from a linear response in the camera systems are intentionally built to serve different purposes [1], [2]. For example, gamma correction is added to code luminance into a perceptually uniform domain [1]. In [2], the nonlinear characteristics of the pixel are utilized to increase the dynamic range (DR) of the image sensor.

However, linearity is still a crucial property for the image systems in many applications where the image performances rely on the absolute signal measurements. In quantitative imaging operations, the image sensor must be linear enough

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F. Wang is with the Electronic Instrumentation Laboratory, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: f.wang-3@tudelft.nl).

L. Han is with the School of Electronic Information Engineering, Tianjin University, Tianjin 300072, China (e-mail: hlq@tju.edu.cn).

A. J. P. Theuwissen is with Harvest Imaging, B-3960 Bree, Belgium, and also with the Electronic Instrumentation Laboratory, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: a.theuwissen@scarlet.be).

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to perform an image analysis [3], [4]. For scientific imaging, the linearity of the image sensor usually constrains the performance of spectral reconstruction. In these applications, high-performance charge coupled devices (CCDs) imaging systems are usually adopted to achieve excellent linearity performance. Due to the advantages of system-on-chip capability with low power consumption and low cost, as well as the technological breakthroughs on the imaging performances in the past decades, CMOS image sensors (CISs) have already become the preferred choice in comparison with the CCD competitor.

Many efforts have been spent on linearizing the photon response of CMOS imaging systems. On software level, many optimization algorithms such as analytical means and lookup table [5], [6], are commonly used to calibrate the Do and recover the linear response by acquiring and refitting the transfer curve of the image sensor. However, the off-chip processing consumes a lot of operation time, power, and the linearity improvement is not remarkable. The improvement usually depends on the order of the polynomial and the accuracy of the approximation that the polynomial function can achieve. A commercial camera attains 0.5% nonlinearity after calibration in [6]. Also with the increase of the resolution and complexity of the sensor, the demands of on-chip image processing capabilities, such as computing and compression capability, further trigger the requirement of on-chip linearity improvement capability.

To reduce the off-chip processing time, power consumption, and improve the system efficiency, more and more attention has been given on on-chip level improvement [7]–[11]. On hardware level, the linearity of a CIS is determined by its pixel design and readout circuitry. Most of the pixel's nonlinearity comes from the source followers (SFs) nonlinear gain and the integration capacitor's voltage dependence [7]. Ge and Theuwissen [9] optimizes the pMOS SF design by tying the source to the bulk in a separated n-well with other transistors, which cancels the body effect and therefore achieves better linearity results. In [10] and [11], two types of pixel design based on the capacitive transimpedance amplifier (CTIA) structure are proposed to improve the linearity on the pixel level. However, the pixel utilizing the CTIA structure has disadvantages such as high power consumption and low fill factor. More importantly, its poorer noise performance has prevented it from being widely used. Njuguna and Gruev [8] propose a feedback mechanism in the current conveyor circuit to reduce the fixed pattern noise (FPN) and improve the

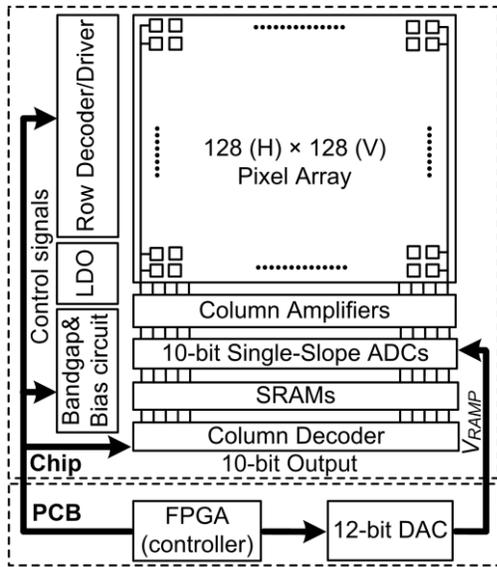


Fig. 1. Proposed CIS system diagram.

linearity of the current mode CIS on system level. However, the hardware overhead is high, and the improvement is limited. Leonardo *et al.* [12] propose an output-regulated voltage follower with a feedback mechanism outside of the pixel, which extends the output linear voltage swing of the pixel without any modification on the pixel. The novel voltage follower can cancel the nonlinearity caused by the SF and achieves a simulated nonlinearity value of 0.05%. However, this structure has a larger noise and the effect of nonlinear integration capacitance on the linearity is still present.

In this paper, based on the linearity analysis of the 4T pixel, a new type of pixel is proposed to improve the pixel's linearity. Nevertheless, the new design cannot overcome the nonlinearity caused by the nonlinear integration capacitor  $C_{FD}$ . A digitally assisted linearity calibration method is employed to further improve the linearity in the prototyped CIS.

An image sensor system is a complex, multi-physical heterogeneous system which consists of optical components and electronic blocks. A hybrid behavioral model of the CIS using MATLAB and Verilog-A is proposed to speed up the simulation and validate the linearity calibration method in this paper.

This paper focuses on the linearity improvement of the CIS and is organized as follows. In Section II, the chip's architecture and circuit implementation are introduced. The behavioral model of the hierarchical image sensor system is also presented in this section. The experimental results of the fabricated image sensor are presented in Section III, followed by a conclusion in Section IV.

## II. CHIP ARCHITECTURE AND CIRCUIT DESIGN

In this paper, a prototype CIS with a digitally assisted linearity calibration method is proposed to achieve high linearity. Fig. 1 shows the overall architecture of the image sensor which uses a rolling shutter readout mechanism. The sensor consists

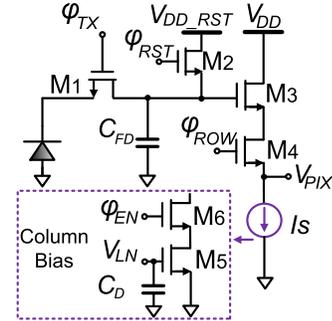


Fig. 2. Schematic of a 4T pixel.

of a pixel array, column readout circuits, row decoder/driver, column decoder, low-dropout regulator, bias/reference circuits, and digital logic controls. The pixel array contains  $128 \times 128$  pixels. The pitch of the pixel is  $10 \mu\text{m}$ . The column-parallel analog chains contain column amplifiers which realize analog correlated double sampling (CDS) function as well as provide a programmable gain from  $1 \times$  to  $8 \times$ , 10-bit single-slope analog-to-digital converters (SS-ADCs), and a static random-access memory (SRAM) array. In each column, the ADC digitizes the analog signal and transfers the data into the SRAM. During the next row's A/D conversion, the SRAM contents are read out through the sense amplifiers. The data will be further processed by an off-chip field-programmable gate array (FPGA). The ramp signal of the ADC,  $V_{RAMP}$ , is provided by an off-chip 12-bit digital-to-analog converter (DAC).

### A. Pixel Design and Layout

The pixel array consists of several different pixel structures. These pixel variations are designed to compare the linearity of different pixel architectures.

The schematic of a standard CMOS 4T pixel is shown in Fig. 2. The pixel consists of a pinned photodiode (PPD) and four transistors, including a charge transfer transistor (TX) which is labeled as (M1), a reset (RST) transistor (M2), an SF (M3), and a row select transistor (M4). The bias transistor (M5) provides a variable bias current  $I_S$  shared by multiple pixels in a column. The value of the bias current is controlled by the bias voltage  $V_{LN}$ . The enable transistor (M6) enables the bias current through the control signal  $\phi_{EN}$  during the readout phase of the image sensor which will be introduced later in this paper. In the other phase, the enable transistor is switched off to save power consumption. The decoupling capacitor  $C_D$  is added to stabilize the bias voltage.  $V_{DD\_RST}$  is the power supply of the RST transistor, and  $V_{DD}$  is the power supply of the pixel. The accumulated charge in the PPD is converted to a voltage by  $C_{FD}$  and read out through the SF. The voltage gain of the SF ( $G_{SF}$ ), from the floating diffusion (FD) node to the output of the pixel, is not a constant value due to the body effect and the output resistance of the current source [13].

The voltage gain of the SF, derived from a simple small signal analysis, is shown in the following equation. The value of  $G_{SF}$  has a complex voltage dependence on the output voltage of the pixel ( $V_{PIX}$ ), which deteriorates the linearity

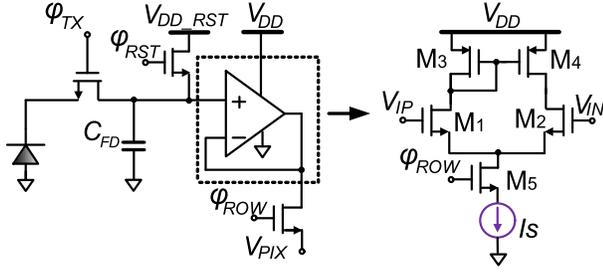


Fig. 3. Schematic of pixel V1.

performance of the pixel

$$G_{SF} = \frac{g_{m,SF} R_S}{(g_{m,SF} + g_{mb,SF}) R_S + 1} = \frac{g_{m,SF}}{(g_{m,SF} + \chi g_{m,SF}) + 1/R_S} = \left( 1 + \frac{\gamma}{2\sqrt{\varphi + V_{PIX}}} + \frac{\lambda\sqrt{I_S}}{\sqrt{2\mu C_{ox}} \left(\frac{W}{L}\right)_{SF} (1 + \lambda(V_{DD} - V_{PIX}))} \right)^{-1} \quad (1)$$

where  $g_{m,SF}$  is the gate–drain transconductance of the SF transistor;  $g_{mb,SF}$  is the bulk–drain transconductance of the SF transistor;  $R_S$  is the output resistance of the current source;  $\chi$  is the body-effect transconductance ratio;  $\gamma$  is the body-effect parameter;  $\lambda$  is the channel-length modulation parameter;  $\mu$  is the field-effect mobility;  $C_{ox}$  is the unit oxide capacitance;  $\varphi$  is the Fermi potential;  $W$  is the width of the SF transistor; and  $L$  is the length of the SF transistor.

In this chip, a new type of pixel design is proposed to reduce the nonlinear effects caused by the SF. In the pixel V1, a single-stage operational amplifier (OPA) in unity-gain configuration is used to drive the loading circuits, which is shown in Fig. 3. The single-stage amplifier structure is chosen based on the wide common mode range and low noise performance within limited pixel size.

In an amplifier, the output of the amplifier  $V_{OUT}$  can be expressed by the following equation, where  $V_{IN}$  is the input signal;  $a_2$  and  $a_3$  are the second- and third-harmonic distortion coefficients, respectively

$$V_{OUT} = A V_{IN} + a_2 V_{IN}^2 + a_3 V_{IN}^3 + \dots \quad (2)$$

The open-loop gain of the amplifier can be modeled as in the following equation, where  $B$  represents all high-order harmonic distortion which is related to the input value  $V_{IN}$

$$A_{OPA} = A(1 + B(V_{IN})). \quad (3)$$

In the unit gain configuration, the closed-loop gain of the amplifier follows

$$G_{OPA} = \frac{A_{OPA}}{A_{OPA} + 1} = \left[ 1 + \frac{1}{A(1 + B(V_{IN}))} \right]^{-1}. \quad (4)$$

The negative feedback can reduce the distortion of the amplifier which is related to the input signal [14]. A larger open-loop gain of the amplifier can thus better suppress the nonlinearity of the voltage buffer. However, the open-loop gain of an amplifier depends on the circuit structure. A telescopic or two-stage amplifier structure can achieve a larger

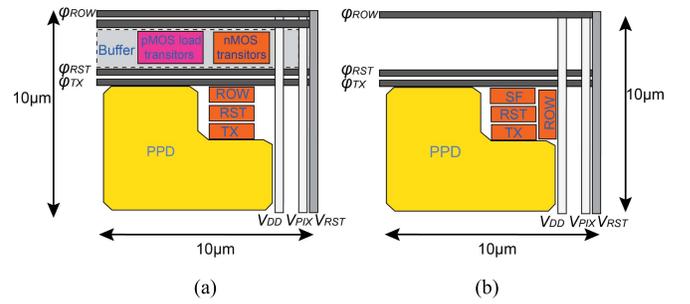


Fig. 4. (a) Conceptual layout of pixel V1. (b) Conceptual layout of pixel V2.

gain at the cost of noise and chip area. It is difficult to adopt a complex amplifier structure within the limited pixel size. In this design, the open-loop gain of the employed single-stage amplifier can reach 44 dB. According to the SPICE simulation, when the input voltage range is 1.7~2.7 V, the nonlinearity of the voltage buffer in pixel V1 is 0.12% while the nonlinearity of the SF is 2.2% in a reference 4T pixel V2.

Pixel V2, as shown in Fig. 2, is included to allow a comparison of the linearity performance. The conceptual layout of the pixels is shown in Fig. 4. The pixels share a pitch of 10  $\mu\text{m}$ . To compare the performance fairly, both pixels use the same photodiode design, while the pixel V2 did not fully utilize the pixel area. The photodiodes adopt a geometrical L-shaped design on the overlapping region with the transfer gate to achieve a large fill factor and improve charge transfer efficiency [15]. Both pixels achieve a 47% fill factor. To improve the linearity, the row selects and RST transistors in the pixels adopt low threshold voltage transistors (around 0.1 V). In pixel V2, the SF also uses the same low threshold voltage transistor to reduce the temporal noise [16]. The entire pixel array is surrounded by a guard ring to isolate the pixel array from substrate noise.

In Fig. 4, the input and load transistors of the buffer in the pixel V1 use a longer length to realize a larger gain, while that of the SF in the pixel V2 adopts an optimized size to achieve optimized noise performance. The other transistors such as the row selects and RST transistors use a minimal length allowed by the process to reduce charge injection.

In the pixel circuit, the integration capacitor on the FD contains several different types of capacitors, some of which are related to the gain of the SF and the output voltage of the pixel [7], [16]. Although the new pixel type V1 can reduce the nonlinearity caused by the SF, we still need to find a new solution to further reduce the nonlinearity caused by the  $C_{FD}$  and the following readout circuitry.

### B. Readout Circuitry

For the CISs, a column-parallel architecture is widely used. Compared with the other types of structures, column parallelism achieves an excellent tradeoff among power, speed, and chip size [17], [18].

Fig. 5 shows the schematic of the readout chain. The column-parallel chain contains a switched capacitor amplifier, an SS-ADC, and SRAM. The SS-ADC consists of a ramp

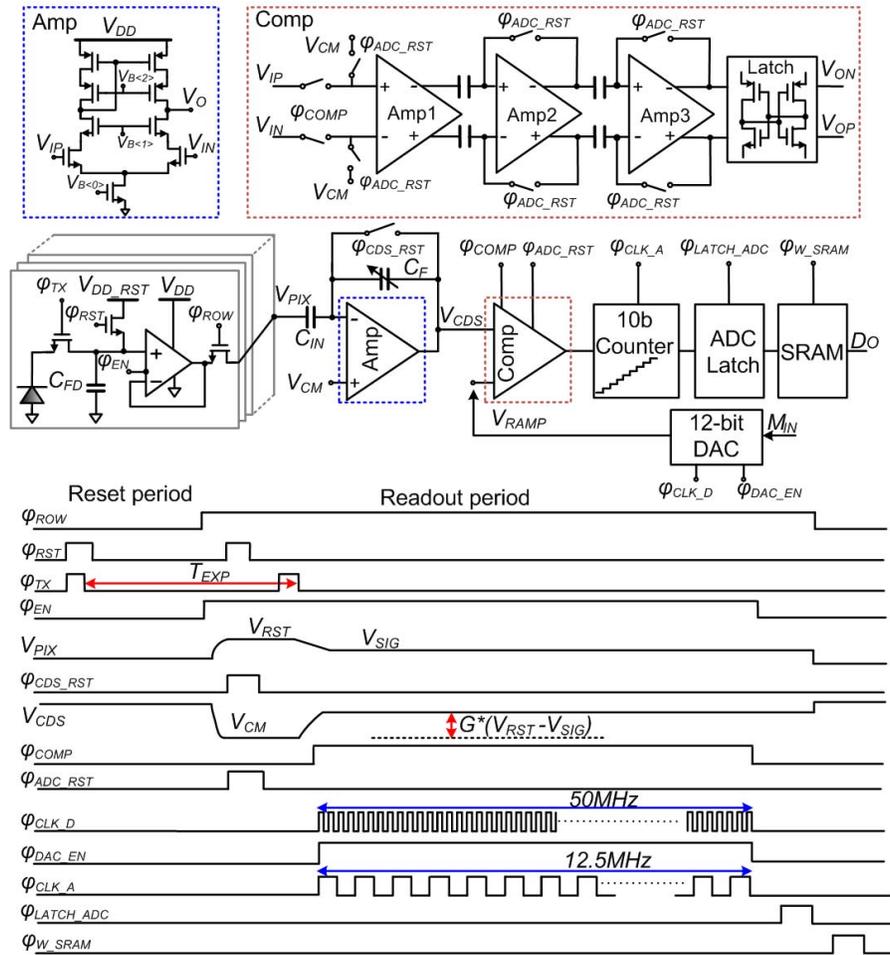


Fig. 5. Schematic and timing diagram of the readout chain.

generator, a differentially clocked comparator, a 10-bit ripple counter, and a 10-bit data latch. The comparator signal  $\phi_{CLK\_A}$  which operates at 12.5 MHz.

The timing of the CIS is divided into two phases. During the RST phase, the pulse  $\phi_{RST}$  and  $\phi_{TX}$  are set high to RST the PPD and FD. The second phase is the readout phase.  $\phi_{RST}$  appears high again to enable the readout process of the  $V_{RST}$  signal, then the column amplifier and the comparator in the ADC realize auto-zeros by setting  $\phi_{CDS\_RST}$  and  $\phi_{ADC\_RST}$  sequentially high.  $\phi_{CDS\_RST}$  is the RST signal of the column amplifier while  $\phi_{ADC\_RST}$  is that of the comparator. When the  $\phi_{CDS\_RST}$  is high, the output voltage of the column amplifier is set as the common voltage  $V_{CM}$  with the offset of the amplifier. Then, the pulse  $\phi_{TX}$  appears high to transfer the charge accumulated in the photodiode to the FD. As shown in Fig. 5, the time period between the two adjacent falling edges of  $\phi_{TX}$  defines the exposure time  $T_{EXP}$ . Then, the difference between RST value and the signal value is obtained as the input of the comparator. The CDS operation removes the FPN, the RST/kTC noise and most of the 1/f noise of the pixel [19].

An A/D conversion begins with the signal  $\phi_{COMP}$ . In this design, an on-board DAC is used to generate a ramp signal for the ADC.  $\phi_{DAC\_EN}$  is the enable signal of the DAC, which is

also the valid signal of the ramp signal. When  $\phi_{DAC\_EN}$  is high, driven by 50-MHz clock  $\phi_{CLK\_D}$ , the 12-bit DAC generates the ramp signal  $V_{RAMP}$  for the 10-bit ADC. Simultaneously, the column counter performs the comparator's output flips. Then, the latches synchronize the Do with the control signal  $\phi_{LATCH\_ADC}$ , then convey the data to SRAM by the signal  $\phi_{W\_ADC}$ .

In Fig. 5, the closed-loop gain ( $G$ ) of the switch-capacitor CDS column amplifier is set by the ratio of the input and feedback capacitors. The input capacitor of the column amplifier  $C_{IN}$  is fixed at 1 pF while the feedback capacitor  $C_F$  can be switched from 0.125 to 1 pF, which leads to a programmable gain from  $1 \times$  to  $8 \times$ .

In the column amplifier, a telescopic cascode OPA is employed. The common voltage  $V_{CM}$  is applied at the positive input of the OPA while the capacitor  $C_{IN}$  is placed between the negative input of the OPA and the output of the pixel. The differential input structure of the OPA is better at rejecting common mode noise at the cost of more noise and power [13]. The bias circuit provides the bias voltages  $V_{B(0)}$  to  $V_{B(2)}$ . The charge injection of the RST switch can be reduced by using dummy transistors in the switch.

In this paper, the SS-ADC structure is chosen based on the principle of the calibration method, as well as its advantage

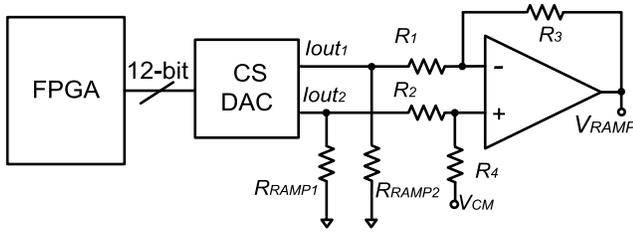


Fig. 6. Schematic of the ramp generator based on a CS-DAC.

of relatively high resolution, high linearity with a small area, and low power consumption [20], [21].

One of the primary sources of FPN is the ADC's offset, which can bring vertical or column fixed-pattern noise in the image. It can be reduced by either offset cancellation techniques or digital CDS [21]. In this paper, the comparator achieves a small offset less than half least significant bit (LSB) by applying a combined offset cancellation technique [22] shown in Fig. 5. A fully differential architecture is adopted in the comparator to be more resistant against common mode noise.

Another critical block in the SS-ADC is the ramp generator, whose performance determines the accuracy and linearity of the ADC [23], [24]. In this paper, combined with the calibration method, a 12-bit on-board current steering DAC (CS-DAC) is employed to provide a ramp signal  $V_{RAMP}$ . A higher resolution DAC can provide a more linear ramp signal for the ADC. Due to the advantages of high speed and high resolution, the structure of current steering is chosen for the DAC. The schematic of the ramp generator is shown in Fig. 6.

As shown in the schematic of Fig. 6, the 12-bit CS-DAC converts the digital input signal from the FPGA into two differential current outputs. The loading resistors  $R_{RAMP1}$  and  $R_{RAMP2}$  convey the current outputs to two differential voltage outputs. Then, a high bandwidth OPA, combining with  $R_1$ – $R_4$ , transforms the differential analog voltage to the single-ended ramp signal  $V_{RAMP}$ , which is shared by all column ADCs.

### C. Calibration Method

In addition, the pixel optimization, this CIS utilizes a digital calibration method, to further reduce the nonlinear errors, which is illustrated in Fig. 7.

The image sensor has two modes: normal mode and calibration mode. In the normal mode shown in Fig. 7(a), the image sensor works conventionally. The operation goes as follows:  $M_{IN}$  is the digital input code of the DAC, which increases from 0 to 4095 ( $2^{12} - 1$ ) evenly, with which the 12-bit DAC generates a linear ramp signal  $V_{RAMP}$  for the 10-bit ADC. During the linearity measurements, the intensity of the incoming light is fixed. The number of incident photons coming to the sensor is evenly increasing by varying the exposure time from  $1 \times T_{EXP}$  to  $1024 \times T_{EXP}$ . The Do of the 10-bit ADC is captured and saved into the SRAM within each exposure time.  $N_{IN}$  is the exposure sequence. Due to the nonlinearity of the imaging system, the transfer function from the incremental injected photons to the individual Do is not linear, which could be observed in Fig. 7(a).

Based on the nonlinear transfer function of the CIS, the nonlinearities of the whole system can be analyzed. The nonlinear behavior of the CIS is copied into the ADC circuitry and to create a new nonlinear ramp signal for the ADC. In the calibration mode illustrated in Fig. 7(b), after the transfer curve of the image sensor, has been captured in normal mode, a new ramp signal  $V_{RAMP\_C}$  is used to realize the calibration.  $M_{IN\_C}$  is the corresponding output sequence after mapping and interpolation. The mapping process removes the offset and the gain errors of the data collected from the SRAMs. Interpolation is needed for the 12-bit DAC. After the interpolation, the calibrated ramp signal  $V_{RAMP\_C}$  contains the information of the nonlinearities of the pixel and of the following readout circuitry. The new ramp signal will cancel out these nonlinearities in the output signal after calibration.

### D. Behavior Model

At the architectural level, various behavioral modeling languages, such as MATLAB, Simulink, and Verilog-A, are commonly used in the circuit design to speed up the simulation with an acceptable accuracy [25], [26]. In this paper, a hybrid behavioral model of the CIS is built for the validation of the proposed calibration algorithm and performance estimation.

In [7], based on the analysis of the nonlinear sources of the image sensor system, a mathematic model of the pixel's response using MATLAB has been presented. The capacitance–voltage characteristic of the  $C_{FD}$  and the nonlinearity of  $G_{SF}$  are well investigated.

Fig. 8 shows a behavioral model of the CIS system with the digital calibration mentioned earlier. Different description languages are used to extract behavioral models of the optical and electronic components. The input of the signal chain is the number of incident photons ( $P$ ) which is regarded as linear. QE is the quantum efficiency of the pixels. Within a constant photodiode size, the average number of integrated electrons ( $Q$ ) increases linearly with the exposure time. The electrons are integrated on  $C_{FD}$  and converted into an analog voltage value. The voltage is read out through the in-pixel voltage buffer either realized by the SF or by the analog buffer. After the pixel's signal is sent to the column amplifier, the following ADC circuit digitalizes the analog voltage. The final output is the digital number.

Using the same technology, based on the proposed model in [7], the same algorithm is used to build a compact behavioral model of the pixels V1 and V2 with MATLAB. The next analog, mixed-signal circuits, and digital processing circuits are described by Verilog-A. In this heterogeneous system model, the nonideality factors of the blocks in the red line are considered, which have been listed in Table I.

In Fig. 9, the primary vertical axis plots the simulation results of the corresponding gain of the voltage buffers in both pixels with the proposed model in [7], whereas the secondary vertical axis depicts the capacitance–voltage characteristics of the  $C_{FD}$ . The horizontal axis is the output voltage range of the pixel.

In the above-mentioned simulation,  $V_{DD\_RST}$  is set as 2.7 V, while the power supply of the pixel  $V_{DD}$  in the pixels is 3.3 V. The bias current is 10  $\mu A$  for both pixels. The red and orange

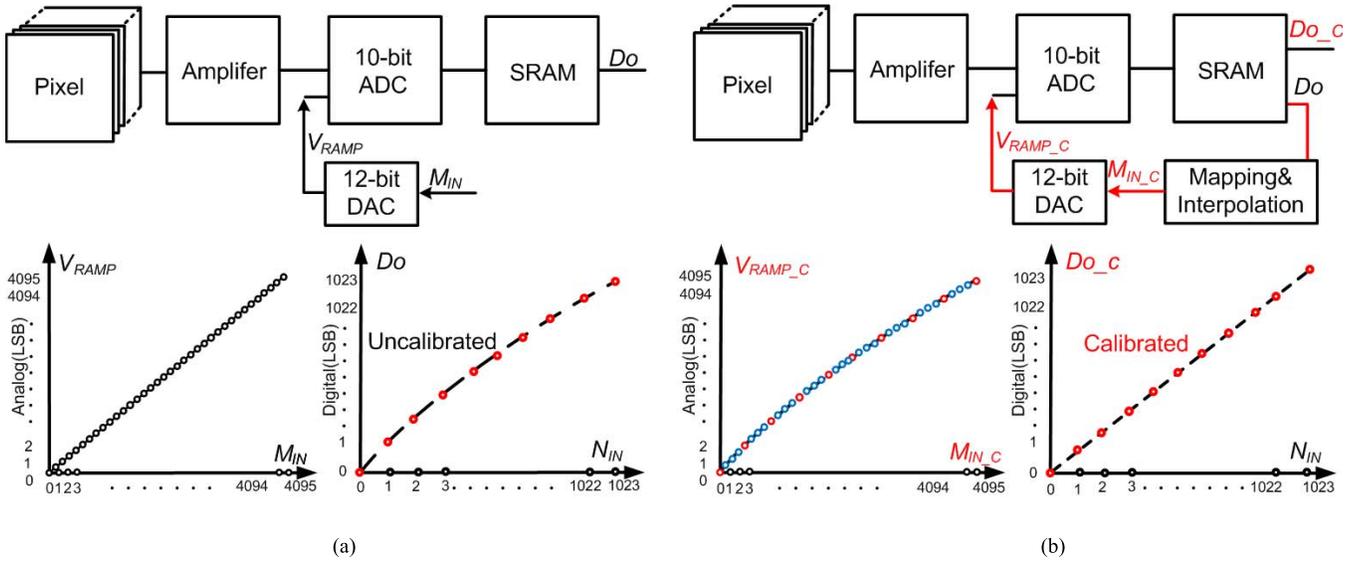


Fig. 7. (a) Operation in normal mode of the CIS. (b) Operation in calibration mode of the CIS.

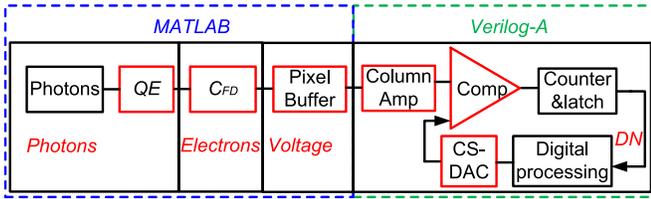


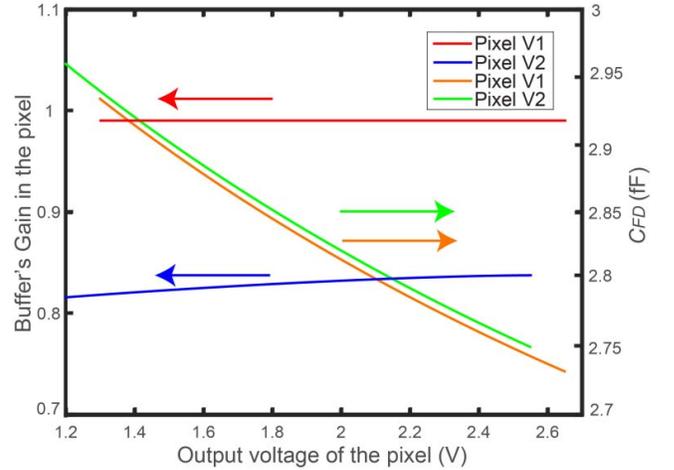
Fig. 8. Behavioral model of the CIS system.

 TABLE I  
 NONIDEALITIES IN CIS SYSTEM

Blocks	Nonidealities in the system	Description language
QE	Differences among pixels	MATLAB
Integration capacitor	Dependence of the output voltage, dependence of the buffer's gain, nonuniformity of the capacitor	MATLAB
Voltage buffer (Pixel V1)	Noise, gain error, gain nonuniformity	MATLAB
SF (Pixel V2)	Noise, gain dependence of the output voltage, gain nonuniformity	MATLAB
Column amplifier	Gain error, offset, nonuniformity of the capacitor	Verilog A
Comparator	Gain error, offset, noise, delay time	Verilog A
CS-DAC	Offset, noise, nonuniformity of the current sources	Verilog A

lines represent the modeling results of the pixel V1 while the blue and green lines give that of the pixel V2. Configured in a closed loop, the pixel V1 realizes a constant nearly unity gain, whose value is only determined by the open-loop gain of the amplifier. For the 4T pixel V2, the gain of SF is not constant. It increases with the output voltage of the pixel  $V_{PIX}$ . The output voltage of the pixel V2 is also lower than that of the pixel V1 due to the SF's threshold voltage.

Fig. 9 also shows the simulation results of the capacitance–voltage characteristics of the  $C_{FD}$  in the pixels V1 and V2,


 Fig. 9. Output voltage versus gain of the pixel's buffer and  $C$ – $V$  characteristic of  $C_{FD}$ .

where the FD capacitances decrease with the output voltage of the pixel. The average values of the capacitances over the whole range of the output voltage are chosen as the modeled value of the  $C_{FD}$ .

For the nonlinearity modeling, the 4T pixel is used to illustrate the procedure.  $G_{SF}$  and  $C_{FD}$  depend on the value of the pixel's output voltage  $V_{PIX}$ ; it is difficult to analyze the linearity performance of the pixel's whole output range with the large signal analysis. With a small signal model, we can derive the relationship between  $Q$  and the pixel's output voltage  $V_{PIX}$ , which is expressed in the following equation:

$$\delta Q = -\frac{C_{FD}(V_{PIX})}{G_{SF}(V_{PIX})}\delta V_{PIX}. \quad (5)$$

By integrating  $V_{PIX}$  from  $V_{PIX\_MAX}$  to  $V_{PIX\_MIN}$  shown in (5), the curve between the number of the integrated charge and pixel's output voltage can be obtained; the nonlinearity of the pixel can also be characterized. In the following equation,  $V_{PIX\_MIN}$  is the minimal value of the pixel's output voltage

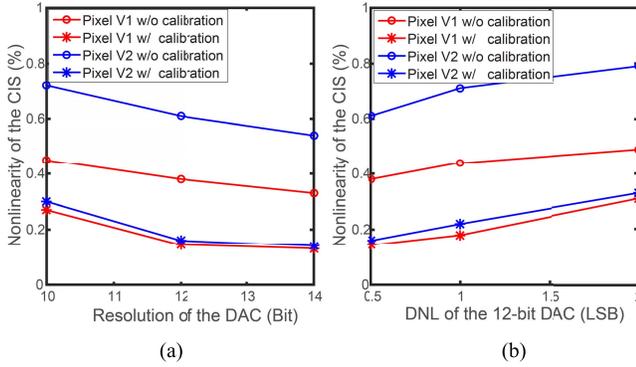


Fig. 10. Modeling results of the linearity performance. (a) With different resolution DACs. (b) With different DNL values of the DAC.

while  $V_{PIX\_MAX}$  is the maximum value:

$$Q = - \int_{V_{PIX\_MAX}}^{V_{PIX\_MIN}} \frac{C_{FD}(V_{PIX})}{G_{SF}(V_{PIX})} dV_{PIX}. \quad (6)$$

After further conversion by the following readout circuitry described in Verilog A, the nonlinearity of the image sensor can be characterized.

This behavioral model of the CIS system not only provides an early validation of the image sensor calibration algorithms but also gives guidance to the circuit design. The DAC's resolution and linearity performance both affect the nonlinearity of the image sensor and the effectiveness of the calibration method. Fig. 10 shows the nonlinearity simulation results of the CIS based on the proposed hybrid model.

In Fig. 10(a), it can be seen that when the resolution of the DAC increases from 10 to 14 bit and with a differential nonlinearity (DNL) of the DAC always less than half LSB, the linearity of the image sensor system is improved with the calibration method. When the DAC's resolution increases from 12 to 14 bit, the linearity improvement is limited. To reduce the operating time and the complexity of the system, a 12-bit DAC is employed to provide a ramp signal for the 10-bit ADC in this design.

Fig. 10(b) plots the modeling results of the CIS's nonlinearity build on a 12-bit DAC with different DNL values. When the DNL of the DAC is less than half LSB, the nonlinearity of the whole CIS system can be improved from 0.38% to 0.14%, and 0.61% to 0.16%, respectively, for pixels V1 and V2, with the assistance of the calibration method. However, the improvement is less effective when the linearity performance of DAC deteriorates. Therefore, a high-resolution DAC with a good linearity performance is needed.

### III. EXPERIMENTAL RESULTS

The proposed CIS has been fabricated in a 0.18- $\mu\text{m}$  1P4M CIS process technology. Fig. 11 shows a micrograph of the fabricated chip. A pixel array of 128 (H)  $\times$  128 (V) has been implemented. The size of the chip is 2.6 mm  $\times$  5 mm. An Altera Cyclone II FPGA is used to provide digital control signals and send the stored data to a computer via a camera link interface. LabVIEW is used to capture and analyze the data.

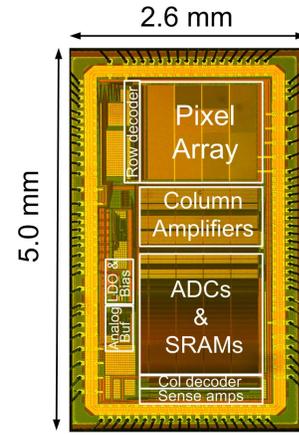


Fig. 11. Chip microphotograph.

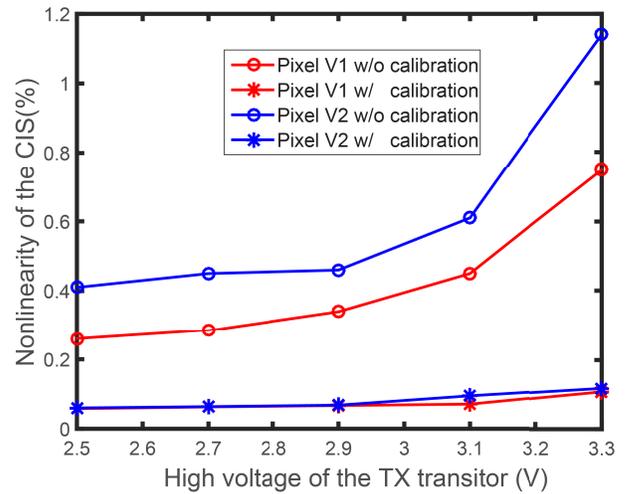


Fig. 12. Nonlinearity performance of the pixels with different  $V_{THX}$ .

In this paper, the linearity performance is the most important index. A tungsten-halogen lamp is used to provide a constant illumination source. The number of photons coming to the image sensor is changed by increasing the exposure time from 1 to 1024  $\mu\text{s}$  evenly. Fig. 12 shows the nonlinearity results of the pixels V1 and V2 with different values of  $V_{TXH}$ , which is the high voltage of the transfer transistor in the pixel.

In the measurement,  $V_{DD\_RST}$  is set as 2.7 V as was the setting in the simulation, which is lower than the power supply of the pixel. This is a requirement of the linear input range for the analog buffer in the pixel V1 at the cost of a lower full well capacity. The value of  $V_{TXH}$  is related to the characteristics of the pixel, such as the dark current and FPN [27]. In the measurement,  $V_{TXH}$  is variable from 2.5 to 3.3 V. The input range of the ADC is set as 1 V. All linearity evaluations are done with a window containing 28  $\times$  28 pixels averaged over the 200 frames captured. According to the measurement results, a higher value of  $V_{TXH}$  leads to a worse linearity of the CIS. When  $V_{TXH}$  equals 2.5 V, the nonlinearity of pixels V1 and V2 is 0.24% and 0.41%, respectively. When  $V_{TXH}$  equals 3.3 V, the nonlinearity of the pixel V1 is 0.76% while that of the 4T pixel V2 is 1.14%.

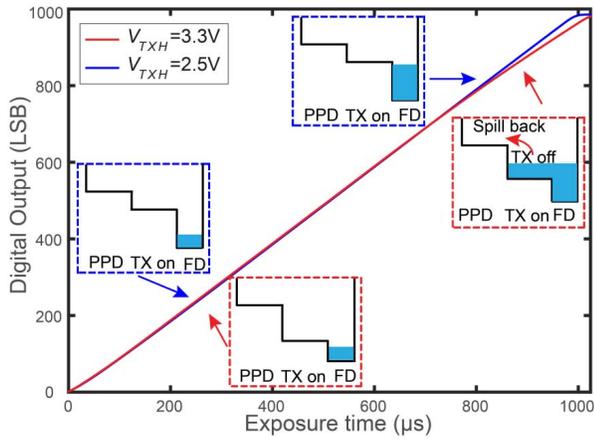


Fig. 13. Digital output of the pixel V1 versus exposure time.

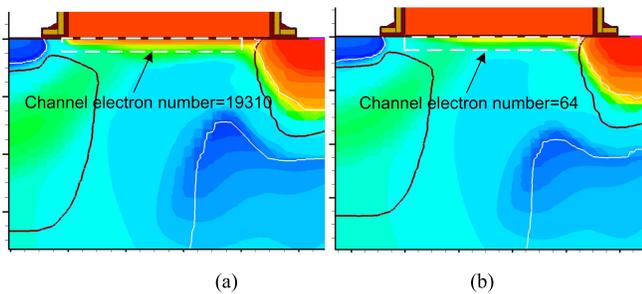


Fig. 14. Electron density during the end of charge transfer phase. (a) High illumination. (b) Low illumination.

In [28], it is explained that the value of  $V_{TXH}$  affects the pixel's performances due to the charge spillback effect. In Fig. 13, the transfer curves of the pixel V1 with different  $V_{TXH}$  values are plotted.

In the small signal region, the charge transfer channel under the transfer transistor is always in the depletion mode. When the number of transferred electrons is increased, the potential of the FD is becoming lower. In the large signal region, the charge transfer channel enters into the inversion mode. Electrons can spillback to the PPD when the TX is switched off. A higher  $V_{TXH}$  enables the channel to enter the inversion mode earlier. This explains why a pixel with a higher  $V_{TXH}$  has a worse linearity performance. Therefore, the linearity with a lower  $V_{TXH}$  is better, if the charge transfer can be completed with this lower value and or if the transfer time is long enough to avoid image lag [29].

We use simulation results of Sentaurus TCAD tool to verify the above-mentioned analysis. Fig. 14 plots the electron density at the end of the charge transfer phase with high and low light illumination. In Fig. 14(a), with highlight illumination, the channel of TX accumulates many electrons and enters into the inversion mode due to the decreasing voltage on FD, while the channel of TX in Fig. 14(b) is working in the depleted mode with a few numbers of accumulated electrons.

As pointed out in [29], after the TX was closed, the spillback effect can encourage the electrons in the channel to return to the FD, which will worsen the linearity performance of the pixels.

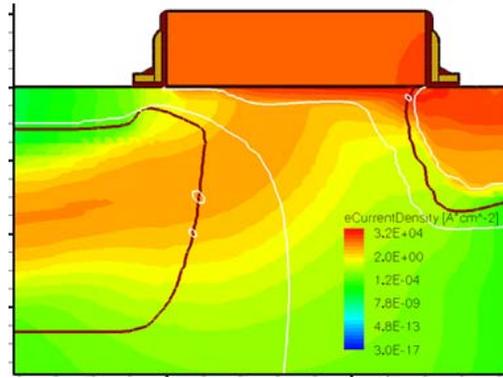


Fig. 15. Electron current density: 1 ns after TX is switched off.

Similar to the conventional nMOS transistor, a higher voltage on the gate can accumulate more electrons in the channel, it also happens to the TX transistor. Fig. 15 shows the simulated electron current density underneath the TX, 1 ns after the TX was turned off. In the simulation, when  $V_{TXH}$  is equal to 3.3 V, the ratio of the electrons flow back to the PPD over the total accumulated charges is 0.6%. When  $V_{TXH}$  reaches 3 V, the ratio becomes smaller which means fewer electrons get back to the PPD. Therefore, the linearity in the high illumination region becomes better.

Although a high  $V_{TXH}$  leads to a degrading linearity performance, the calibration method proposed improves the pixels' linearity effectively. In Fig. 12, the blue lines represent the measurement results without calibration, and the red lines represent those with calibration. After the calibration, the pixels have better linearity results. When  $V_{TXH}$  equals 2.5 V, the nonlinearity of the pixel V1 is 0.24% while that of the pixel V2 is 0.41% before calibration. After calibration, the averaged output of both pixel array achieves a nonlinearity less than 0.06%.

Fig. 16 plots the nonlinearity results for each pixel in the pixel arrays V1 and V2. We can observe obvious improvement on linearity for each pixel with calibration.

Fig. 17 shows the corresponding histogram of the nonlinearity results in the pixel array. Mean values of the nonlinearity of single pixel in the pixel arrays V1 and V2 are, respectively, 0.34% and 0.48% without calibration. With the assistance of the calibration, the nonlinearity values of pixels V1 and V2 become 0.14% and 0.15%, respectively.

It is also easy to observe the spillback effect from the mean-variance curves. Fig. 18(a) shows the mean-variance curves of the pixel V1 with different values of the  $V_{TXH}$ . When  $V_{TXH}$  is higher than 3.0 V, the digital response at the saturation region is very nonlinear. Fig. 18(b) plots the mean-variance curves of the pixel V1 after calibration. When  $V_{TXH}$  equals 3.3 V, the mean-variance curves which is close to the saturation region becomes normal. In fact, the calibration cannot cancel off the spillback effect; however, it can calibrate the Do. Pixel V2 shows the same trends. This is another way to validate the effectiveness of the calibration method.

The calibration method is also valid for the other settings. Fig. 19(a) shows the linearity improvement for the pixels V1 and V2 as a function of the gain of the column amplifier.

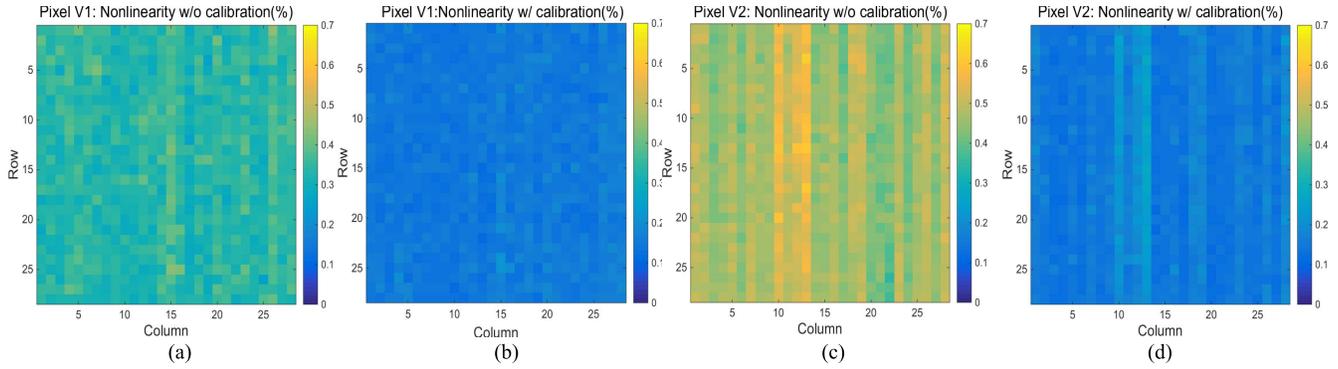


Fig. 16. Nonlinearity of each pixel. (a) Pixel V1 without calibration. (b) Pixel V1 with calibration. (c) Pixel V2 without calibration. (d) Pixel V2 with calibration.

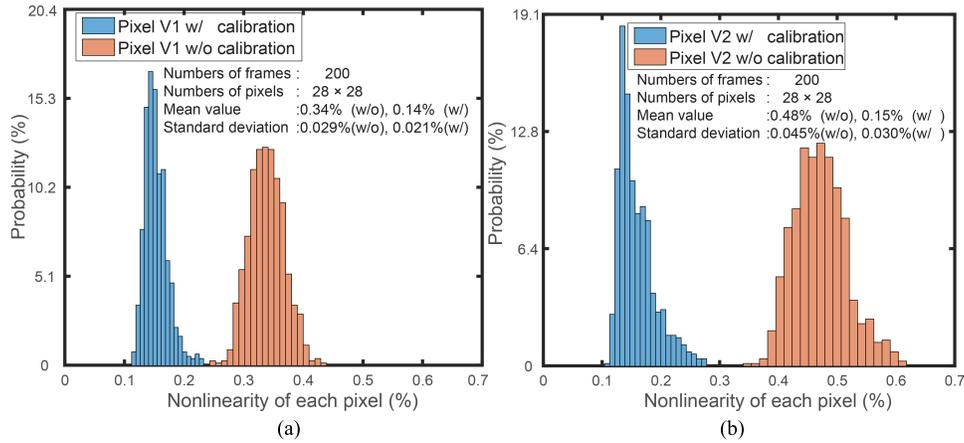


Fig. 17. Histogram of the nonlinearity. (a) Pixel V1 array. (b) Pixel V2 array.

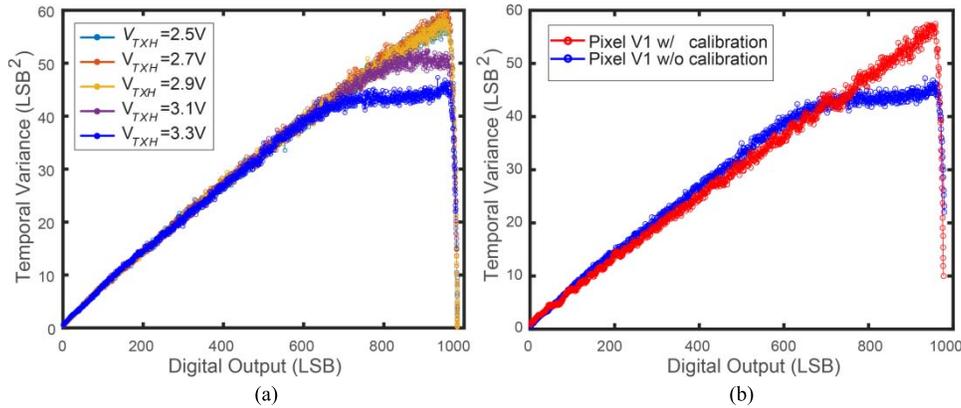


Fig. 18. (a) Mean-variance curves of pixel V1 with a different  $V_{THX}$ . (b) Mean-variance curves of pixel V1 with calibration ( $V_{THX} = 3.3$  V).

When the gain of the column amplifier varies from  $1\times$  to  $8\times$ , the nonlinearity of the CIS has been improved with the proposed calibration method.

In the linearity measurement mentioned earlier, a constant illumination is used and the minimal exposure time is  $1\ \mu\text{s}$ . To prove the calibration method is useful in different illumination conditions, the same input code of the ramp signal extracted from the measured results with  $1\text{-}\mu\text{s}$  unit exposure time is used. Then, we change the illumination intensity and exposure time, and finish the nonlinearity measurements

with calibration. From Fig. 19(b), we can conclude that the calibration method is valid under different light intensities.

Fig. 19(c) plots the nonlinearity performances of the CIS at different wavelengths. A monochromator ranges from 300 to 1000 nm, and a small-size integrating sphere is used to obtain the desired bandwidth of light. By extracting the Do of the CIS at the wavelength of 460 nm, the same calibration code was used to calibrate the CIS at the other wavelengths. Fig. 19(c) shows that the calibration method is valid for

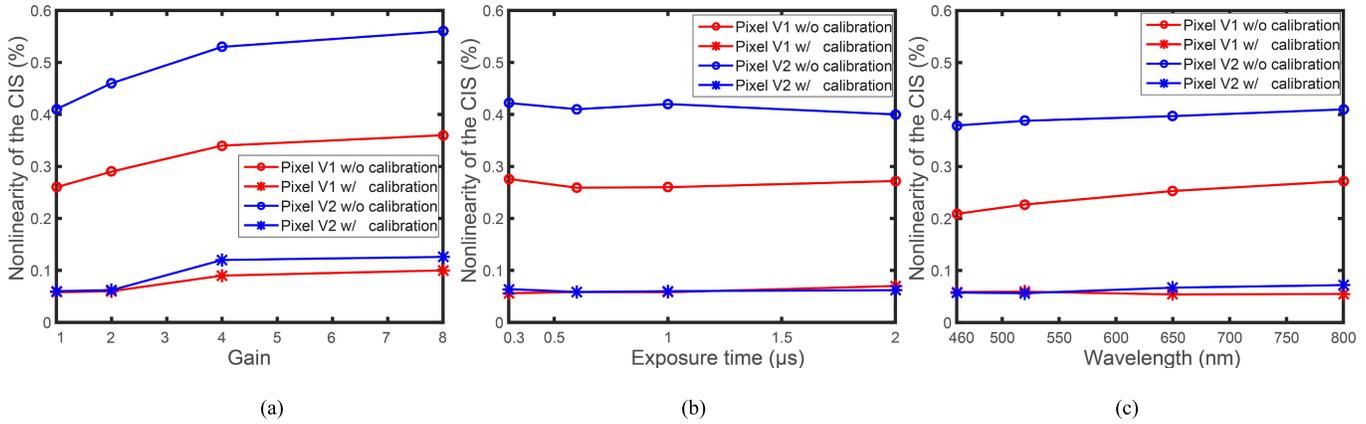


Fig. 19. Nonlinearity performances of the pixels as a (a) function of the gain, (b) function of the exposure time, and (c) function of the wavelength.

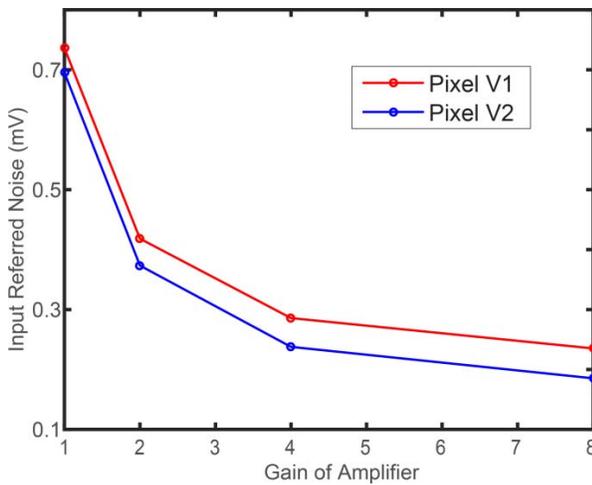


Fig. 20. Input-referred noise versus column amplifier gain.

the CIS at different wavelengths, which is of great importance to color image sensors.

Pixel V1 not only attains a better linearity performance but also realizes a unity gain, and hence, increases the conversion gain of the pixel. Based on the behavioral model introduced earlier, the simulation results of the conversion gain for the pixel V1 is  $55.7 \mu\text{V}/e^-$ , while that of the pixel V2 is  $46.9 \mu\text{V}/e^-$ . The measured results of the conversion gain are 56.8 and  $45.3 \mu\text{V}/e^-$  for pixel V1 and pixel V2, respectively. The measured results are in line with the simulation results.

Compared with the standard 4T pixel, pixel V1 introduces more input referred noise in the voltage domain. Fig. 20 shows the input-referred noise voltage in dark for the proposed pixels with different amplifier gain settings. Pixel V1 has a slightly higher input-referred noise than that of the 4T pixel V2. The programmable gain of the column amplifier efficiently suppresses the pixel’s input-referred noise. The input-referred noise of pixels V1 and V2 is, respectively, 234 and  $189 \mu\text{V}_{\text{rms}}$  at an analog gain of  $8\times$ . Nevertheless, the pixel V1 achieves a lower input referred noise in the electron domain due to the larger conversion gain, compared with 4T pixel V2. When the gain of the column amplifier is  $8\times$ , the readout noise is 4.12 e- for pixel V1 and 4.17 e- for pixel V2.

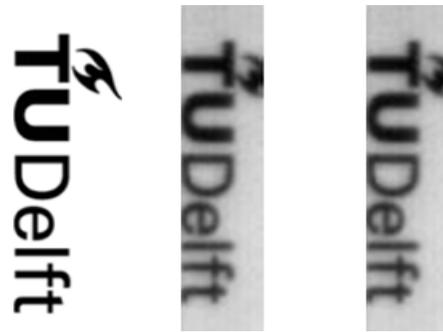


Fig. 21. (a) Sample photograph. (b) Captured photograph (Pixel V1) without calibration. (c) Captured photograph (Pixel V1) with calibration.

The whole pixel array is  $128 \times 128$  in this design, which contains several different types of pixel designs. In this paper, pixels V1 and V2 are used to compare and validate the effectiveness of the calibration method. For image demonstration purposes, we choose the images taken by the pixel V1 array whose size is  $128 \times 32$ . Fig. 21(a) shows a sampled photograph while Fig. 21(b) and (c) shows the captured photograph by pixel V1 array at a frame rate of 60 frames/s without and with calibration.

From Fig. 21, it is not easy to observe the linearity improvement from the monochrome photograph. In the following design, color filters will be added on the sensor to get a clear visual comparison on the effectiveness of the calibration.

The measurement results of the proposed image sensor are summarized in Table II. Compared with previously published works [6], [8]–[10], [30], this paper improves the state-of-the-art performance in linearity. Pixel V1 achieves superior linearity result to the traditional 4T pixel. After calibration, both pixels have a nonlinearity which is less than 0.06%.

In contrast to off-chip calibrations, this method can reduce the following off-chip processing time and improve the system efficiency, as well as attain better linearity results. The proposed calibration method can realize high linearity without adopting a special pixel design.

The linearity performance of the DAC decides the effectiveness of the calibration. A high resolution and highly linear on-chip DAC is preferred. The transfer curve of the

TABLE II  
PERFORMANCE COMPARISON

Reference		This Work		[6]	[8]	[9]	[10]	[30]	
Linearity improvement techniques		<b>Pixel optimization &amp; digital calibration</b>		LUT calibration	Feedback mechanism	Pixel optimization	Pixel optimization	N/A	
Array size		<b>128 × 128</b>		640 × 480	54 × 60	64 × 128	128 × 160	1032 × 1024	
Global/Rolling shutter		<b>RS</b>		RS	RS	RS	RS	RS	
ADC Architecture		<b>10-bit SS-ADC</b>		10-bit ADC	Off-chip 14-bit ADC	Off-chip 16-bit ADC	12-bit SS-ADC	13–19-bit Folding + Cyclic ADC	
Process	nm	<b>180</b>		180	180	180	180	180	
Pixel size	μm <sup>2</sup>	<b>10 × 10</b>		6.2 × 6.2	25 × 25	11 × 11	12 × 10	7.5 × 7.5	
Fill factor	%	<b>47</b>		49	68	51	36	52	
Frame rate	fps	<b>60</b>		30	100	N/A	40	4	
Pixel type		<b>Buffer</b>	<b>4T</b>	3T	4T current mode	4T	4T optimized	CTIA	4T
Conversion gain	μV/e-	<b>56.8</b>	<b>45.3</b>	N/A	N/A	71	122	40	67
Read Noise	μVrms	<b>234</b>	<b>189</b>	N/A	1560	92	134	656	80
	e-rms	<b>4.12 (Gain=8)</b>	<b>4.17 (Gain=8)</b>	50	N/A	1.3 (Gain=16)	1.1 (Gain=16)	16.4 (Gain=8)	1.2
Full well capacity	e-	<b>17270</b>	<b>20960</b>	N/A	1M	8730	3739	30613	14950
Dynamic range	dB	<b>72.4</b>	<b>74</b>	72	52	77	71	65	82
Nonlinearity	% (w/o calibration)	<b>0.24</b>	<b>0.42</b>	1.8	1.7	0.3	0.2	0.095	0.32
	% (w/ calibration)	<b>0.058</b>	<b>0.06</b>	0.5	0.51				

CIS captured at low-speed clock can be used to calibrate the Do where the DAC works at a high speed. Therefore, this method can also be applied to the commercial CIS which has a large pixel array.

#### IV. CONCLUSION

In this paper, a highly linear CIS is proposed. The implemented image sensor utilizes a new type pixel design, leading to better linearity and larger pixel conversion gain compared to the traditional 4T pixel.

Furthermore, the novel feature of on-chip linearity calibration significantly improves the linearity of the pixel and reading circuit.

The sensor chip is fabricated in 0.18-μm CMOS CIS technology, and silicon experiments results show that the on-chip linearity correction efficiently suppressed the sensor nonlinearity to 0.06% for both pixels.

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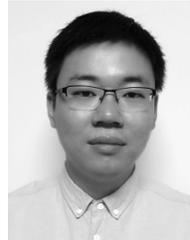
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**Fei Wang** was born in Jinhu, Jiangsu, China, 1984. He received the M.S. degree in microelectronics engineering from Southeast University, Nanjing, China, in 2009.

He was with ZTE Corporation, where he was involved in CMOS data converter design. He joined the Electronic Instrumentation Laboratory, TU Delft, Delft, The Netherlands, where he was involved in integrated circuit and CMOS image sensor design. His current research interests include highly linear CMOS image sensor design.



**Liqiang Han** received the M.S. and Ph.D. degrees from the School of Electronic Information Engineering, Tianjin University, Tianjin, China, in 2012 and 2016, respectively.

He was a Visiting Student with the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands, in 2015. Since 2016, he has been a Post-Doctoral Researcher with Tianjin University. His current research interests include the global shutter and high-quantum efficiency pixel design.



**Albert J. P. Theuwissen** (F'02) received the M.S. and Ph.D. degrees in electrical engineering from the Catholic University of Leuven, Leuven, Belgium, in 1977 and 1983, respectively.

In 1983, he was a member with the Scientific Staff of Philips Research Laboratories, Eindhoven, The Netherlands. In 1991, he was the Department Head of the Imaging Devices Division, where he was involved in CCD as well as CMOS solid-state imaging activities. In 2001, he was a Part-Time Professor with the Delft University of Technology, Delft, The Netherlands. In 2002, he was a Chief Technological Officer with DALSA Corporation, Eindhoven. In 2007, he started his own company Harvest Imaging, Bree, Belgium, where he was involved in consulting, training, teaching, and coaching in the field of solid-state imaging technology. He has authored or co-authored over 200 technical papers in the solid-state imaging field and issued several patents.

Dr. Theuwissen was the President of the International Image Sensor Society in 2017. He was a recipient of the Electronic Imaging Engineer of the Year in 2010.