

## Temperature Effect on the Linearity Performance of a CMOS Image Sensor

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**Abstract**—This article focuses on the effect of the operating temperature of a CMOS image sensor (CIS) on the pixel performance, especially the linearity behavior. As the temperature increases, the value of the integration capacitor  $C_{FD}$  in the floating diffusion (FD) region increases as well. Moreover, the gain of the in-pixel voltage buffer decreases. These two factors lead to a reduced value of the conversion gain. Due to an increase in the nonlinear part of the  $C_{FD}$ , the linearity of the CIS at a higher temperature will deteriorate. A digital calibration method proposed previously is used to improve the linearity of the CIS. Measurement results conducted on a prototype image sensor, designed with a 0.18- $\mu\text{m}$  CIS technology, agree well with an updated analytical model of the CIS and demonstrate an efficient linearity improvement at different temperatures.

**Index Terms**—Electromagnetic wave sensors, calibration, CMOS image sensor (CIS), linearity, pixel, temperature.

### I. INTRODUCTION

Recently, self-driving cars have become a topic of interest. Image sensors, which are the eyes of an autonomous vehicle, have experienced impressive growth [1]. However, this application brings challenges on the image sensor design. An image sensor with high speed, high dynamic range, and an excellent linearity should be able to withstand harsh temperatures due to complex driving environments, such as blazing sunlight and large temperature variations.

The imaging performance of the CMOS image sensor (CIS) is significantly affected by temperature, of which the most notable is the dark current, which is strongly temperature-dependent [2]. The temperature dependence of the full well capacity (FWC) in a CIS has also been discussed in [3]. Using an analytical model of the pinned photodiode, the authors successfully explained the FWC variations as a function of temperature and verified the conclusion through a test chip. Based on the bias current's temperature characteristics of the pixel, a temperature compensation method is introduced in [4] to stabilize the output of the CIS against any temperature variations. However, the temperature effect on the linearity performance of the image sensors has not been well studied.

For image sensors used in autonomous vehicles, linearity is a crucial parameter, especially when the output signal strongly depends on the absolute measurements of the light input.

In our previous studies, a MATLAB model of the CIS [5] is proposed to assist the linearity analysis of the CIS. Furthermore, a digital calibration method is presented to improve the linearity performance of a prototyped CIS [6].

As introduced in [5], the linearity of the CIS is mainly constrained by the transfer function of the pixel, where the voltage gain of the voltage buffer and the integration capacitor in the pixel are two determining

factors. Both factors have a complicated temperature dependence, which will be discussed in the following section.

In this article, the temperature effects on the linearity characteristic of the CIS are analyzed. By adding the temperature model of the elements in the proposed model [5], it is possible to perform a temperature-dependent linearity modeling of the CIS. The analysis was experimentally verified by using two types of pixels, fabricated with a 0.18- $\mu\text{m}$  commercial CIS technology. Measurement results are in line with the modeling results. The results also demonstrate an efficient linearity improvement at different temperatures with the assistance of the calibration method proposed in [6].

### II. DEVICE UNDER TEST

The device tested in this article is a rolling-shutter CIS with a  $128 \times 128$  pixel array, manufactured through a 0.18- $\mu\text{m}$  CIS process [6]. The pixel array contains several types of pixel designs. A column amplifier provides a variable gain. Next, a single-slope analog to digital converter (ADC) converts the analog signal to a digital output. In this article, two types of pixels are selected to analyze the temperature characteristics. Pixel V1 is a linearity-optimized pixel, which uses an operational amplifier (OPA) in a closed-loop configuration to reduce the nonlinearity caused by the source follower (SF) in the 4 T pixel V2. Within a limited pixel size, pixel V1 achieved a better linearity at the cost of the fill factor and noise performance. Fig. 1 shows the row select (ROW) and reset transistors (RST) in both pixels, as well as the SF in pixel V2, which uses a transistor with a low threshold voltage  $V_{th}$ .

### III. TEMPERATURE ANALYSIS

In a conventional 4 T pixel, the voltage gain of the SF  $G_{SF}$  varies with the pixel output voltage  $V_{PIX}$  [5], which leads to a pixel-related

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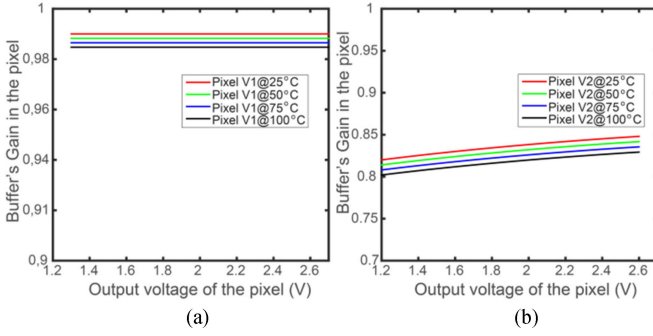


Fig. 2. Buffer's gain versus  $V_{PIX}$ . (a) Pixel V1. (b) Pixel V2.

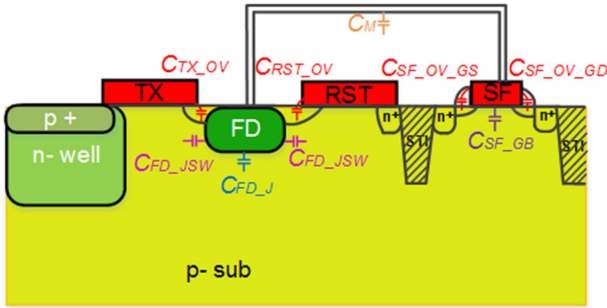


Fig. 3. Cross-sectional view of  $C_{FD}$ .

$V_{RST}$  is set as 2.7 V. Furthermore, the gain variation of pixel V1 at different temperatures is also smaller than that of the 4 T pixel V2.

Subsequently, the temperature effects on the capacitor  $C_{FD}$  are discussed. The 4 T pixel V2 is used to illustrate the temperature effect, which consists of several types of capacitances [5], [10] from different transistors, such as metal capacitance, junction capacitance, overlap capacitance, and gate–channel capacitance, as shown in Fig. 3.

$C_M$  represents the parasitic capacitance of the metal wires.  $C_{TX,OV}$ ,  $C_{RST,OV}$ , and  $C_{SF,OV}$  are the overlap capacitances of the TX, RST, and SF transistors, respectively.  $C_{SF,GB}$  is the equivalent gate–source capacitance to the substrate of the SF, which changes with the SF's gain due to the Miller effect, and can be expressed as follows:

$$C_{SF,GB} = C_{SF,GS} \cdot (1 - G_{SF}) = 2/3 \cdot W_{SF} \cdot L_{SF} \cdot C_{ox} \cdot (1 - G_{SF}). \quad (12)$$

As presented in [5],  $C_{TX,OV}$  is related to the channel overlap length  $Xd_{TX}$  and width of the TX transistor  $W_{TX}$ . Similarly,  $C_{RST,OV}$  depends on the channel overlap length  $Xd_{RST}$  and width of the RST transistor  $W_{RST}$ . Thus, we have

$$C_{TX,OV} = Xd_{TX} \cdot W_{TX} \cdot C_{ox}; C_{RST,OV} = Xd_{RST} \cdot W_{RST} \cdot C_{ox}. \quad (13)$$

$C_{SF,OV}$  consists of  $C_{SF,OV,GS}$  and  $C_{SF,OV,GD}$ , which are the gate–source and the gate–drain overlap capacitances of the SF, respectively.  $C_{SF,OV}$  is related to  $G_{SF}$  as follows:

$$C_{SF,OV} = C_{SF,OV,GS} + C_{SF,OV,GD} = Xd_{SF} \cdot W_{SF} \cdot C_{ox} \cdot (2 - G_{SF}). \quad (14)$$

From Fig. 3, the junction capacitances of the floating diffusion (FD) consist of the bottom-plate capacitance  $C_{FD,J}$  and the side-wall capacitance  $C_{FD,JSW}$ .  $C_{FD,J}$  and  $C_{FD,JSW}$  are directly proportional to the diffusion area  $A_{FD}$  and the perimeter of the FD region  $P_{FD}$ . Both capacitances are dependent on the voltage value at the FD node  $V_{PD}$ .

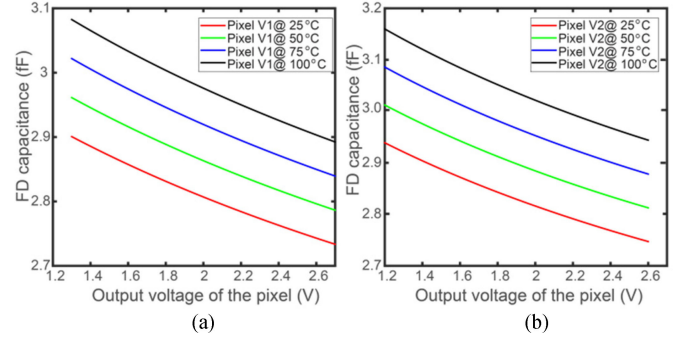


Fig. 4.  $C_{FD}$  versus  $V_{PIX}$  at different temperatures. (a) Pixel V1. (b) Pixel V2.

Thus, the junction capacitances vary with  $V_{PIX}$  and are given by

$$C_{FD,J} = \frac{C_{J0}}{(1 + V_{PD}/\varphi_B)^{M_J}} A_{FD}; C_{FD,JSW} = \frac{C_{JSW0}}{(1 + V_{PD}/\varphi_{BSW})^{M_{JSW}}} P_{FD} \quad (15)$$

where  $C_{J0}$  is the zero-bias junction capacitance per unit area and  $C_{JSW0}$  is the normalized capacitance per unit length;  $\varphi_B$  and  $\varphi_{BSW}$  are the built-in potentials of the bottom and side-walls' junction capacitance, respectively; and  $M_J$  and  $M_{JSW}$  are the junction grading coefficients of the bottom area and side-walls' capacitances, respectively.

$C_{FD}$  consists of linear and nonlinear parts, which vary with  $V_{PIX}$ . More importantly,  $C_{FD}$  has a strong TC due to the temperature dependence on  $G_{SF}$ ,  $\varphi_F$ ,  $V_{th}$ , and other parameters. To simplify the analysis, the linear polynomial functions are used to describe the temperature dependence of each component in  $C_{FD}$ .

In the simplified analytical model, the metal capacitance has a low TC, which could be regarded as independent of the temperature and voltage variations.  $C_{SF,GB}$  has a negative TC  $T_{CCG_{BSF}}$ . The overlap capacitance has a small TC  $T_{CCOV}$ , while the junction capacitances have a larger positive TC, which is around 0.25%/°C. Having the largest capacitance value and TC, the junction capacitance is dominant in the temperature variation of  $C_{FD}$ .

The modeling of  $C_{FD}$  in pixel V1 is similar to that in the 4 T pixel. The modeling results for  $C_{FD}$  of both pixels are shown in Fig. 4, where  $C_{FD}$  decreases with the output voltage of the pixel. The average value of the capacitance is chosen as the modeled value of the  $C_{FD}$  to calculate the final value of the conversion gain (CG). In both pixels,  $C_{FD}$  has a positive TC.

## IV. MEASURED RESULTS

The temperature characteristic of the CIS is included in the model by adding the temperature model of the components in the pixel's model proposed in [5]. Measurement results conducted on the prototype image sensor, fabricated with a 0.18- $\mu\text{m}$  CIS technology, are used to verify the above-mentioned analysis and the updated analytical model.

In the unity-gain configuration, pixel V1 realizes a larger CG than the 4 T pixel, as shown in Fig. 5(a); the lines with star marks represent the modeled results, and the lines with circle marks represent the measured results over the temperature range of 25–100 °C. When the temperature goes up, both pixels have a declined CG, mainly due to the increasing value of  $C_{FD}$  and the decreasing value of the voltage

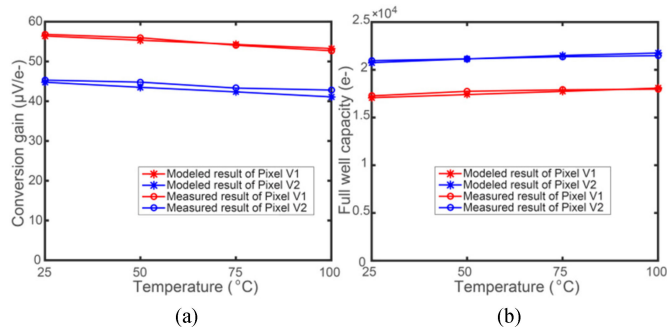


Fig. 5. (a) CG as a function of temperature. (b) FWC as a function of temperature.

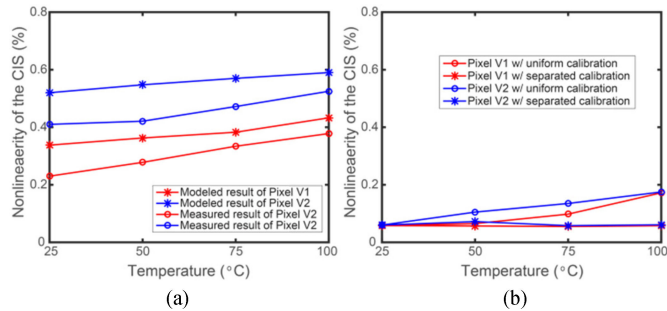


Fig. 6. Nonlinearity of the pixels at different temperatures. (a) Without calibration. (b) With calibration.

buffer's gain. As shown in Fig. 5(a), the measured results of the CG agree well with the modeled results.

In this design, the FD region determines the FWC value of the pixel, which increases with temperature due to the decreasing CG, while the voltage range of the ADC remains the same for all temperatures considered. The modeling results exhibit a good agreement with the measured results, as shown in Fig. 5(b). In [3], the authors also came to the same conclusion, explained from the standpoint of the increasing pinning voltage at a higher temperature.

The measured dark current of pixels V1 and V2 is 58 and 65  $e^-/s$ , respectively, at room temperature and rises exponentially with temperature. The doubling temperature is approximately 7–8  $^{\circ}\text{C}$ , which is similar to the results observed in other publications [11], [12].

When the temperature increases, the nonlinear part of  $C_{FD}$  increases and, thereby, deteriorates the linearity performance of the pixel [5]. In the nonlinearity measurement, the light intensity is fixed, while the exposure time of the CIS increases evenly. As shown in Fig. 6(a), the linearity deteriorates with increasing temperature for both types of pixels. Pixel V1 shows a superior linearity compared with the 4 T pixel V2 for all temperatures. The measured results are obtained for a maximum exposure time of 0.5 ms, wherein the dark current has not destroyed the CIS' linearity performance even at 100  $^{\circ}\text{C}$ .

In [6], a digital calibration method is proposed to reduce the nonlinearity. The digital output of the CIS is used to predistort the ADC's ramp in such a way that the resulting ADC's nonlinearity compensates for the original nonlinear behavior of the CIS. In this article, the effectiveness of the method at different temperatures is validated. First, the transfer curve of the CIS, from the incident photons to the final digital output at 25  $^{\circ}\text{C}$ , is captured. As shown in Fig. 6(b), after calibration, both pixels achieve a nonlinearity of less than 0.06% at 25  $^{\circ}\text{C}$ . The

same calibrated ramp code is employed to calibrate the CIS at other temperatures; this is known as a "uniform calibration." However, when the temperature rises, especially above 75  $^{\circ}\text{C}$ , the improvements are not as effective as the results at room temperature. This is mainly due to the fact that the extracted information of the capacitance–voltage characteristics of the  $C_{FD}$  at 25  $^{\circ}\text{C}$  is different, compared with what would be extracted at a higher temperature. Another group of measurements was carried out, wherein the corresponding transfer curve of the CIS at each specific temperature is used to calibrate the output of the image sensor at that specific temperature. This is called "separated calibration." The measurement results show that with this specific temperature-dependent calibration code, the proposed digital calibration achieves excellent linearity over the whole temperature range.

In a future design, a temperature sensor would be implemented on-chip to realize a fully automatic linearity calibration by choosing the corresponding calibration code according to the measured temperature results.

## V. CONCLUSION

Based on an updated analytical CIS model including temperature-dependence, the pixels' behavior at different temperatures is explored. The measured results of a prototyped CIS agree well with the analysis. Furthermore, a digital linearity calibration method proves the validity of the linearity improvement when the temperature varies.

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