Linearity analysis of a CMOS image sensor

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Abstract
In this paper, we analyze the causes of the nonlinearity of a voltage-mode CMOS image sensor, including a theoretical derivation and a numerical simulation. A prototype chip designed in a 0.18 µm 1-poly 4-metal CMOS process technology is implemented to verify this analysis. The pixel array is 160 × 80 with a pitch of 15 µm, and it contains dozens of groups of pixels that have different design parameters. From the measurement results, we confirmed these factors affecting the linearity and can give guidance for a future design to realize a high linearity CMOS image sensor.

I. Introduction

In the past decades, the use of CMOS and charge coupled device (CCD) image sensors have increased exponentially, due to the growth of electronic devices in applications such as mobile camera phones, security, and surveillance systems. CMOS image sensors (CIS) offer advantages over CCDs, particularly when low power consumption, low cost, and system-on-chip capability are crucial.

Although in most commercial cameras or imaging systems gamma correction is added to code luminance into a perceptually uniform domain, and it will introduce nonlinearity to the image sensor, linearity is still an important parameter for image sensors in many applications. For example, for quantitative imaging, the image sensor must be linear enough to perform image analysis, including shading correction, linear transforms, flat fielding, *etc.*[1].

A high-performance CCD image sensor has an excellent linearity, and its nonlinearity can be as low as a few tenths of a percent. This is much better than its CMOS counterpart, which can achieve a nonlinearity of several percent [2]-[3].

CIS can be divided into voltage mode and current mode, categorized by readout circuit types. In a voltage mode CIS, after the electrons are converted from the charge domain into the voltage domain, they are stored on the floating diffusion region (FD) and are read out through a source follower (SF); in current mode, the readout transistor is biased in the linear region or the velocity saturation region [3] to generate a current instead of a voltage, and the current is proportional to the illumination intensity.

A current mode CIS is suited for high-speed readout and focal-plane processing [4]. However, poorer noise performance and higher nonlinearity have prevented it from being widely used.

This paper focuses on the linearity of the voltage mode CIS and is organized as follows. An overview of the complete imaging system is given in Section II. An analysis and review of the linearity of a standard CIS operating in the voltage mode is presented in Section III. Experimental results of the fabricated image sensor are presented in the following section. Section V gives the conclusion of the overall work.

II. Imaging system overview

CMOS image sensors utilize photodiodes (PD) to convert photons into electrons and then further into an electrical signal. Then the electrical signal is further processed. A functional block diagram of a typical CMOS image sensor system is shown in Figure 1.

The system shown contains five blocks. Photodiodes absorb incident photons and generate a flow of electrons in the pixel. The total capacitance (C_{FD}) of the floating diffusion transforms the electrons to a voltage. A source follower is used to drive the loading circuit. An amplifier provides extra gain and noise reduction, especially under low illumination conditions. The Analog-to-Digital converter (ADC) finally digitalizes the analog output into digital signals to be further processed. The input of the imaging system is an average number of the incident photons (P) with unit exposure time, and the final output is a digital number (DN). Ideally, the transfer function between the incident photon signal and the final digitized output should be linear. However, as each block introduces a nonlinearity, the output signal cannot be simplified as the photon input multiplied by a proportionality constant.

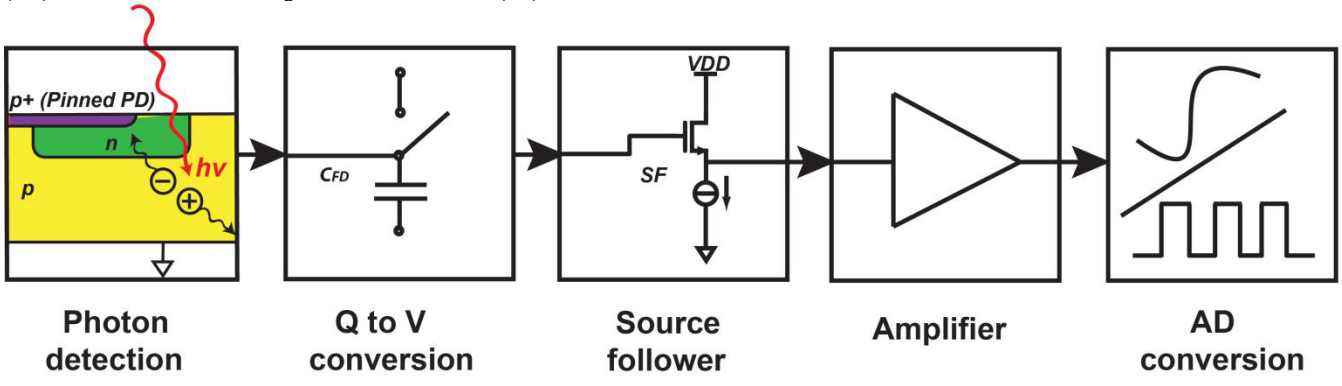

Figure 1 *The diagram of a CMOS image sensor.*

III. Nonlinearity analysis

The photocurrent of a photodiode is extremely linear to the incident light level. The lower limit of the photocurrent linearity is determined by the dark current [5]. Nowadays, pinned photodiodes (PPD) are widely used to bring down the dark current. For this reason, the nonlinearity from the photodiode is usually ignored. In this paper, we assume that the conversion from the photons to electrons by the photodiode is linear.

The ADC and the amplifier can achieve relatively excellent linearity with an elaborate circuit design. The nonlinearity of the pixel is mainly caused by the source follower's variable gain and the nonlinear integration capacitor C_{FD}.

Figure 2 shows the schematic of a typical voltage mode 4T pixel. The pixel circuit consists of a pinned photodiode, a charge transfer switch (M1), a reset switch (M2), a source follower (M3) and a row select switch (M4). The current source transistor (M5) is shared by multiple rows of pixels. V_{DD} is the power supply while V_{PIX} is the output voltage of pixel. V_{LN} provides an adjustable bias current. In the following analysis, the nonlinearity caused by the row select transistor (M4) is omitted to simplify the analysis.

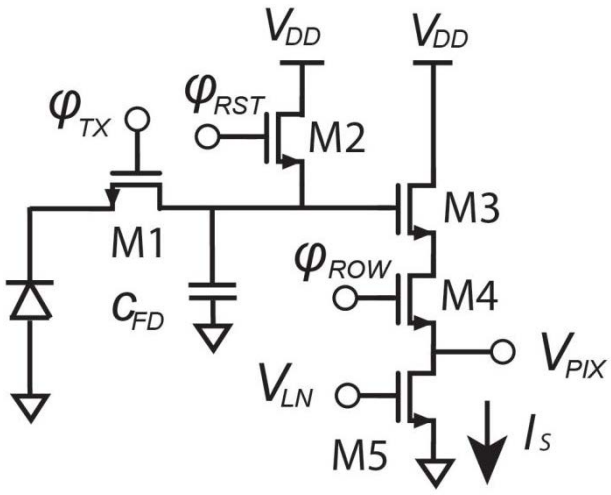

Figure 2 *A schematic of the 4T pixel.*

The SF is used to drive the load circuit and its size is usually designed as small as possible to achieve a higher fill factor. Equation (1) shows the small-signal voltage gain (G_{SF}) of the SF, where $g_{m,SF}$ and $g_{mb,SF}$ are the gate-drain and the bulk-drain transconductances of the SF transistor; the factor χ is the ratio of $g_{m,SF}$ and $g_{mb,SF}$; R_S is the finite output resistance of the current source; γ represents the body effect; φ is the strong inversion surface potential while V_{SB} is the source-to-bulk voltage. The nonlinear gain of the SF degrades the linearity of the image sensor, as it changes with the output voltage of the pixel.

$$G_{SF} = \frac{g_{m,SF} \cdot R_S}{(g_{m,SF} + g_{mb,SF}) \cdot R_S + 1} = \frac{g_{m,SF}}{(g_{m,SF} + \chi \cdot g_{m,SF}) + 1/R_S}$$
$$= \left(1 + \frac{\gamma}{2\cdot\sqrt{\varphi + V_{SB}}} + \frac{1}{g_{m,SF} \cdot R_S}\right)^{-1} = \left(1 + \frac{\gamma}{2\cdot\sqrt{\varphi + V_{PIX}}} + \frac{1}{g_{m,SF} \cdot R_S}\right)^{-1} \quad (1)$$

When the transistor is working in the saturation region, its current is shown in Equation (2). λ is the channel-length modulation parameter; C_{ox} is unit oxide capacitance and μ is the field-effect mobility of the transistor; W and L are the width and length of the transistor; V_{th} is the threshold voltage; V_{GS} and V_{DS} are the gate-to-source and the drain-to-source voltages of the transistor.

$$I = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})^2 (1 + \lambda \cdot V_{DS}) \quad (2)$$

The finite output resistance of the current source changes with the bias current I_S and it can be expressed as [6].

$$R_S \approx \frac{1}{\lambda I_S} \quad (3)$$

From Equation (3), we can derive

$$g_{m,SF} \cdot R_S = \sqrt{2 \cdot \mu \cdot C_{ox} \cdot \left(\frac{W_{SF}}{L_{SF}}\right) \cdot (1 + \lambda \cdot V_{DS})} \cdot \frac{1}{\lambda \cdot \sqrt{I_S}} \quad (4)$$

In Equation (4) ,W_{SF} and L_{SF} are the width and length of the SF. Combining Equations (1) to (4), the gain of the SF is expressed in Equation (5). When the bias current increases, the SF's gain decreases with the output voltage of the pixel.

$$G_{SF} = \frac{1}{1 + \frac{\gamma}{2 \cdot \sqrt{\varphi + V_{PIX}}} + \frac{\lambda \cdot \sqrt{I_S}}{\sqrt{2 \cdot \mu \cdot C_{ox} \cdot \left(\frac{W_{SF}}{L_{SF}}\right) \cdot (1 + \lambda \cdot (V_{DD} - V_{PIX}))}}} \quad (5)$$

V_{FD} is the voltage on the FD, and it is related to the output voltage of the pixel. Based on Equation (2), we can calculate the value of V_{FD} as follows.

$$V_{FD} = V_{PIX} + \sqrt{\frac{2 \cdot I_S}{\mu \cdot C_{ox} \cdot (W_{SF} / L_{SF}) \cdot (1 + \lambda \cdot (V_{DD} - V_{PIX}))}} + V_{th,SF} \quad (6)$$

The threshold voltage of the SF can be expressed as in Equation (7), and V_{th0} is the zero-bias threshold voltage. The signal dependent threshold fluctuations result in variations in the photodiode reset level.

$$V_{th,SF} = V_{th0} + \gamma \cdot (\sqrt{\varphi + V_{PIX}} - \sqrt{\varphi}) \quad (7)$$

The total capacitance of the FD diffusion determines many important performance parameters of the pixel, such as full-well capacity, conversion gain, and readout noise. It also affects the linearity of the image sensor. C_{FD} consists of several different types of capacitances. A cross-sectional view of the C_{FD} is shown in Figure 3. The capacitances can be categorized into metal

capacitance, p-n junction capacitance and gate capacitance [7]-[8]. Table 1 gives a detailed summary of C_{FD}.

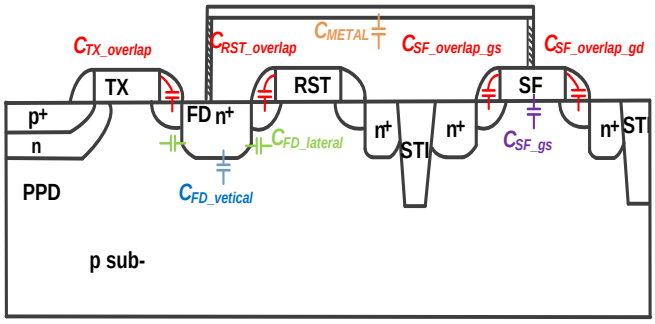

Figure 3 *A cross-sectional view of* C_{FD}.

C_{METAL} represents the parasitic capacitance of the metal wires. *It* does not vary with the output voltage and is therefore regarded as a constant.

$C_{TX\_overlap}$, $C_{RST\_overlap}$ and $C_{SF\_overlap}$ are the overlap capacitances of the TX, the RST and the SF transistors, respectively, while Xd_{TX}, Xd_{RST}, Xd_{SF} and W_{TX}, W_{RST}, W_{SF} are the channel overlap lengths and widths of these transistors, correspondingly. C_{SF_gs} is the equivalent gate-source capacitance to substrate of the source follower transistor. $C_{SF\_overlap}$ consists of $C_{SF\_overlap\_gs}$ and $C_{SF\_overlap\_gd}$, which are the gate-to-source and the gate-to-drain overlap capacitances. C_{SF_gs} and $C_{SF\_overlap}$ change with the SF's gain due to the Miller effect.

Junction capacitances of the FD include the bottom plate capacitor $C_{FD\_vetical}$ and the side wall capacitor $C_{FD\_lateral}$. The bottom plate junction capacitance $C_{FD\_vetical}$ is directly proportional to the diffusion area A_{FD} and inversely proportional to the width of the vertical depletion region $W_{vertical}$.

$$C_{FD\_vertical} = \varepsilon_0 \cdot \varepsilon_r \cdot A_{FD} / W_{vertical} \tag{8}$$

In Equation (8), ε_r is the relative permittivity of the silicon while ε_0 is the permittivity of free space. $W_{vertical}$ can be calculated by Equation (9).

$$W_{vertical} = \left[\frac{2 \cdot \varepsilon_0 \cdot \varepsilon_r \cdot (\varphi_B + q \cdot V_{FD})}{q^2} \cdot \left(\frac{N_A + N_D}{N_A \cdot N_D} \right) \right]^{MJ} \tag{9}$$

In Equation (9), φ_B is the built-in potential of the bottom and *MJ* is junction grading coefficients of the bottom area. q is the electronic charge. The width of the depletion region depends on N_A and N_D, which are the doping concentrations of the p- and n- type materials, respectively.

Similarly, the sidewall junction capacitance $C_{FD\_lateral}$ is proportional to the perimeter of the FD regions P_{FD} and inversely proportional to the width of the depletion region $W_{lateral}$.

$$C_{FD\_lateral} = \varepsilon_0 \cdot \varepsilon_r \cdot P_{FD} / W_{lateral} \tag{10}$$

$W_{lateral}$ is shown in Equation (11). φ_{BSW} is the built-in potential of the sidewalls, and *MJSW* is the junction grading coefficients of the side-walls.

$$W_{lateral} = \left[\frac{2 \cdot \varepsilon_0 \cdot \varepsilon_r \cdot (\varphi_{BSW} + q \cdot V_{FD})}{q^2} \cdot \left(\frac{N_A + N_D}{N_A \cdot N_D} \right) \right]^{MJSW} \tag{11}$$

Table 1 A summary of the components of C_{FD}

Components of C_{FD}	Equation
Metal capacitance	C_{METAL}
Gate capacitance	$C_{TX\_overlap} = Xd_{TX} \cdot W_{TX} \cdot C_{ox}$
	$C_{RST\_overlap} = Xd_{RST} \cdot W_{RST} \cdot C_{ox}$
	$C_{SF\_overlap} = C_{SF\_overlap\_gs} + C_{SF\_overlap\_gd}$ $= W_{SF} \cdot Xd_{SF} \cdot C_{ox} \cdot (1 - G_{SF})$ $+W_{SF} \cdot Xd_{SF} \cdot C_{ox}$ $= W_{SF} \cdot Xd_{SF} \cdot C_{ox} \cdot (2 - G_{SF})$
	$C_{SF\_gs} = 2/3 \cdot W_{SF} \cdot L_{SF} \cdot C_{ox} \cdot (1 - G_{SF})$
p-n junction capacitance	$C_{FD\_vertical} = \varepsilon_0 \cdot \varepsilon_r \cdot A_{FD} / W_{vertical}$
	$C_{FD\_lateral} = \varepsilon_0 \cdot \varepsilon_r \cdot P_{FD} / W_{lateral}$

Based on the summary given in Table 1, the total capacitance on FD is given as follows:

$$C_{FD} = C_{RST\_overlap} + C_{TX\_overlap} + C_{SF\_gs} + C_{SF\_overlap} + C_{FD\_vertical} + C_{FD\_lateral} + C_{METAL} \tag{12}$$

Q is the integrated charge within a certain exposure time t, and it is related to the area of the photodiode A_{PPD}. QE is the quantum efficiency.

$$Q(t) = P \cdot QE \cdot q \cdot t \cdot A_{PPD} \tag{13}$$

The output voltage of the pixel is related to $Q(t)$ and varies with the integration time t.

The gain of SF can be rewritten as

$$G_{SF}(t) = \frac{1}{1 + \frac{\gamma}{2\sqrt{\varphi + V_{PIX}(t)}} + \frac{\lambda \cdot \sqrt{I_S}}{\sqrt{2 \cdot \mu \cdot C_{ox} \cdot \left(\frac{W_{SF}}{L_{SF}}\right) \cdot (1 + \lambda \cdot (V_{DD} - V_{PIX}(t)))}}} \tag{14}$$

We can derive the output voltage of the pixel from Equation (15), where V_{RST} is the initial value of a pixel output after the FD is reset.

$$V_{PIX}(t) = V_{RST} - Q(t) \cdot G_{SF}(t) / C_{FD}(t) \tag{15}$$

The amplifier, shown in Figure 1, provides programmable gain for the image sensor. After the function of analog correlated double sampling (CDS) is realized, the input signal of the ADC can be expressed as

$$V_{CDS}(t) = G_{PGA} \cdot G_{SF}(t) \cdot Q(t) / C_{FD}(t) \tag{16}$$

In Equation (16), G_{PGA} is the gain of the amplifier.

Finally, the ADC is employed to convert the analog signal into a digital number, *DN*. A linear amplifier and a high-resolution ADC with excellent static performance are needed to guarantee the linearity of the whole sensor system. G_{ADC} is the conversion gain of ADC.

$$DN(t) = G_{ADC} \cdot G_{PGA} \cdot G_{SF}(t) \cdot Q(t) / C_{FD}(t) \tag{17}$$

Based on the theoretical derivation from photons to final digital numbers in the image sensor, we propose an algorithm to calculate the C_{FD}, G_{SF} and hence the linearity of the CMOS image sensor, as shown in Figure 4.

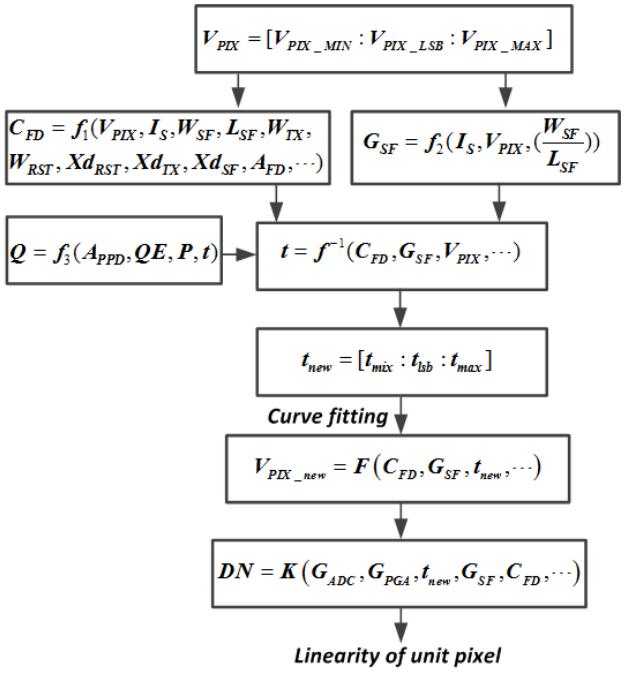

Figure 4 *A linearity modelling of unit pixel.*

In this algorithm, we will consider the nonlinearity caused by the SF and the C_{FD} as well as the mismatch in the image sensor. The nonlinearity incurred during the conversion from photons to electrons is not taken into consideration. Firstly, the algorithm to calculate the linearity of a unit pixel is introduced.

V_{PIX} is set to increase linearly within a reasonable range with each step of V_{PIX_LSB}. After that, we calculate the corresponding values of C_{FD} and G_{SF} for incremental V_{PIX} values. Combined with the integrated charge *Q*, we deduce the corresponding value of the exposure time under the incremental V_{PIX} values through the inverse function. Then, through the curve fitting, we obtain the V_{PIX_new} that contains the nonlinearity from G_{SF} and C_{FD}, while the exposure time is evenly increasing with a step of t_{lsb}. After the CDS and the digitalization of the image sensor outputs, the transfer function between the incident photon signal and *DN* is obtained.

The pixel array has *i* rows and *j* columns. According to the technology file, we add the mismatch model of transistors in the pixel as well as that of the bias current, based on the current source size. The noises of the circuit as well as the mismatches of the amplifier and ADC are also added in the algorithm. Then, we calculate the output *DN* of each individual pixel. After averaging *DN* of the whole pixel array, the linearity of the image sensor can be calculated according to the EMAV1288 measurement standard.

VI. Model verification

A chip with a 1-poly 4-metal CMOS process technology [9] is used to verify the algorithm we proposed above. The structure of the chip is shown in Figure 5. The image sensor has a pixel array of 80 (rows) × 160 (columns). The pixels are divided into dozens of groups. The variable design parameters include transfer gate width (W_{TX}) and length (L_{TX}), floating diffusion node width (W_{FD}) and length (L_{FD}), and SF's width (W_{SF}) and length (L_{SF}). The column amplifier provides a programmable gain by changing the ratio of the input and the feedback capacitors. The sample and hold circuit is utilized as a CDS circuit to bring down the noise. The output is then buffered and digitalized by a high-resolution on-board ADC. The ADC's excellent static performance guarantees it does not restrict the linearity performance of the image sensor.

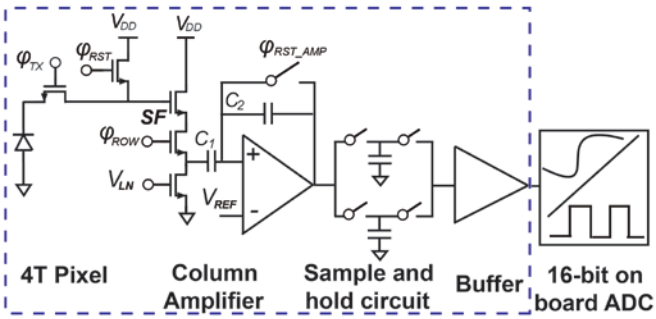

Figure 5 *The schematic of the test image sensor.*

The size of the chip is 4.62 mm × 3.15 mm. The micrograph of the chip is shown in Figure 6.

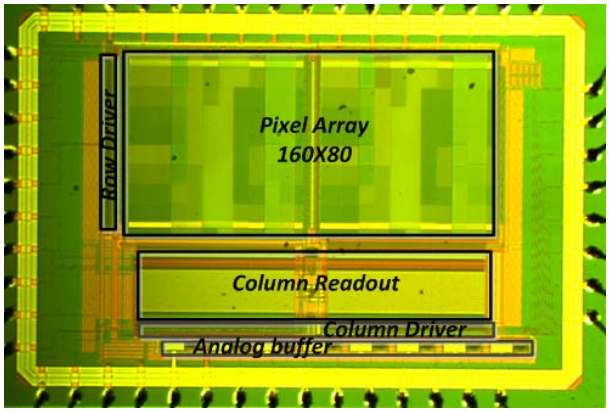

Figure 6 *The micrograph of the test image sensor.*

Two groups of the pixels are chosen to compare the nonlinearity of the image sensor, based on various design parameters shown in Table 2. Groups A and B have different PPD sizes while each pixel in the same group uses the same PPD size.

Table 2 The design parameters of all the pixels

Group	Pixel	TX(W_{TX}/L_{TX}) (μm/ μm)	FD(W_{FD}/L_{FD}) (μm/ μm)	SF(W_{SF}/L_{SF}) (μm/ μm)
Group A	Pixel1	6/0.6	5.7/1.3	0.6/1
	Pixel2	6/0.6	5.7/1.3	0.7/1
	Pixel3	6/0.6	5.7/1.3	0.8/1
	Pixel4	6/0.6	5.7/1.3	0.9/1
Group B	Pixel1	2/0.6	1.7/1.3	0.9/0.5
	Pixel2	4/0.6	3.7/1.3	0.9/0.5
	Pixel3	8/0.6	7.7/1.3	0.9/0.5
	Pixel4	10/0.6	9.7/1.3	0.9/0.5
	Pixel5	12/0.6	11.7/1.3	0.9/0.5

Based on the algorithm, the modelling results of the *C-V* characteristic of the C_{FD} for the pixels of Group B are plotted in Figure 7 (a). The width of the FD increases from 1.7 μm to 11.7 μm. The wider the FD, the larger the capacitance of the FD is. The FD capacitances decrease with the output voltage of the pixel. These variations are consistent with Equation (8) and (10). The average values of the capacitor are chosen as the modelled value of the C_{FD}. Nine types of pixels of Group A and B are chosen to compare the test results with the modelling results. Figure 7 (b) shows that the photoelectric conversion characteristic of the measurement results agrees with that of the modelling results in the image sensor.

According to the analysis mentioned above, a conclusion can be made that the threshold voltage and the gain of the source follower nonlinearly vary with the output voltage of the pixel. A column of pixels without photodiodes are used to test the linearity performance of the SF independently. The width of the SF is 0.9 μm while the length is 0.5 μm. Figure 7 (c) shows that V_{GS} of the SF increases with the output voltage, due to body effect. Figure 7 (d) plots the relationship between G_{SF} and the output voltage of the pixel. In Figure 7, the solid lines stand for the simulation results while the lines with asterisk markers represent the test results. The chip is tested with several different bias currents of the pixel ranging from 1 μA to 3 μA. A larger bias current leads to a smaller G_{SF}. These conclusions validate Equation (5) and (6).

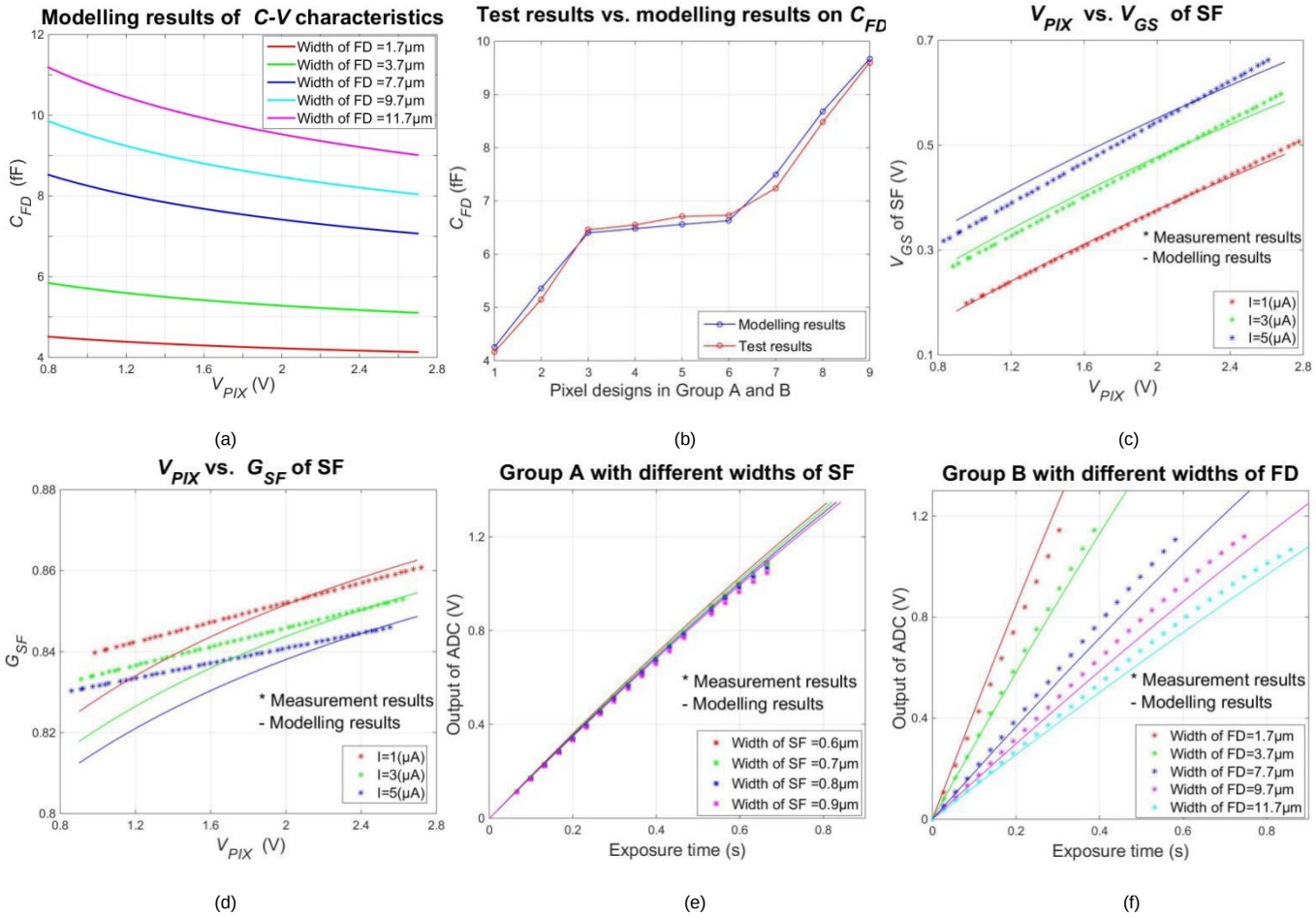

Figure 7 *(a) C-V characteristic of C_{FD}; (b) Test vs. modelling results of C_{FD}; (c) V_{PIX} vs. V_{GS}; (d) V_{PIX} vs. G_{SF}; (e) Signal output vs. exposure time for the pixels in Group A; (f) Signal output vs. exposure time for the pixels in Group B.*

The calculation of the nonlinearity begins with the plot of the signal level versus the exposure time. The signal level is typically specified in *DN*. We converted the *DN* into an analog voltage in order to have a clearer view of the output swing plotted in Figure 7 (e) and (f). In Group A, the width of the SF increases from 0.6 µm to 0.9 µm. The capacitance of the FD slightly increases. Meantime, the slope of the signal output versus time slightly decreases. Figure 7 (f) shows that while the width of FD is changing from 1.7 µm to 11.7 µm in Group B, the junction capacitance of the FD is increasing, leading to a decreasing conversion gain.

The nonlinearity value is usually expressed in percentage, based on the deviation between the obtained data points and the calculated best-fit line. Figure 8 concludes the nonlinearity and noise performances for the different pixels in Group A, while Figure 9 shows the pixels' nonlinearity results in Group B. In Figure 8 and 9, the blue lines with circle markers represent the modelling results while the red ones give the test results of nonlinearity for the image sensor. The pink line with star markers illustrates the noise performance of the pixels in Group A. The modelling and the test results share the same trend on the nonlinearity for various pixel designs. Theoretically, when the sizes of the SF and the FD increase, the fact that the nonlinear capacitance increases will bring down the linearity performance of the whole image sensor. We can improve the linearity of the pixel by choosing suitable design parameters, such as a smaller size of the FD or the SF, based on the measurements results.

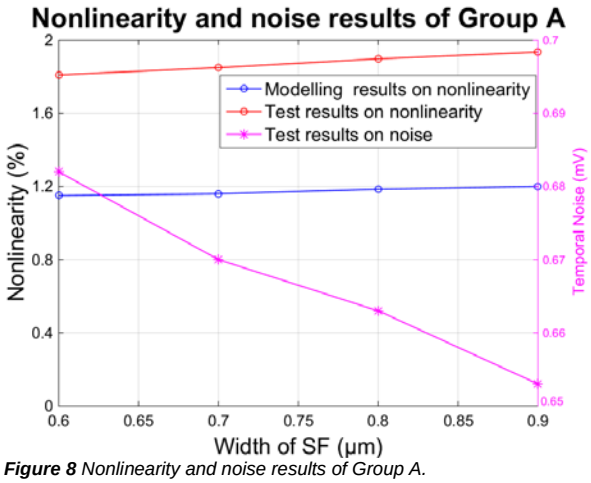

Figure 8 *Nonlinearity and noise results of Group A.*

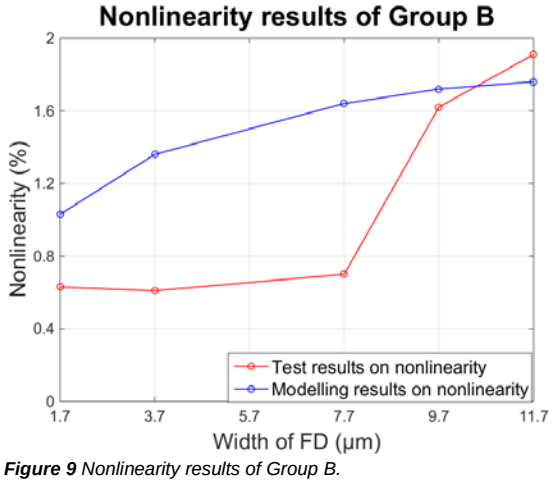

Figure 9 *Nonlinearity results of Group B.*

In addition, from Figure 8, we find a smaller size of the SF can lead to a larger noise. Hui Tian showed the evidence that the nonlinearity of an image sensor actually improves SNR at high illumination in [10]. Besides, Jun Lin analyzed the relationship between the nonlinearity and modulation transfer function (MTF) in [11]. Tradeoffs exist among the performances of noise, nonlinearity, and MTF for image sensors. The above-mentioned procedures can serve as a guideline for future pixel designs.

V. Conclusion

In this paper, we proposed a method to analyze the floating diffusion capacitance $C_{FD,}$ G_{SF} and the linearity of the voltage mode CIS. The modelling results of the linearity, G_{SF} and C_{FD} are in agreement with the measurement results, validating the effectiveness of the modelling algorithm.

Acknowledgement

The authors would like to thank TowerJazz for their support in realizing the test devices. The project is part of the E450EDL project, sponsored by the EC.

References

[1] W. Cao, et. al, "1024 x 1024 HgCdTe CMOS Camera for Infrared Imaging Magnetograph of Big Bear Solar Observatory", Proc. SPIE, Vol. 5881, pp. 245, 2005.

[2] http://www.photometrics.com/resources/learningzone/linearity.php (retrieved 2016-02-05).

[3] Z. Yang, "Low Fixed Pattern Noise Current-mode Imager Using Velocity Saturated Readout Transistors", in ISCAS 2007, ISCAS, pp. 2842-284, 2007.

[4] J. Nakamura, et. al, "On-Focal-Plane Signal Processing For Current-Mode Active Pixel Sensors", IEEE Transactions on Electron Devices, vol. 44, no. 10, pp. 1747-1758, Oct. 1997.

[5] B. Tabbert, "Linearity of the photocurrent response with light intensity for silicon PIN photodiode array", Proc. SPIE, Vol. 647111, pp. 647, 2007.

[6] B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill International Edition, pp. 55-56, 2001.

[7] S. U. Ay, "Photodiode peripheral utilization effect on CMOS APS pixel performance", IEEE Trans Circuits Systems I, pp. 1405-1411, 2008.

[8] F. Kusuhara, "Analysis and Reduction Technologies of Floating Diffusion Capacitance in CMOS Image Sensor for Photon-Countable Sensitivity", ITE Transactions on Media Technology and Applications, pp. 91-98, 2016.

[9] Y. Xu, et. al, "A Potential-Based Characterization of the Transfer Gate in CMOS Image Sensors", IEEE Transactions on Electron Devices, Vol. 63, pp. 42-48, 2016.

[10] T. Hui, et. al, "Analysis of temporal noise in CMOS photodiode active pixel sensor", IEEE J Solid-State Circuits, 36(1), pp. 92, 2001.

[11] J. L. Li, et. al, "Study of V/Q Non-Linearity in Scientific CMOS Sensor", in International Journal of Grid and Distributed Computing, Vol. 9, pp.289-298, 2016.

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