Investigating Transfer Gate Potential Barrier by Feed-Forward Effect Measurement

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***Abstract*— In a 4T pixel, the transfer gate (TG) "OFF" surface potential is one of the important parameters, which determines the pinned photodiode (PPD) full well capacity. The feed-forward effect measurement is a powerful tool to characterize the relationship of the PPD injection potential and the feed-forward electrons. In this paper, a parameter V_b is introduced to characterize the TG "OFF" surface potential and V_b can be extracted from the feed-forward measurement result. Using this characterization method, the pixel design and application parameters will be investigated. To better understand and control the full well capacity of the PPD, these effects and parameters will be investigated in this paper. Two test chips, using different technologies, were implemented. Further, the different mechanisms of the feed-forward effect will be discussed.**

I. Introduction

In a CMOS image sensor (CIS) pixel design, the full well capacity of the chip is one of the most important parameters, which determines the dynamic range of the sensor. With the pixel size shrinking, achieving sufficient full well capacity (FWC) is becoming a challenge especially in the high dynamic application.

The full well capacity of the image sensor can have a few different definitions. The most common definition is the maximum signal obtained from the sensor. Tracking from the signal path there are a few limitations that will determine the final output signal swing. Without the limitation of the analog circuit, the capacity ability of the PPD-TG structure will determine the full well capacity of the image sensor. Fig. 1 shows the cross-section schematic of a simple 4T pixel and the potential diagram of the pinned photodiode-transfer gate-floating diffusion (PPD-TG-FD) structure when the FD is reset to a high voltage and TG is "OFF". In this situation, except for the capacitance of the PPD and the pinning voltage (V_{pin}), the TG "OFF" potential barrier height will limite the maximum FWC of the pixel. In this paper, the TG "OFF" potential barrier is characterized based on the feed-forward measurement. The feed-forward measurement not only can measure the feed-forward voltage, which is mentioned in previous study [1], but it also can be use to extract the TG "OFF" potential barrier.

II. Measurment

Two similar test chips were implemented in two distinct technologies, and both of them are commercial 0.18 µm CIS processes. Process A and process B represent these two processes. As shown in Fig. 2, the feed-forward measurement has a special timing diagram based on the normal 4T pixel schematic. Compared with normal 4T operation, the VDD_RST is changed from a DC value to a pulse. Both the high voltage (VDD_RST_H) and low voltage level (V_{inj}) can be adjusted externally. According to the pulse of VDD_RST, the measurement can be divided into two phases: injection phase and readout phase. In the injection phase, the V_{inj} is connected to the drain of reset transistor, the RST and TG are turned "ON" to make sure the electrons are injected into PPD and FD region, and the electrons potential is forced to the V_{inj}. After the injection, TG is "OFF" to keep the injected electrons in PPD. The readout phase is like an imaging readout where VDD_RST is changed to a relatively high voltage (VDD_RST_H). The reset transistor is switched "ON" again to reset the FD node. The measurement will be repeated multiple times while varying the injection voltage (V_{inj}) from 0V to about 2.5V.

With an increasing injection voltage, the TG "OFF" potential barrier can be characterized by introducing a new parameter V_b. As Fig. 3 shows how V_b is defined as the potential difference between the surface potential of the

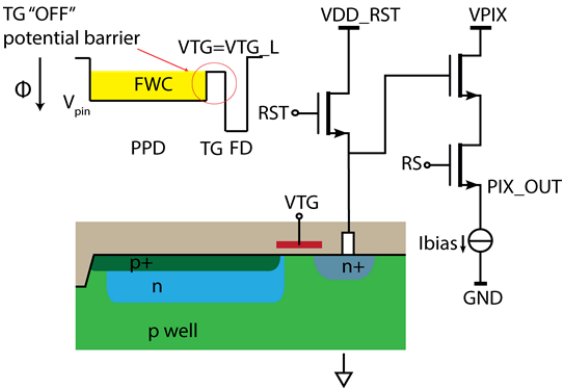

Fig. 1. Schematic of the pixel and simplified PPD-TG-FD structure potential diagram (TG is "OFF", FD is reset).

barrier beneath the transfer gate (when TG is "OFF") and the PPD charge potential in equilibrium state (V_{inj}=0V). If V_b is negative, it means that the potential barrier is higher than the PPD injected electron potential (V_{inj}=0). Correspondingly, a positive V_b means the TG "OFF" potential barrier is lower than the PPD injected electron potential (V_{inj}=0). A larger V_b shows a lower TG "OFF" potential barrier. For the same pinning voltage, a larger V_b also means less FWC in the PPD. If $V_{inj}<V_b$, the TG barrier cannot hold all the electrons, some electrons will overflow to the FD node and then are emptied by the reset pulse. If $V_{inj}=V_b$, the amount of electrons stored in the PPD is maximum. After a holding time (t_{hold}), the electrons jumped to the FD node during this holding time will be counted. The amount of the feed-forward electrons also achieves a maximum. From the analysis above, the first knee-point of the curve (Fig.3) can be extracted as V_b. Process A has a lower potential barrier than process B, $V_{b\_ProcessA}>0V$ and $V_{b\_ProcessB}<0V$. These two different technologies have different process parameters such as the under-gate doping concentration and/or the gate oxide thickness, resulting in two measurements exhibiting a different V_b. The reported results about the feed-forward effect [1] have a similar situation like process B, which has a negative V_b. However, the reported research in [1] did not measure and analyze this knee-point. To allow an easier measurement and analysis of V_b the measurements in this paper will be based on the Process A.

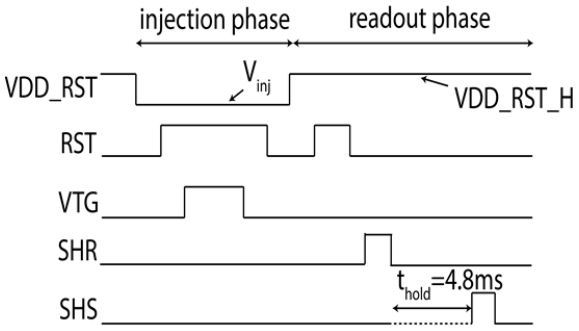

Fig. 2. Timing diagram of the feed forward measurement

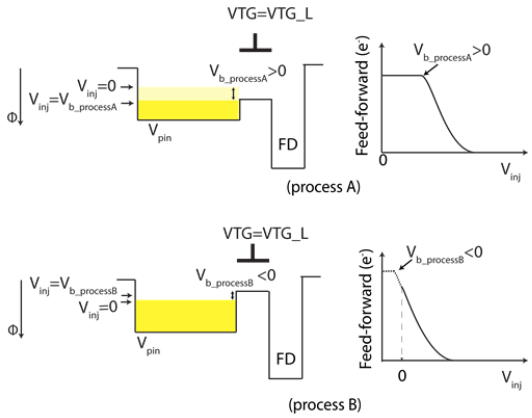

Fig. 3. Potential diagram analysis for Process A and B.

III. Transfer Gate "OFF" Potential Barrier Dependency

Based on the analysis above, the defined parameter V_b can be extracted from feed-forward measurement, which can be used to characterize the TG "OFF" potential barrier. Due to the feed-forward electrons are much less than the normal readout signal, even for a small FD node pixel design, the TG "OFF" potential barrier still can be measured by this characterization method. Except for the technology and TG "OFF" voltage, V_b will also be influenced by other parameters. TG length (TGL), the FD node reset voltage (VDD_RST_H), and TG width (TGW) are three important parameters which can influence V_b. When the FD is reset, TG is "OFF", the junctions of the PPD-TG and FD-TG are reversed biased. The space charge regions of these two junctions will extend into the channel region.

In reality since the space charge area of the PPD-TG and FD-TG will extend into the channel region, the effective channel length will be smaller than the designed one. For a long transfer gate situation, the junction extension effect does not have much influence. However, for a short transfer gate design, the gate control over the channel potential can decreased. In extreme situations, this extension could make the gate controllable channel length to disappear, which results in a punch-through underneath transfer gate. On one hand, for the same FD reset voltage, decreasing TGL can also reduce the potential barrier height. On the other hand, the value of VDD_RST_H will influence the gate controllable channel length, threshold voltage, and potential barrier of the TG. These are the so-called short channel and DIBL (Drain-Induced Barrier Lowering) effect. Fig. 4 and Fig. 5 are the potential diagrams to show the short channel effect and DIBL effect. The measurement results also prove these effects. Fig. 6 presents the feed-forward measurement results for different transfer TGLs. With the TGL increasing from 0.52µm to 1µm, the increase of the potential barrier is 0.6V. Measurement result in Fig. 7 also proved the influence of the FD reset voltage. It shows that when VDD_RST_H is reduced from 3.3V to 2.3V, the increase

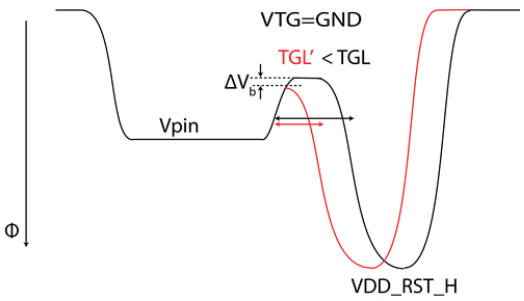

Fig. 4. Potential barrier influenced by the transfer gate length.

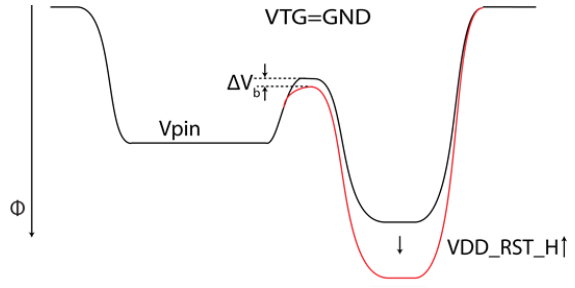

Fig. 5. DIBL effect potential diagram.

of the potential barrier is 0.2V.

Except these two effects, the narrow channel effect also influences V_b. Fig. 8 shows the cross-section of the transfer gate structure widthwise. If a gate voltage is applied, a depletion region is created under the gate area. But, the actual depletion region in the channel is always larger than what is usually assumed for a one-dimensional analysis, due to the existence of the fringing field [2]. Considering the extra charge (ΔQ_{SD}) introduced in the p-well-channel diffusion region (Fig. 8), with the transfer gate width (TGW) being decreased, ΔQ_{SD} cannot be neglected anymore. Therefore, the TG "OFF" potential barrier will be increased. Fig. 9 reveals that V_b is increased from about 0.6V to 1V when the TGW increases from 4

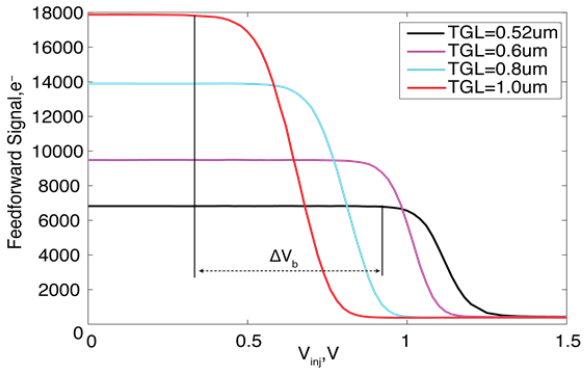

Fig. 6. Potential barrier height improved by an increased transfer gate length.

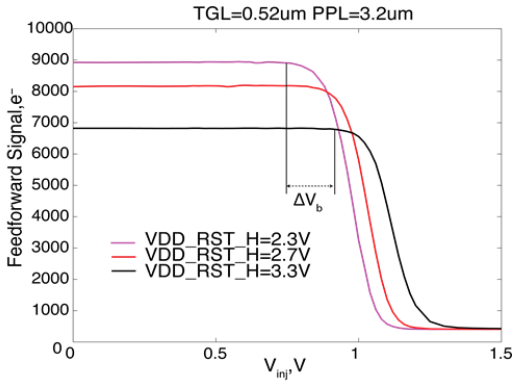

Fig. 7. Feed-forward voltage measurements for the DIBL effect for different reset voltages.

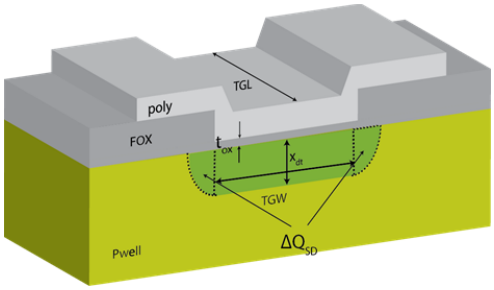

Fig. 8. Cross-section of the transfer gate in the width direction.

μm to 10 μm, which is consistent with the conductive analysis above. However, due to the wider TGW, making the interface between PPD and FD larger, electrons will have a higher possibility to feed-forward into the FD node. But this potential barrier increase for the narrow TG pixel will not increase the FWC of the PPD. From the pinning voltage measurement result shown in Fig. 10 and FWC extraction [3], it can be found although the potential barrier is increased with a TG width reduction, but also the pinning voltage is changed with TG width. Thus, the FWC is not increased by a decreased TG width.

IV. Feed-forward Effect

After the characterization of V_b, the electron feed-forward effect mechanisms will be analyzed. Fig. 11

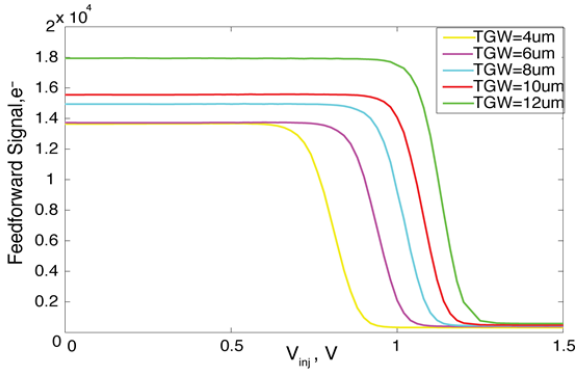

Fig. 9. Potential barrier height differences for the different transfer gate widths.

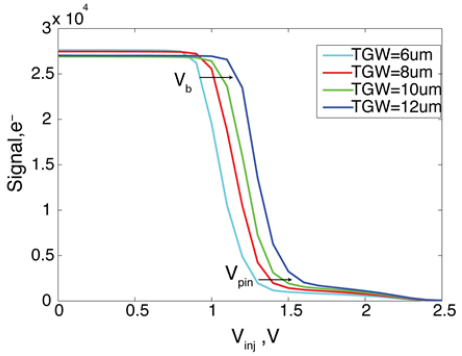

Fig. 10. Pinning voltage measurement for different transfer gate widths.

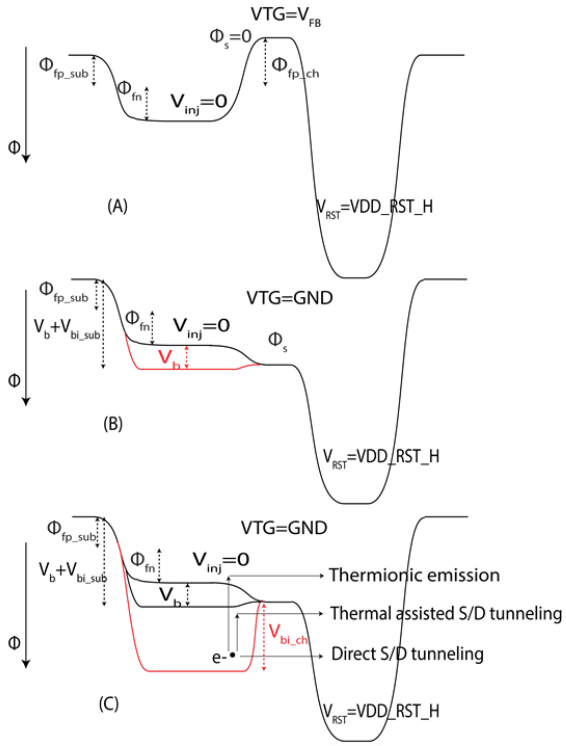

Fig. 11. Potential diagram to explain feed-forward measurement.

depicts the potential diagram of the PPD-TG-FD structure, which will explain the whole process of the feed-forward effect. Plot (A) and (B) describe the TG flat-band voltage (V_{FB}) and the zero voltage applied on the transfer gate situation respectively. In plot (C), the injection voltage already is lower than the surface potential of transfer gate ($V_{inj}>V_b$). There are three distinct mechanisms [4] to be considered here for the feed-forward effect.

The first mechanism is the thermionic emission. Carriers are thermally excited in the PPD, and then jump over the TG potential barrier. This effect will depend on the total number of electrons being held, temperature, and the electron potential. On one hand, both increasing the potential barrier distance (V_{inj}-V_b) and decreasing temperature will decrease the possibility of electron emission. On the other hand, because the photodiode well depth (V_{pin}) is limited, with an injection voltage increase, the thermionic emission of electrons will disappear.

Secondly, with thermally assisted S/D tunnelling, carriers are thermally excited and then tunnelling slightly beneath the top of the potential barrier. Both thermionic emission and thermally assisted S/D tunnelling as their names implied, have a strong temperature dependence.

The third effect is direct S/D tunneling. It can be understood as the PPD-TG junction forward bias current or the sub-threshold current. After a long holding time, all feed-forward electrons have arrived in the FD, and the potential of the PPD will decrease to $V_{inj}=V_b+V_{bi\_ch}$. V_{bi_ch} is the built-in potential of the PPD-TG junction. When the PPD-TG junction is no longer forward biased, the forward bias current and sub-threshold current components will disappear. The forward bias current of this junction before equilibrium can be simply written as:

$$I = I_s \exp\left(\frac{q(V_{bi\_ch}-(V_{inj}-V_b))}{nkT}-1\right) \qquad (1)$$

in which n is the ideality factor, V_{bi_ch} is the build-in potential of the n-doping- channel junction. If V_{bi_ch}-(V_{inj}-V_b) is large, then n≈1; if V_{bi_ch}-(V_{inj}-V_b) is small, then n≈2. I_S is the reverse saturation current of this pn- junction. From the Eq. (1), it can be found that the leakage current decreases with a decrease in V_{inj}. Except for the diffusion current, the sub-threshold current is also the most important component of the leakage current in this situation. The subthreshold current can be expressed as [5]:

$$I_{d,sub} = I_0 \frac{TGW}{TGL}\exp((\kappa VTG\_L - V_b)\frac{q}{kT}) \qquad (2)$$

in which I_o is a proportional constant of the subthreshold current, κ is the gate coupling coefficient of about 0.7, and VTG_L is the transfer gate "OFF" voltage.

V. Conclusion

In this paper, using the feed-forward measurement, the transfer gate "OFF" potential barrier characterization method is proposed; two 4T pixel test chips were implemented. To better understand and control the transfer gate and FWC, the dependency of the potential barrier is investigated: not only the technology and the TG low voltage affect the potential barrier, but also the TG length, the FD node reset voltage, and the TG width have a big influence on the TG "OFF" potential barrier. In this paper, the mechanism of the feed forward effect is further analyzed. These studies are important to understand and model the PPD-TG-FD structure, which is important to come to an optimized pixel design.

Reference

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