Feed-forward voltage in CMOS pinned photodiodes

Mukul Sarkar*, Bernhard Büttgen† and Albert J.P. Theuwissen‡
*Indian Institute of Technology Delhi,
†Mesa Imaging, ‡University of Technology Delft/Harvest Imaging
Tel: +91(11) 2659-1072, Fax: +91(11) 2658-1606, Email: msarkar@ee.iitd.ac.in

***Abstract*—CMOS image sensors have become very popular in low cost imaging devices. In order to realize images of high quality, the image sensors need to have a high resolution, be able to achieve a high Signal-to-Noise ratio (SNR) and have a wide dynamic range. To increase the spatial resolution of the image sensors, the pixel size has been scaling down allowing integration of more pixels in a given die area. On the side, this scaling process reduces the potential barrier separating the charge generation centers from collection centers in modern CMOS photodiodes. This reduces the charge handling capacity of the photodiode well as well. Electrons contained within a well possess thermal energy, and thus acquire random thermal velocities. A sufficient barrier is thus needed to prevent the overflow of electrons when the photodiode potential well is full. In classical CCDs it was found that the minimum barrier needed to hold the electrons in the photodiode well is around 0.4V-0.6V. However the charge handling capacity of the CMOS pinned photodiodes are not well studied. In this paper, the minimum barrier potential needed in a pinned photodiode and the feed-forward of electrons are presented for dependencies on variations in photodiode geometry, temperature and bias voltages.**

I. Introduction

CMOS image sensors have made tremendous advances in the recent years and are being used in almost all field of electronic imaging. The quality of the images obtained from the CMOS image sensors depends mainly on the pixel resolution, signal-to-noise ratio (SNR) and dynamic range. These specifications of the image sensor are directly related to the full well capacity of the photodiodes used in the pixel. In normal operation of a pinned photodiode (PPD) of a standard 4-Transistor pixel as shown in figure 1, after the integration of charges in the photodiode well, the transfer gate is opened allowing the accumulated charges to flow into the floating diffusion node (FD) and being read out. The pixel also includes a transistor (S_{RST}) for resetting the FD to a predetermined voltage level (V_{RST}) prior to the charge transfer. The other two transistors are the source follower and row select transistor (S_{RS}). The row select transistor loads the column bus with the pixel output voltage for readout.

The full well capacity of the PPD region is determined by the number of electrons that the photodiode potential well can store. The potential barrier generated by the transfer gate's channel potential, prevents the overflow of the collected electrons. Ideally when the transfer gate is closed (acting as a barrier) no electrons from the photodiode potential well will flow to the FD node. However from literature it is known that even when the transfer gate (TG) is closed, some electrons will overflow (across the potential barrier), and reach the FD node. This overflow of electrons causes a feed-forward voltage on the FD node [1].

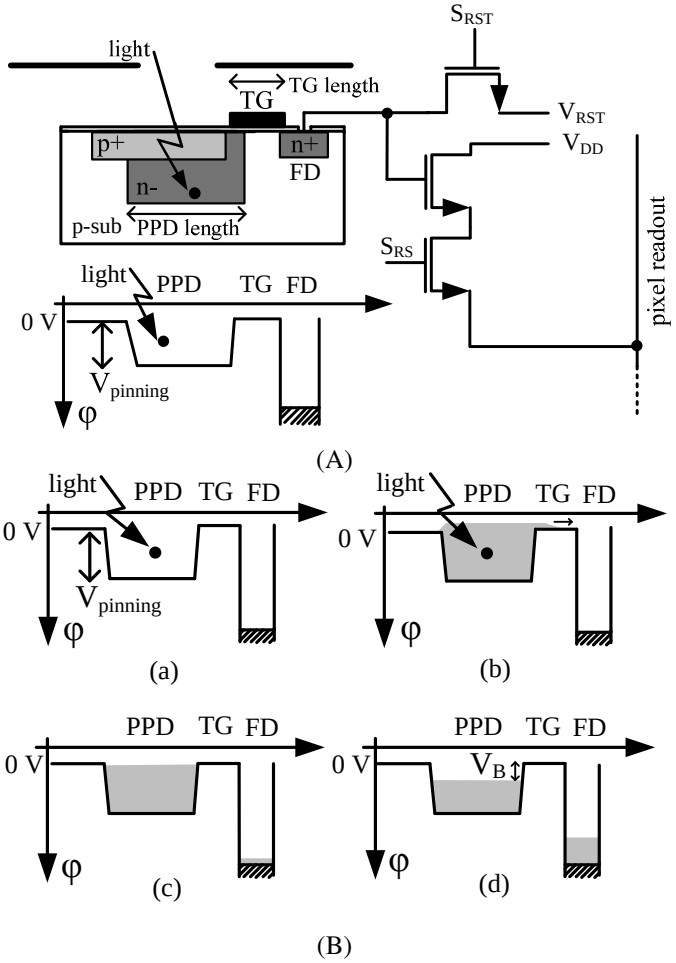

Fig. 1: *Pinned photodiode operation (A)standard pinned photodiode (B)operating principle of pinned photodiode: a) before charge integration, b) during and after charge integration, c) photodiode filled to full well, d) feed-forward charge transfer to FD.*

The movement of electrons from the photodiode potential well to the FD node is a two-step process. Initially the potential difference between the photodiode well and the FD node facilitates the movement of electrons. The charge arrangement in the photodiode potential well when full, results in an asymmetrical TG barrier potential near the edges [2]. This asymmetry and the self-induced drift will tend to transfer any free moving charges to the FD node. This charge movement is a function of time and causes an overflow of electrons to the

FD node till a stage is reached wherein the photodiode well potential settles to a stage as shown in figure 1B (d). After the initial phase, thermionic emission helps the electrons to flow to the FD node. However this process is very slow as the electrons need to overcome the barrier height of V_B as shown in figure 1B.

The charge handling capacity and charge transfer (in)efficiency of the CCD are well published in literature, while the charge handling capacity of the CMOS PPD has not yet been well documented. For a CCD, a barrier height of nearly 0.5V-0.6V has been reported in [3], [4], [5]. In this paper we present the feed-forward effect in a 4-Transistor CMOS pixel. The feed-forward voltage is a function of storage time, photodiode well capacity, photodiode geometry and temperature [6]. In section II the experimental setup is briefly described and the experimental results of the feed-forward voltage with variations in barrier height, storage time, photodiode and barrier geometry and temperature are presented. It is shown that the minimum barrier height required to hold the electrons in the PPD is 0.5V for CMOS image sensors. Finally section III concludes this paper.

II. Experiments and Results

The microphotograph of the designed image sensor is shown in figure 2 and the specifications are listed in table 1.

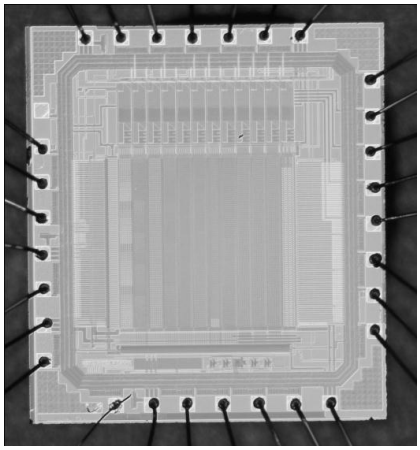

Fig. 2: *Microphotograph of the chip.*

Process	TSMC 0.18 µm CMOS CIS
Pixel pitch	15 µm
Fill factor	7% up to 44%
Sense node area	25.5 μ^2
Conversion gain	8.96 µV/e^-
TG lengths	0.7 µm, 1.0 µm, 1.5 µm, 2.0 µm
PPD lengths	1.2 µm, 3.2 µm, 5.2 µm, 7.2 µm, 9.2 µm
Pixel array	6 x 4 (for each TG and PPD length variation)

TABLE I: *Sensor specifications and performance.*

The designed imager consists of test structures of varying dimensions of TG and PPD lengths as shown in the figure 3.

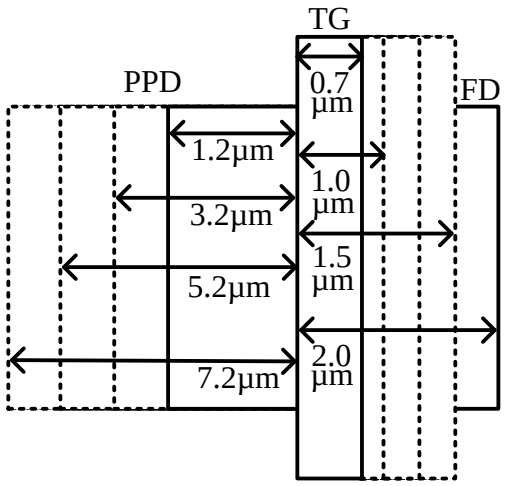

Fig. 3: *Geometrical variations in the TG and PPD lengths of the pinned photodiode.*

The pixel circuitry is similar to a standard CMOS 4-Transistor pixel with a pinned photodiode with the exception that the reset voltage level (V_{RST}) may be controlled from external via an external signal line. During the measurements the photodiode well is filled electrically by injecting charges from the reset voltage. The reset voltage is changed between high and low voltage levels (V_{RST_low}), where the lower level is used to inject a controlled number of electrons into the photodiode well. After filling the photodiode well, the TG is closed and the floating diffusion node is reset. The captured reset image is denoted as the image 1 in figure 4.

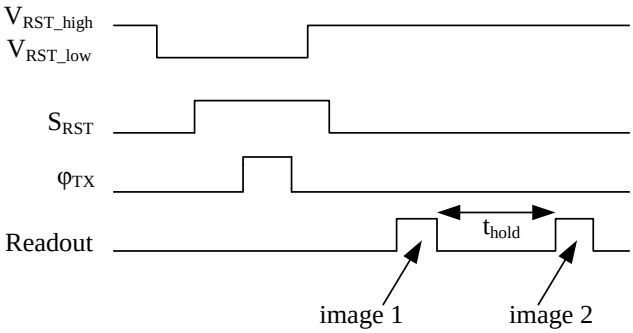

Fig. 4: *Pixel timing diagram for minimum barrier height determination.*

After a variable charge holding time (t_{hold}) the signal image, denoted as image 2 in figure 4, is captured and it is subtracted from the reset image in order to compensate pixel offsets. The t_{hold} is the time allowing the charges to feed into the FD node.

Figure 5 shows the measured feed-forward voltage on the floating diffusion node for varying V_{RST_low} levels and TG lengths at a temperature of 293K. The feed-forward voltage at the FD node is higher, when the photodiode well is completely full (V_{RST_low} = 0 V) as compared to when the photodiode is below its full well capacity (V_{RST_low} > 0 V). The decreasing

of feed-forward effect with an increase in TG length as seen in figure 5 is the result of a longer barrier that restricts more efficiently the overflow of electrons. Further it is found that the feed-forward voltage for the longer photodiodes is higher compared to the smaller photodiodes. Thus it can be inferred that the feed-forward voltage is proportional to the number of electrons in the photodiode well. For V_{RST_low} higher than 0.1V, the voltage on the FD is nearly constant and is the result of the integration of the dark electrons on the FD node.

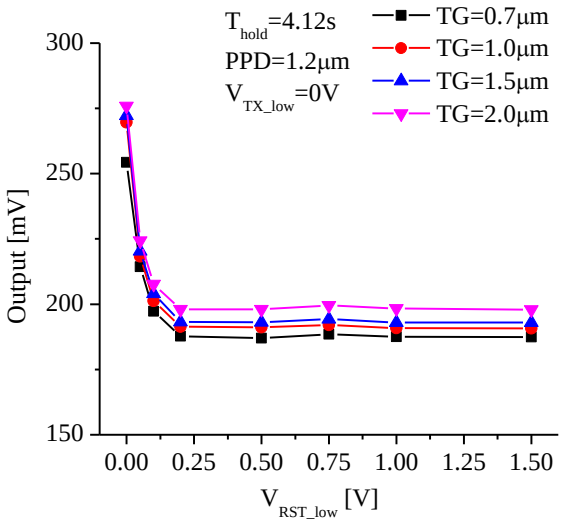

Fig. 5: *The FD node variation for varying V_{RST_low} and TG lengths.*

The probability that the electrons jump the potential barrier to reach the FD node is proportional to the total number of electrons in the photodiode well [6]. Figure 6 shows the feed-forward voltage with increasing charge holding time and the PPD length. The increase in the PPD length increases the charge handling capacity of the photodiode, thus proportionally increasing the feed-forward voltage. Further it is seen from the figure the feed-forward voltage saturates for long charge holding times, indicating that most of the electrons from the photodiode well has crossed the potential barrier and have reached the FD node.

The feed-forward voltage also depends on the operating temperature. As the temperature increases the electrons in the photodiode gains in kinetic energy and are thus able to cross the photodiode potential barrier more easily. The feed-forward voltage variations as a function of temperature is shown in figure 7. When there is no feed through, only the dark electrons are integrated on the FD node.

In CMOS 4-Transistor pixels with pinned photodiodes, the effective barrier, which is needed to hold the electrons inside the photodiode well, is determined by the voltage applied on the TG. The TG voltage is converted into an effective channel potential by a function that depends on the doping of both the gate and the channel. To understand the behavior and experimentally determine the effective barrier potential, the TG potential is varied with respect to the photodiode well

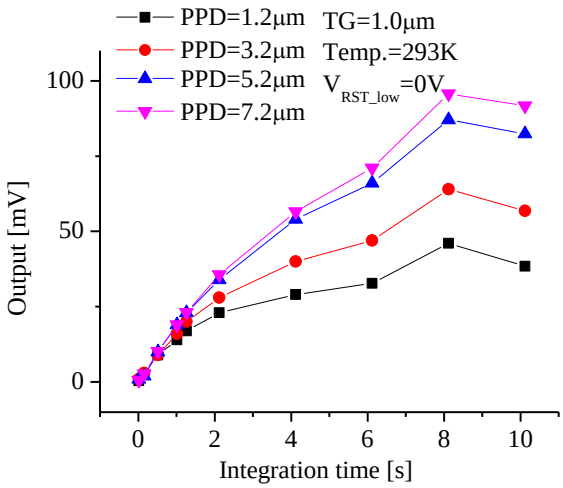

Fig. 6: *The FD node variation for varying t_{hold} and PPD lengths.*

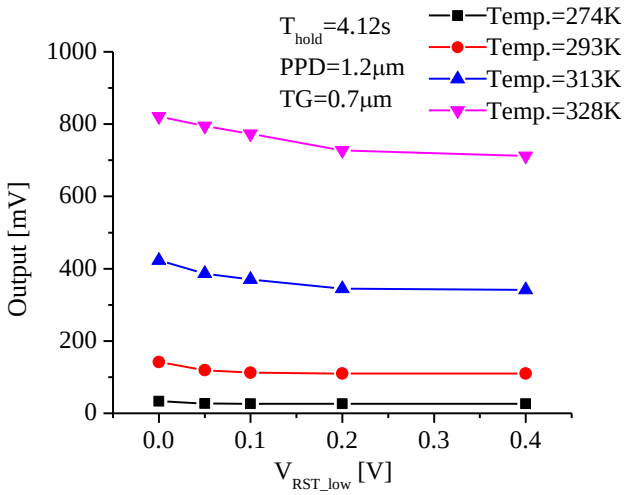

Fig. 7: *The FD node variation for varying V_{RST_low} and temperature.*

potential. If V_{RST_low} is below the pinning voltage of the photodiode, some charges will be injected into the photodiode. However, when V_{RST_low} is higher than the pinning voltage, no charges will be injected into the photodiode well, thus the voltage change on the FD node would only be due to dark current generation in the FD node. Thus when V_{RST_low} is maintained lower than the pinning voltage of the photodiode and the TG channel potential is increased, the feed-forward voltage would be expected to increase, as the increase in the TG channel potential would lower the barrier potential.

In figure 5, the TG potential was held constant at 0V. Figure 8 shows the feed-forward voltage for varying the TG potential and the TG length and figure 9 with varying PPD length when the photodiode is completely full. Initially the FD node voltage increases with increasing voltage on the TG gate, however for voltages higher than 0.5V, the FD node voltage is nearly constant. This is because when the potential on TG is 0.5V; all the electrons have already overflowed from the

photodiode to the FD node when the photodiode well depth is 1V.

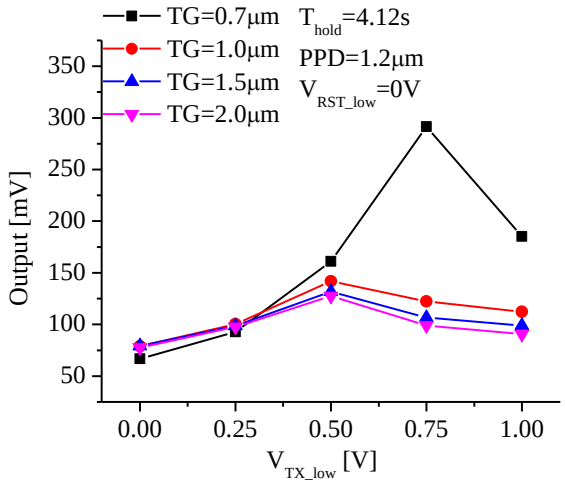

Fig. 8: *The FD node variation for varying V_{TX_low} and TG lengths.*

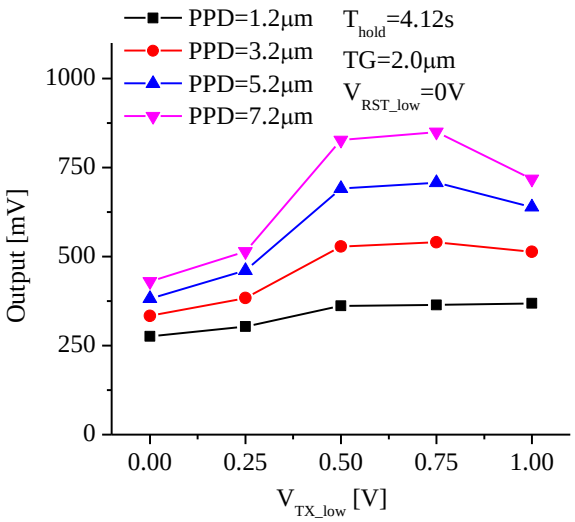

Fig. 9: *The FD node variation for varying V_{TX_low} and photodiode length.*

The FD node output due to feed-forward of charges decreases with decreasing injected electrons as shown in figure 10. However for V_{RST_low}=0.5V, the FD node voltage does not change and reflects the integrated dark current.

III. Conclusion

In this paper the effect of feed-forward in standard pinned photodiodes of CMOS image sensors is shown. The full well capacity of the photodiodes defines the signal-to-noise ration and dynamic range of the image sensor and thus is very important. The full well capacity of the photodiodes is determined by the barrier height that is needed to prevent the overflow of electrons. The barrier height depends on the total number of electrons in the photodiode, the time for which these electrons are held, the geometry of the photodiode and the barrier, the potential on the barrier and the operating

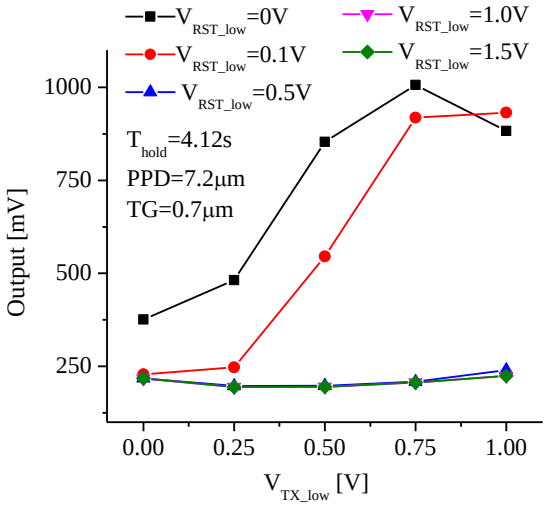

Fig. 10: *The FD node variation for varying photodiode well capacity and potential on the TG.*

temperature. From experiments, it was determined that a minimum barrier of 0.5V is necessary to hold the electrons in the photodiode well. This is consistent with the minimum barrier measured for CCDs. If the barrier height is insufficient, some electrons from the photodiode are fed into the floating diffusion node leading to a loss of charges and lowering the full well capacity of the photodiode. The transfer of the electrons is aided by increase in the operating temperature. At higher temperatures, the electrons have higher energy and are thus able to overcome the potential barrier and reach the floating diffusion node. These studies are important to understand the effects of temperature and holding times of electrons on the potential barrier separating the photodiode and the floating diffusion node for a higher dynamic range and SNR of an image sensor.

Acknowledgement

The authors would like to thank the team of MESA Imaging for proving the measurement set-up and help with the analysis.

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