Feedforward Effect in Standard CMOS Pinned Photodiodes

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***Abstract*—The charge handling capacity or the full well of the photodiodes used in CMOS image sensors is a very important characteristic because it affects the saturation level and the dynamic range of the image sensor. The scaling of the pixel size to increase the spatial resolution is also reducing the barrier separating the photon detection and the collection node in a standard pinned photodiode (PPD). The barrier reduction and the thermionic emission of the electrons allow some of the charges from the photodiode well to feed into the collection node, resulting in a feedforward voltage. In conventional readout of the pixels, this feedforward voltage is neglected and lost when the collection node is reset. The barrier height of the transfer gate (TG) determines the quantity of electrons held back in the photodiode well. Thus, the knowledge of this barrier height is very important in determining the true charge handling capacity of the photodiode potential well. Experiments with standard PPDs showed that a barrier height of around 0.5 V is needed to hold the electrons in the photodiode potential well. This is analogous to the barrier potential for charge-coupled devices reported in the literature. Furthermore, the barrier height dependence on the charge storing time in the photodiode well and the structural dimensions of the TG and photodiode length are also explored in this paper.**

***Index Terms*—Barrier height, charge transfer, CMOS image sensor, feedforward voltage, pinned photodiode (PPD).**

I. Introduction

CMOS IMAGE sensors have become very popular in all fields of electronic imaging, particularly in low-cost imaging devices, for example, consumer applications. The sensors are always tried to be optimized further for delivering high-quality images. The quality of an image is particularly characterized by the maximization of the following parameters: pixel resolution, signal-to-noise ratio (SNR), and dynamic range. All these parameters are strongly related to the full well, which is the maximum number of electrons that can be stored in a pixel without any loss.

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Spatial resolution: Larger numbers of pixels enable the imaging of finer spatial details of the scene. The increase in the pixel number without increasing the total die area of CMOS image sensors has led to a continuous process of scaling down the pixel size. The smallest pixels today measure 1 μm or less, and the trend is going further to even smaller structures. Regarding the full well of the pixel, this downscaling trend is reducing the photodiode's well capacity [1] and the potential barrier separating the charge generation centers from collection and readout, which, in turn, negatively affects both the maximum achievable SNR and the dynamic range.

SNR: A high SNR is important in order to obtain images of uniform segments and in order to individually perceive them as a realistic scene. Assuming photon shot noise limited signal detection, the maximum achievable SNR benefits from the full well capacity in the sense that the SNR proportionally increases to the square root of the signal itself.

Dynamic Range: The dynamic range of a sensor expresses the ability to capture dark and bright sections within an image while maintaining the highest fidelity. Technically expressed, the dynamic range is the ratio of the largest possible signal divided by the smallest possible signal that is still detectable. A low dynamic range would mean a loss of perceived intensity information, which, however, is tried to be avoided by an appropriate pixel design for high dynamic range coverage. An increased dynamic range can be achieved by either lowering the noise floor or increasing the full well capacity.

A. Full Well in a Four-Transistor Pixel

In a standard four-transistor pixel, as shown in Fig. 1, the pinned photodiode (PPD) collects the charges generated by the photons, and a transistor with a transfer gate (TG) is used for transferring the collected charges from the photodiode to the floating diffusion (FD) node. The pixel also includes a transistor S_{RST} for resetting the FD to a predetermined voltage level V_{RST} prior to the charge transfer. The other two transistors are the source follower and row select transistor S_{RS}. The row select transistor loads the column bus with the pixel output for readout. The PPD forms a fully depleted n-region, which is "pinned to a voltage" V_{pinned}. In this region, the photogenerated charges are collected and stored until the readout starts by transferring the charges to the FD. In such a pixel configuration, the potential well in the PPD forms the storage well, whereas a low voltage on the TG forms the barrier region preventing the electrons from exiting the PPD region.

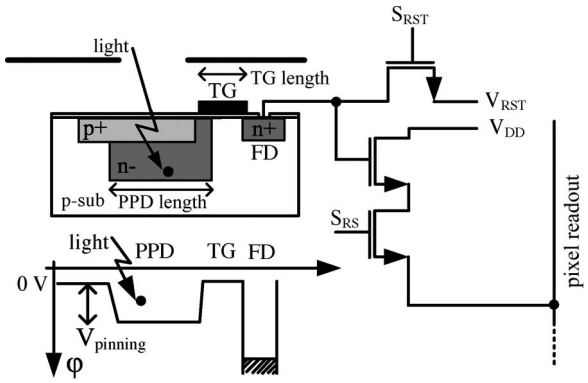

Fig. 1. Four-transistor pixel.

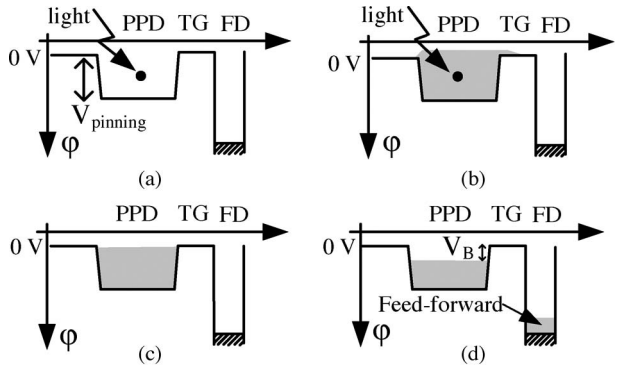

Fig. 2. PPD operation. (a) Before charge integration. (b) During and after charge integration. (c) Photodiode filled to full well. (d) Feedforward charge transfer to FD.

The full well capacity of the PPD region is determined by the number of electrons that the potential well can store. Since the potential barrier generated by the TG's channel potential prevents the overflow of the collected electrons, the size of the gate and the channel doping must have a strong influence on the well capacity. In addition to that, the temperature affects the well capacity value, too. Electrons contained within a well possess thermal energy kT, where k is the Boltzmann's constant, and T is the absolute temperature, and thus, the electrons acquire random thermal velocities. Consequently, the potential barrier needs to be large enough in order to suppress any electron overflow due to thermal agitation when the PPD region is full of electrons [2]. The charge handling capacity and the charge transfer (in)efficiency of the charge-coupled device (CCD) are published in literature, whereas the charge handling capacity of the CMOS PPD has not yet been well documented. A barrier height of 0.5 V for typical vertical-CCD structures was reported in [3], whereas [2] reported a barrier voltage of 0.6 V at a full well of 500 ke$^-$ and at room temperature for buried-channel CCDs. The barrier voltage for thermionic emission in full-frame CCDs is also reported to be around 0.5 V [4].

B. Outline

In this paper, we investigate the feedforward effect in a four-transistor CMOS pixel. Feedforward results due to the overflow of electrons from the photodiode to the FD when the barrier potential is too low. The theory of feedforward is explained in Section II. Experiments have been performed in Section III, and results are presented in Section IV. Finally, Section V concludes this paper.

II. Theory on Feedforward in a Four-Transistor Pixel

The operation of a PPD pixel is described in Fig. 2 by considering the potential setups during different operation phases. The PPD is completely empty after reset; newly generated charges are collected, assuming the pixel is exposed to light. This is shown in Fig. 2(a). After the integration of the charges in the photodiode well, the TG is opened, allowing the accumulated charges to flow into the FD and to be read out. Ideally, when the TG is closed (acting as a barrier), no electrons from the photodiode potential well will flow to the FD node. However, from literature, it is known that, even when the TG is closed, some of the electrons will cross the potential barrier and reach the FD node. In order to investigate the charge leakage to the FD node, the pixel accumulates as long as needed so that the PPD potential well is totally filled. Fig. 2(b) shows that, if the PPD maximum storage value is exceeded, electrons will start to overflow to the FD node. If the light exposure is stopped in this phase of the operation, electrons will continue to overflow to the FD node until the flat-voltage situation in Fig. 2(c) is reached.

Both diffusion and self-induced drift of electrons due to gradients in the charge concentration contribute to the movement of electrons from the photodiode well toward the FD node during this phase. The initial overflow is also helped by the charge arrangement in the photodiode potential well. According to Carnes *et al.* [5], the charges placed in a square well with no externally induced electric fields in the interior will tend to crowd at the edges of the well due to the mutually repulsive properties of like charges similar to the arrangement of charge on a conducting disk in free space. The photodiode wells are not perfectly square; however, they still result in higher charge concentration near the edges.

After reaching the flat-voltage condition, the electrons continue to flow to the FD node due to thermionic emission. This process is very slow as the electrons need to overcome the barrier height of V_B presented by the TG to reach the FD node, as indicated in Fig. 2(d). The process of charge flow due to thermionic emission is investigated more deeply in the succeeding discussion.

The number of electrons that are able to escape the photodiode well will be proportional to the $\exp(qV_B/kT)$, where q is the electron charge, k is the Boltzmann's constant, V_B is the barrier potential presented by the TG, and T is the absolute temperature. The overflow current dQ/dt can be expressed as a function of the barrier potential V_B as [6]

$$\frac{dQ}{dt} = I_0 e^{\left(\frac{-qV_B}{kT}\right)} \tag{1}$$

where I_0 is the current coefficient, which is a function of the semiconductor device's structure and its impurity concentration. The overflow current defined in (1) causes the charges Q in the potential well to decrease with time. If these changes in the charge levels are not very large, then it can be reasonably

assumed that the photodiode well capacitance is constant, and thus, Q can be expressed as

$$Q = C(V_{\text{pinned}} - V_B) \tag{2}$$

where V_{pinned} is the pinning voltage, C is the well capacitance, and V_B is the barrier potential. Using (1) and (2) and integrating over time the charges held in the photodiode potential well, the barrier potential can be then expressed as

$$V_B = \frac{kT}{q} \ln\left(\frac{q}{kTC} I_0 t_{\text{hold}} + 1\right) \tag{3}$$

where t_{hold} is called the holding time during which the charges are held in the photodiode. This corresponds to the integration time of any overflowing electrons to the FD node.

From (2) and (3), it is evident that, for a PPD, the probability of an electron in the photodiode well crossing the barrier to reach the FD node is depending on the following factors:

- the number of electrons (since $Q = qN$, where N is the total number of electrons in the photodiode well);
- the operating temperature;
- the holding time t_{hold} the charges are stored in the photodiode well;
- the structural dimensions and geometry of the TG length and the photodiode length, because the photodiode length affects the well capacitance C, and the geometrical parameters and doping concentration influence the current coefficient I_0;
- the surface potential in the channel of the TG (directly related to the barrier height with respect to the pinning potential of the photodiode, thus influencing the total number of electrons N that can be accumulated in the photodiode well).

The overflow of electrons has profound effects on the design and operation of CMOS photodiodes. One immediate effect of the decrease in the barrier potential is the overall reduction in the full well capacity of the photodiode. Two distinct states of the full well, namely, static and dynamic full well, for the CCDs were mentioned in [2], which is also found to be true for CMOS PPDs.

The overflow current on the FD node due to the movement of free charges, even in the presence of a TG barrier between the photodiode and the FD node, results in a "feedforward voltage" [7]. The feedforward voltage on the FD node is shown in Fig. 2(d). In this paper, we focus on the feedforward voltage variations due to the barrier height modulation at a constant temperature by varying the total number of electrons in the photodiode well at the start time and by varying the TG channel voltage. The variation of the barrier height with changes in temperature will be published as a different paper.

III. Experiments

Here, the test sensor is described first, and second, the experimental setup is presented with special focus on the timing diagram of the controlling signals used for extracting the information on the pixel full well.

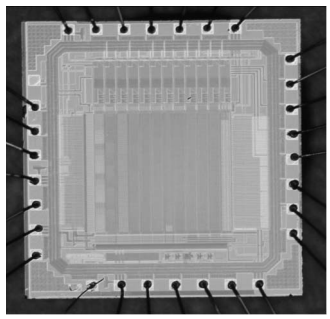

Fig. 3. Microphotograph of the test chip.

A. Sensor Description

The microphotograph of the designed test image sensor is shown in Fig. 3.

The image sensor was designed in a Taiwan Semiconductor Manufacturing Company 0.18-μm CMOS image sensor process with a pixel pitch of 15 μm and a maximum fill factor of 44% depending on the different pixel geometries. The area of the FD node is 25.5 μm^2, which corresponds to a conversion gain of 8.96 μV/e$^-$ for the chosen technology. Each variation in the pixel geometry is represented by an array of 6×4 pixels. The TG length was designed for sizes of 0.7, 1.0, 1.5, and 2.0 μm; whereas the photodiode lengths selected were 1.2, 3.2, 5.2, 7.2, and 9.2 μm; all photodiodes have the same width. The rest of the pixel circuitry is the same as in standard CMOS four-transistor pixels with a PPD.

B. Experimental Setup

In conventional PPD readout, the potential on the TG of the four-transistor pixel is made more positive than the photodiode well but less positive than the FD node potential during the phase of shifting charge from the diode to the readout node. The abrupt step in potential distribution generates high electric fields, and thus, the charges are efficiently swept in terms of speed from the photodiode well to the FD node, lowering the FD potential.

The following measurements apply a special timing control scheme to the four-transistor test pixels, aiming for determining the minimum potential barrier height between the photodiode well and the TG barrier. A minimum barrier is needed to hold the electrons in the photodiode area without significant electron loss due to leakage to the FD node. Particularly, leakage due to thermionic agitation of electrons is considered herein.

The dedicated timing diagram for the operation of the pixels is shown in Fig. 4. Since the measurement of the overflow current due to thermionic emission requires the avoidance of light incident, the measurement itself is accomplished in a dark environment. The initial filling up of the photodiode by electrons is accomplished electrically instead of optically. This is achieved by activating both the reset and TG signals and setting the reset voltage to low level $V_{\text{RST\_low}}$. While the reset voltage low level is configurable off-chip, $V_{\text{RST\_high}}$ is fixed to the 3.3-V power supply. The variability of $V_{\text{RST\_low}}$ enables an accurate control of injecting a certain number of electrons into the photodiode. $V_{\text{RST\_high}}$ is used in a second phase to reset the FD node to a high potential.

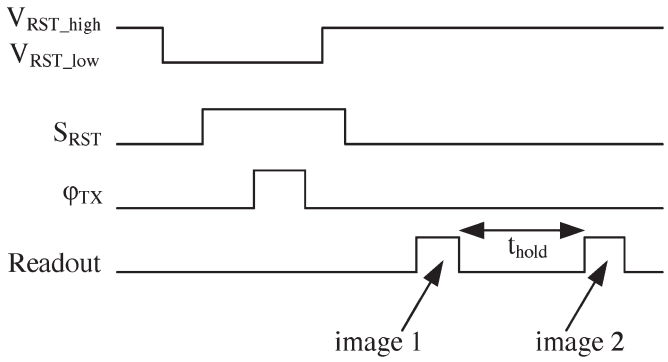

Fig. 4. Pixel timing diagram for minimum barrier height determination.

A special situation is reached when $V_{\mathrm{RST\_low}}$ is set to a voltage higher than the pinning voltage of the photodiode. In this case, no charges will flow into the photodiode during the injection phase. The pinning voltage for the pinned photodiodes is experimentally found to be around 1 V [8].

After the initial phases of filling up the photodiode well by electrons and resetting the FD to a high potential, a first image is captured, representing the reset levels. After a holding time t_{hold}, which can be externally chosen, a second image is captured, representing the signal levels. The signal levels constitute the electrons collected during the holding time, meaning any dark current contribution. By subtracting the two images of signal and reset levels, a correlated double sampling process in the digital domain is accomplished, enabling the elimination of any pixel-inherent offsets and kTC noise components.

One restriction of the measurement setup, and worth mentioning, is the fact that the first few microseconds of the electron overflow process cannot be resolved. The reason is a minimally required time duration of 25 μs between the falling edges of the TG and reset signals and some delay until the readout of the pixels starts. A faster control sequencer would have to be set up in order to improve the resolution at the beginning of the charge flow process.

For each condition of different levels of charges injected into the photodiode region, a total of 50 frames is continuously recorded. Temporal averaging is performed on a per-pixel basis in order to reduce random pixel noise and to improve the confidence of the observed data.

IV. Results and Discussion

In Section II, it was shown that the full well and thus the feedforward voltage due to the overflow of electrons from the photodiode potential well to the FD node is a function of time, temperature, barrier potential, and the TG and photodiode geometrical cross sections. Here, the relationship between the barrier potential of the TG and the amount of charges in the photodiode well is experimentally explored according to the afore-described measurement procedure.

A. Feedforward Voltage Changes Due to Variations in the Stored Charge Quantity

Here, the relationship between the barrier height and the stored charge quantity Q in the photodiode well is evaluated. The number of electrons in the full well is varied by adjusting the lower level of the reset voltage $V_{\mathrm{RST\_low}}$, as explained in Section III-B.

Fig. 5 shows the measured feedforward voltage on the FD node for varying $V_{\mathrm{RST\_low}}$ levels and TG lengths at a temperature of 293 K. The low voltage applied on the TG is always 0 V, thus preventing the creation of any direct channel between the FD node and the photodiode well. Fig. 5(a) and (b) is for a short charge holding time of $t_{\mathrm{hold}} = 20$ ms with photodiode lengths of 1.2 and 7.2 μm, respectively. Fig. 5(c) and (d) is for a longer charge holding time of $t_{\mathrm{hold}} = 4.12$ s and for photodiode lengths of 1.2 and 7.2 μm, respectively. As stated in Section II, $V_{\mathrm{RST\_low}} = 0$ V corresponds to the maximal possible full well of the PPD, whereas other values of $V_{\mathrm{RST\_low}}$ correspond to those lower than that.

Fig. 5 shows two distinct trends.

1) The feedforward voltage at the FD node is high when the photodiode well is completely filled by electrons by setting $V_{\mathrm{RST\_low}} = 0$ V, and the feedforward voltage is getting lower when the photodiode is below its full well capacity. Furthermore, the feedforward voltage for the longer photodiodes is higher compared with the smaller photodiodes. Thus, it can be inferred that the feedforward voltage is proportional to the number of electrons in the photodiode well.
2) If $V_{\mathrm{RST\_low}}$ is higher than 0.1 V, the voltage on the FD is nearly constant. Thus, the photodiode can be considered to be not full. No electrons due to thermionic emission are flowing to the FD node. The offset in the curves is only the result of the integration of the dark electrons on the FD node directly.

Table I summarizes the dark voltage and the feedforward voltage on the FD node for different TG and PPD dimensions and charge holding times. The FD node output for $V_{\mathrm{RST\_low}} = 0.2$ V is denoted as dark voltage, whereas the FD node output for $V_{\mathrm{RST\_low}} = 0$ V is referred as feedforward voltage.

A first observation from this table is that the feedforward effect is getting less important with a longer TG length if short charge holding times are considered. If, however, the charge holding time is large, the feedforward dependence on the TG disappears. This is pointed out in more detail in the following: At 20-ms charge holding time, the increase in the TG length from 1.0 to 2.0 μm causes about 17% less electrons flowing from the photodiode to the FD node. However, it should be noted that, for the small holding time, the voltage levels on the FD node are only in the range of a couple of millivolts. This is close to the noise limit of the setup, and thus, the corresponding lower data confidence compared with the one achieved with the long charge holding time must be reminded at this point. Considering a longer charge holding time ($t_{\mathrm{hold}} = 4.12$ s), there is no clear trend visible anymore for the feedforward voltage dependence on the TG length.

The decrease of feedforward effect with an increase in TG length, which is particularly visible at short charge holding times, is the result of a smaller current coefficient in (3), because the longer barrier more efficiently restricts the overflow of electrons. The reason for the less visible dependence of the feedforward voltage on the TG length in the case of long charge holding times is given by the fact that, in any case, the

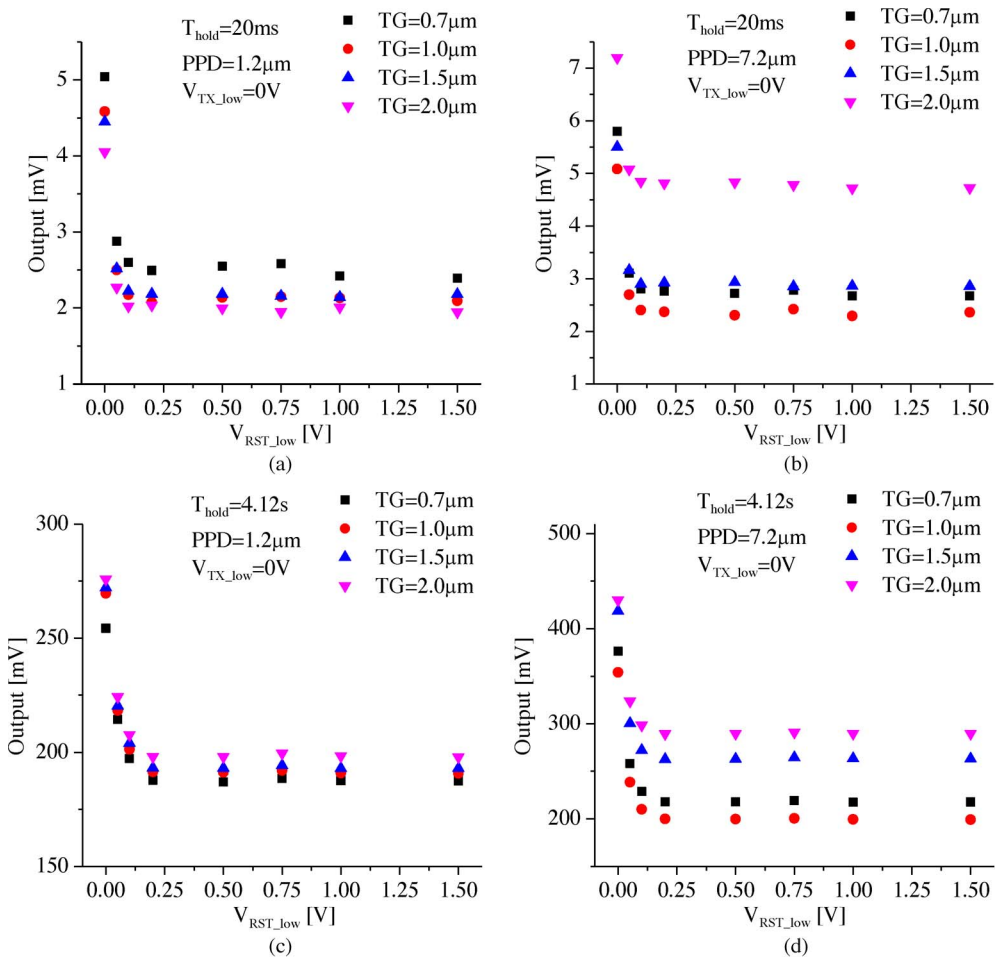

Fig. 5. FD node variation for varying $V_{\mathrm{RST\_low}}$ and TG lengths. (a) t_{hold} of 20 ms and PPD length of 1.2 μm. (b) t_{hold} of 20 ms and PPD length of 7.2 μm. (c) t_{hold} of 4.12 s and PPD length of 1.2 μm. (d) t_{hold} of 4.12 s and PPD length of 7.2 μm.

TABLE I
DARK VOLTAGE AND FEEDFORWARD (FF) VOLTAGE AT 293 K FOR VARYING TG AND PPD GEOMETRY

TG length	t_{hold}=20ms						t_{hold}=4.12s					
	PPD=1.2μm			PPD=7.2μm			PPD=1.2μm			PPD=7.2μm		
	Dark voltage [mV]	FF voltage [mV]	FF DC comp. [mV]	Dark voltage [mV]	FF voltage [mV]	FF DC comp. [mV]	Dark voltage [mV]	FF voltage [mV]	FF DC comp. [mV]	Dark voltage [mV]	FF voltage [mV]	FF DC comp. [mV]
0.7μm	2.41	5.04	2.63	2.67	5.80	3.13	187.55	254.34	66.79	219.11	376.21	157.10
1.0μm	2.13	4.58	2.45	2.29	5.09	2.80	190.88	269.70	78.82	199.53	354.17	154.64
1.5μm	2.14	4.45	2.31	2.86	5.50	2.64	192.16	272.24	80.08	263.37	418.53	155.16
2.0μm	1.95	4.05	2.10	4.72	7.20	2.48	198.36	275.89	77.53	289.61	430.14	140.53

thermal equilibrium state tends to generate the same potential distribution for diodes with a short and with a large TG. A long charge holding time of several seconds approximates to the equilibrium situation, and differences due to thermionic emission of electrons become less visible in the voltage domain.

A second observation from Table I is the increase in the feedforward voltage when larger photodiodes are used. The explanation for this tendency is the following: The photodiode length, which is defined as the length of the diode's n-layer implant length, affects the electron concentration and thus the well capacitance but not the barrier height [3]. A larger PPD means that more electrons can be stored. At the same time, more electrons experience thermal agitation so that the likely number of electrons crossing the TG barrier due to thermionic emission increases, too.

In Fig. 5, it is observed that, for a short charge holding time and a TG length of 1.0 μm, the increase in the photodiode length from 1.2 to 7.2 μm causes a 14.3% increase in the FD node output, whereas for a TG length of 2.0 μm, the increase is 18%. The percentage increase is calculated as

$$\%\ \text{increase in FD node output} = \frac{[V_{\mathrm{FF}} - V_{\mathrm{Dark}}]_{\mathrm{PPD}=7.2\ \mu\mathrm{m}} - [V_{\mathrm{FF}} - V_{\mathrm{Dark}}]_{\mathrm{PPD}=1.2\ \mu\mathrm{m}}}{[V_{\mathrm{FF}} - V_{\mathrm{Dark}}]_{\mathrm{PPD}=1.2\ \mu\mathrm{m}}} \tag{4}$$

where V_{FF} is the feedforward voltage. Considering the measurements with a long charge holding time of 4.12 s, the FD node increases by 96% for a TG length of 1.0 μm, whereas for the TG length of 2.0 μm, the increase is only 81%.

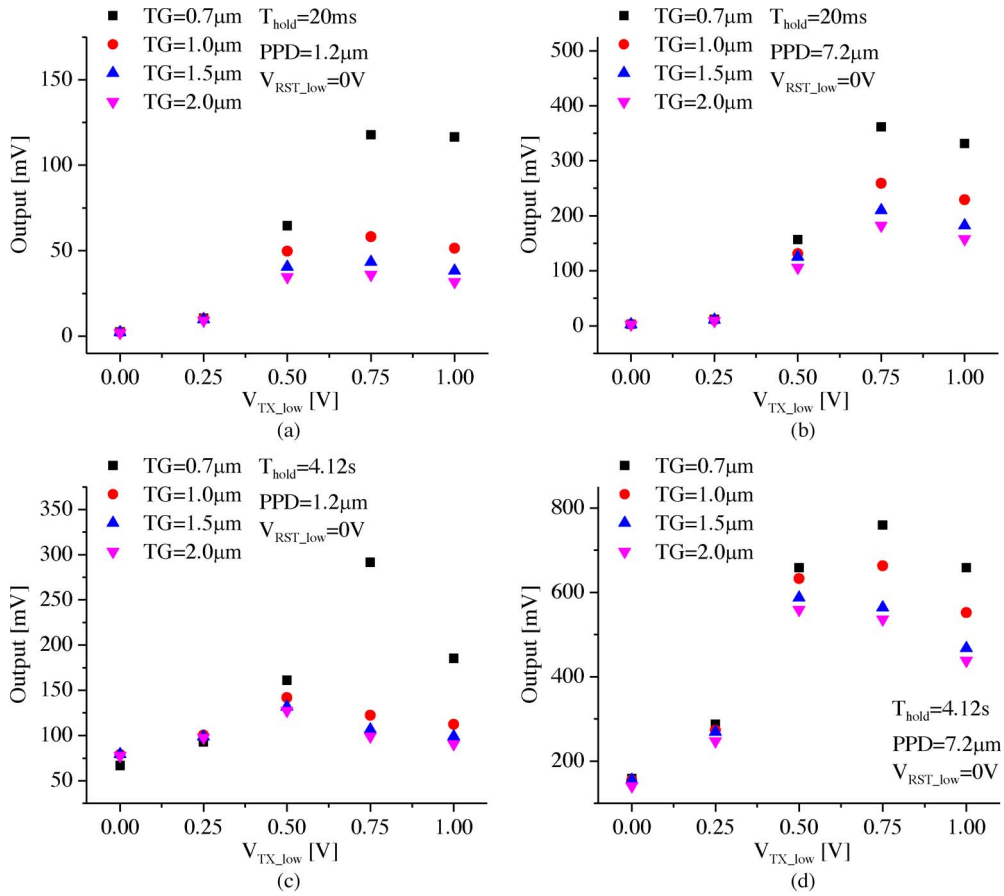

Fig. 6. FD node variation for varying $V_{\mathrm{TX\_low}}$ and TG lengths. (a) t_{hold} of 20 ms and PPD length of 1.2 μm. (b) t_{hold} of 20 ms and PPD length of 7.2 μm. (c) t_{hold} of 4.12 s and PPD length of 1.2 μm. (d) t_{hold} of 4.12 s and PPD length of 7.2 μm.

B. Feedforward Voltage Changes Due to Variations in the Channel Potential of the TG

In classical CCDs, it was found that the minimum barrier needed to hold the electrons in the photodiode well is around 0.4–0.6 V [2]. In CMOS four-transistor pixels with PPDs, the effective barrier within the charge transport channel, which is needed to hold the electrons inside the photodiode well, is determined by the voltage applied on the TG. The TG voltage is converted into an effective channel potential by a function that depends on the doping of the gate, the channel, and the substrate. As a result, an inherent voltage beneath the TG, even when the TG is held at 0 V, is generated.

To understand the behavior and experimentally determine the barrier potential, the TG potential is varied with respect to the photodiode well potential. The lower voltage level of the TG pulse is adjusted between 0 and 1 V, whereas the higher level is fixed to 3.3 V.

As stated in Section III-B, as long as $V_{\mathrm{RST\_low}}$ is below the pinning voltage of the photodiode, some charges will be injected into the photodiode. However, when $V_{\mathrm{RST\_low}}$ is higher than the pinning voltage, no charges will be injected into the photodiode well; thus, the voltage change on the FD node would only be due to the dark current generation in the FD node. Thus, when $V_{\mathrm{RST\_low}}$ is maintained lower than the pinning voltage of the photodiode and the TG channel potential is increased, the feedforward voltage would be expected to increase, as the increase in the TG channel potential would lower the barrier potential.

Fig. 6 shows the measurements of the feedforward voltage for varying the lower voltage level of the TG pulse when $V_{\mathrm{RST\_low}}$ is 0 V, which is the full well condition of the PPD. Fig. 6(a) and (b) is for a short charge holding time with photodiode lengths of 1.2 and 7.2 μm, respectively, whereas Fig. 6(c) and (d) is for a large charge holding time with photodiode lengths of 1.2 and 7.2 μm, respectively.

Some of the trends already shown in Fig. 5 are observed by this measurement as well. However, Fig. 6 shows two further distinct behaviors.

1) For small photodiodes, the FD node voltage increases with increasing voltage of the low level of the TG signal. However, for voltages higher than 0.5 V, the FD node voltage is nearly constant for both short and long charge holding times.
2) For large photodiodes, the FD node voltage is much higher due to the increased charge handling capacity of the photodiode itself. Furthermore, the FD node voltage behavior is similar to the smaller photodiode, wherein the FD node output is nearly constant when the TG voltage is higher than 0.5 V.

When the lower voltage level on the TG pulse is 0.5 V, a maximum electron flow from the photodiode to the FD node is reached. This trend confirms the fact that a minimum zero

TABLE II
FEEDFORWARD VOLTAGE AT THE FOLLOWING CONDITIONS: 293-K TEMPERATURE, FULL WELL FOR VARYING TG AND PPD SIZES, 0.5 V LOW LEVEL OF THE V_{TX} SIGNAL

TG length	t_{hold}=20ms		t_{hold}=4.12s	
	PPD= 1.2μm [mV]	PPD= 7.2μm [mV]	PPD= 1.2μm [mV]	PPD= 7.2μm [mV]
0.7μm	65	156	161	658
1.0μm	50	131	142	632
1.5μm	41	126	132	588
2.0μm	35	106	128	559

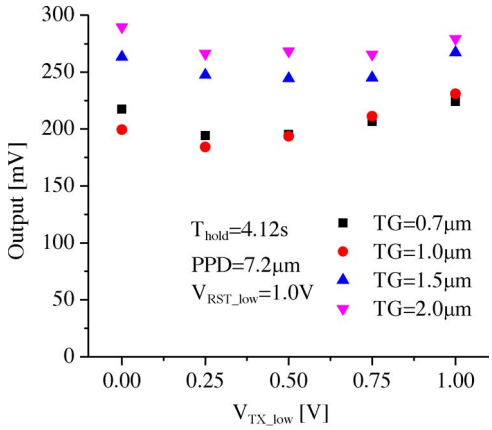

Fig. 7. FD node variation for $t_{\rm hold} = 4.12$ s with $V_{\rm RST\_low} = 1$ V.

barrier is created when the low level of the TG pulse is 0.5 V or higher.

Table II shows the feedforward voltages measured at the FD node output for short and long charge holding times and varying pixel geometrical dimensions. The values are extracted for the case of a zero barrier between the PPD well and the TG, which is obtained for a 0.5 V low level of the $V_{\rm TX}$ signal.

Fig. 7 shows the FD node voltage variations for a long charge holding time when the photodiode well is empty. Since the pinning voltage of the photodiode used is near 1 V, with $V_{\rm RST\_low} = 1.0$ V, no charges are injected into the photodiode, and thus, the FD node should remain constant. For the case of the low-level TG voltage being higher than 0.5 V, the FD node voltage is observed to be relatively constant because the zero-barrier condition is always the starting condition of the overflow process.

C. Feedforward Voltage and Photodiode Length

The feedforward voltage as function of the photodiode length is shown in Fig. 8. As expected, the FD node voltage increases with an increase in the photodiode length until the $V_{\rm TX\_low}$ is around 0.5 V, after which the increase in the FD node is only marginal.

In Fig. 9, $V_{\rm TX\_low}$ has been fixed to 0.5 V, which corresponds to the zero-barrier condition. The number of electrons in the photodiode well is varied by varying $V_{\rm RST\_low}$. According to the figure, there is no electron overflow anymore for $V_{\rm RST\_low} > 0.5$ V. Compared with Fig. 5(c), the difference is the higher voltage of the $V_{\rm TX}$ low level, which enables a zero-barrier starting condition and, thus, shifts the point of

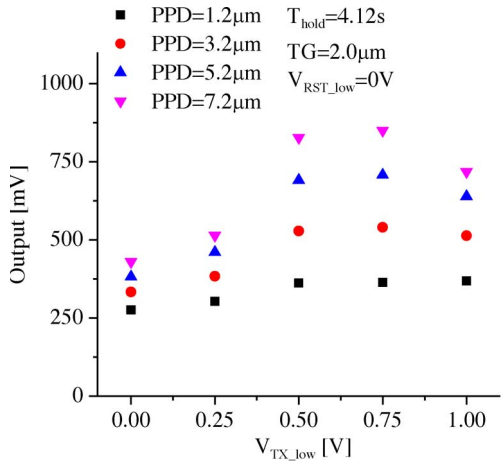

Fig. 8. FD node variation for varying $V_{\rm TX\_low}$ and photodiode length.

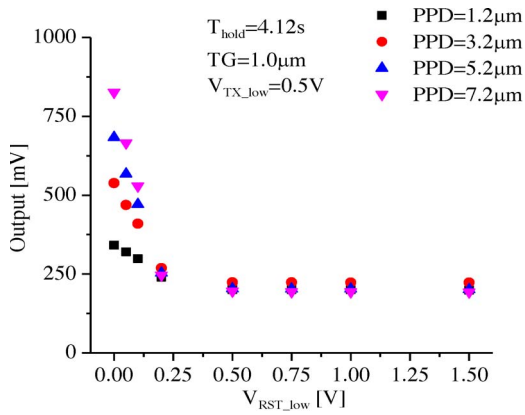

Fig. 9. FD node variation for varying $V_{\rm RST\_low}$ and photodiode length.

constant FD node voltage or the equilibrium state to higher $V_{\rm RST\_low}$ voltages.

V. CONCLUSION

In this paper, we have shown the effect of feedforward in standard PPDs. The full well capacity of a photodiode is defined by the barrier height that is needed to hold the electrons in the photodiode well. From experiments, it was determined that a minimum barrier of 0.5 V is necessary to hold the electrons in the photodiode well. This is consistent with the minimum barrier measured for CCDs. If the barrier height is insufficient, the electrons from the photodiode are fed into the FD node, leading to a loss of charges and lowering the full well capacity of the photodiode. The full well capacity defines the dynamic range, SNR, light sensitivity, and charge saturation of the photodiode and, thus, is an important metric in CMOS imagers.

The magnitude of the barrier is a linear function of temperature and varies as the log of the number of electrons and the amount of time the electrons are stored in the potential well. The transfer of electrons from the photodiode to the FD node in PPDs takes place by a diffusion process. This transfer is aided by the thermal energy of the electrons. These studies are important to model the PPDs for increased well capacity, thus improving the performance of the CMOS image sensors.

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