22.3 A 0.7e^-_{rms}-Temporal-Readout-Noise CMOS Image Sensor for Low-Light-Level Imaging

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For low-light-level imaging, the performance of a CMOS image sensor (CIS) is usually limited by the temporal readout noise (TRN) generated from its analog readout circuit chain. Although a sub-electron TRN level can be achieved with a high-gain pixel-level amplifier, the pixel uniformity is highly impaired up to a few percent by its open-loop amplifier structure [1]. The TRN can be suppressed without this penalty by employing either a high-gain column-level amplifier [2] or a correlated multiple sampling (CMS) technique [3-5]. However, only 1-to-2 electron TRN level has been reported with the individual use of these approaches [2-5], and the low-frequency noise of the in-pixel source follower i.e. *1/f* and RTS noise is a further limitation. Therefore, by implementing a high-gain column-level amplifier and CMS technique together with an in-pixel buried-channel source follower (BSF) [6], the TRN level can be reduced even further.

This paper introduces a CMOS image sensor that integrates an in-pixel BSF, a high-gain column-level amplifier and the digital implementation of the CMS technique in a column-parallel single-slope (SS) ADC. Measurement results show that it achieves a 0.7e^-_{rms} input-referred TRN level. Compared to a conventional CIS without any noise-suppression techniques, this work demonstrates a 40× input-referred TRN reduction, which corresponds to a 32dB SNR improvement. This work also explores the noise-reduction factors that can be achieved with each technique.

Figure 22.3.1 shows a simplified schematic diagram of the sensor with the pixel and the column-readout circuits, and which is fabricated in TSMC's 0.18μm CIS technology. Standard 4T pixels with a pinned-photodiode are used and both SSF and BSF pixels are implemented in the pixel array of 128(H)×198(V) with 10μm pixel pitch. The column readout circuits consist of the column-parallel gain amplifiers with ×1, ×4 or ×16 variable analog gains and SS-ADCs for implementing digital CMS. The column-parallel SS-ADC consists of a comparator driven by a ramp voltage and a bit-wise inversion (BWI) counter [4].

Figure 22.3.2 shows the readout timing diagram of the pixel and column readout circuit. The readout starts by closing the row-select switch (RS) and the reset transistor (RT) of the pixel. Then the column gain amplifier and the comparator are reset as well by sequentially closing the amplifier-reset switch (T_{op}) and the comparator-reset switch (T_{az}). Both reset noise and offset noise of every stage are then stored in a subsequent capacitor and later cancelled by the digital CMS. The digital CMS sequence is as follows. After the pixel is reset, the reset level is available in the column. The column amplifier provides the amplified reset level to the SS-ADC. The amplified reset level is compared with the ramp voltage (V_{ramp}) and the BWI counter is set to count up synchronously. Whenever V_{ramp} is equal to the reset level, the BWI counter stops and stores the reset value in digital. In the case of M-times reset-level sampling, the ramp voltage performs up/down ramping M times while the BWI counter counts M times up. The latched counter output thus corresponds to M-times sampling of the pixel-reset level. After the signal charge is transferred by opening the transfer transistor (TX), the comparator input voltage (V_C) goes up to the amplified signal level voltage. During the charge-transfer period, each bit of the BWI counter is inverted to perform a 1's complement operation by applying a control pulse (B). Then the BWI counter holds the negative value of M-times reset-level sampling as an initial value in the signal conversion. During signal-level conversion, the ramp voltage and the BWI counter are configured in the same manner as the reset-level sampling, thus providing M-times signal-level sampling. Eventually, the counter provides the M-times CMS value of the pixel with analog gain. During the whole conversion, the switch T_{SH} is always closed in order to monitor the column voltage of the source follower, V_{SF}. It should be noted that the ADC's hardware complexity is independent of the exact value of M, since this is determined by a simple change in the clocking pattern. This makes the ADC reconfigurable in a very simple way.

Figure 22.3.3 shows the measured input-referred TRN of BSF and SSF pixels. During the measurements, the sensor operates at 3fps, a 120MHz clock is used to drive the column-parallel SS-ADCs in 12b mode, different gain configurations with 4-times digital CMS are implemented, and the pixel TX is grounded to verify the TRN from dark shot noise. With a pixel conversion gain of 45μV/e^- and ×64 analog gain, the input-referred TRN of BSF pixels achieves 0.76e^-_{rms} under 2.5V reset voltage (V_{rt}). Lowering the reset voltage on BSF pixels can also reduce the TRN [6]; a 0.70e^-_{rms} input-referred TRN is obtained with 1.6V reset voltage. The ×64 analog gain here is configured with ×16 amplifier gain and ×4 ramp voltage gain of the ADC. The noise-reduction trend first has a proportion of $1/g$ and then a proportion of $1/\sqrt{g}$, where g denotes the analog gain. This different trend indicates the dominant thermal noise sources in the readout chain, i.e. mainly the thermal noise from the ADC and external circuits connected at the back of the column amplifier, and then the thermal noise from the pixel source follower and the column amplifier.

Figure 22.3.4 shows a comparison of the CMS noise reduction for SSF and BSF pixels, respectively. For comparison, ×16 column amplifier gain is applied. Compared to the BSF pixels, the SSF pixels show the limited noise improvement from 4-times CMS because of *1/f* and RTS noise from in-pixel source follower. However, this limitation is avoided up to 8-times CMS in BSF pixels due to the buried-channel technique [6]. Comparing the input-referred TRN with only digital CDS (1-time CMS), the noise reduction of CMS is about 36% for SSF pixels while about 55% for BSF pixels where 8-times CMS is applied. Because of the limited configurable range and slope of V_{ramp}, 8-times CMS is the maximum available value with ×16 amplifier gain.

Figure 22.3.5 shows the input-referred TRN level under different configuration modes. While only digital CDS is applied, compared with the input-referred TRN at ×1 amplifier gain, the input-referred TRN is improved by 9.7 times for SSF pixels and by 10.7 times for BSF pixels after ×16 amplifier gain. Compared with the SSF pixels without analog gain and CMS technique, the BSF pixels with ×64 gain and 4-times CMS achieves a 40-times input-referred TRN reduction, which corresponds to a 32dB SNR enhancement in low-light-level conditions. It is also demonstrated that a high input-referred TRN reduction capability can be achieved without abundant CMS cycles [3,5], which simplifies the architecture and configuration of imagers.

Figure 22.3.6 shows a sample image taken by the chip at very low light condition of 0.06 lux at the focal plane in room temperature, with ×16 amplifier gain and 4-times CMS. During the measurement, an infrared cutoff filter (CM500S) and a green optical filter (VG9) are used. Fig. 22.3.7 shows the die microphotograph and main features.

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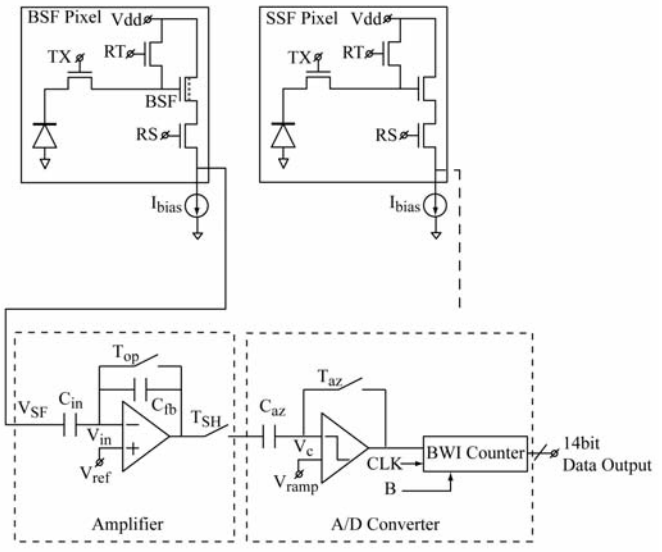

Figure 22.3.1: Schematic diagram of pixel and the column-readout circuits.

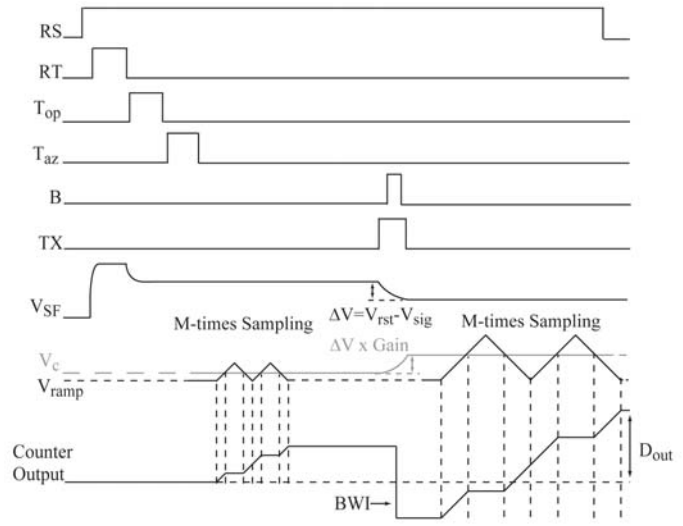

Figure 22.3.2: Sensor readout timing diagram.

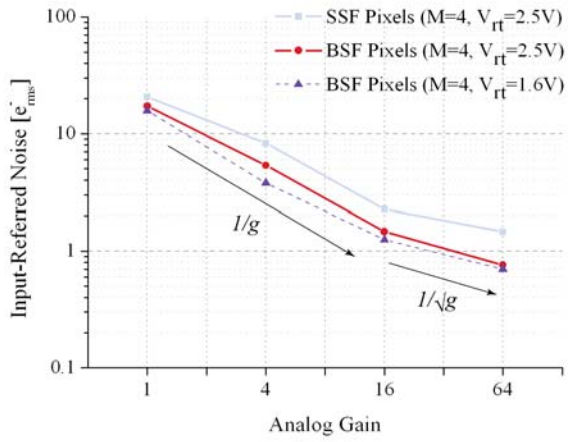

Figure 22.3.3: Measured noise of BSF and SSF pixels as a function of the analog gain.

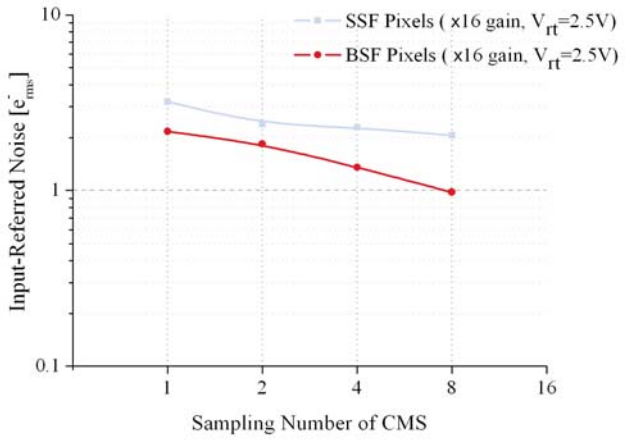

Figure 22.3.4: Measured noise of BSF and SSF pixels as a function of the sampling number of CMS.

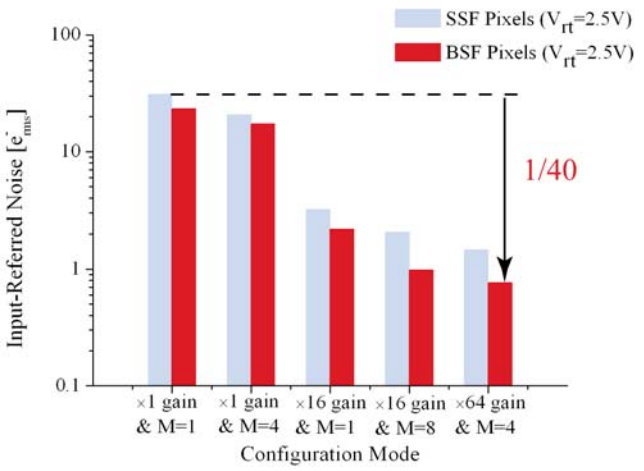

Figure 22.3.5: Measured noise under different sensor configuration modes.

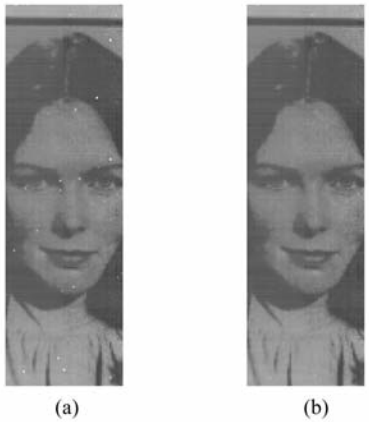

Figure 22.3.6: Sample image at 0.06 lux at the focal plane, F=4.0, ×16 gain and 4-times CMS, (a) raw image, (b) image after hot pixel removal.

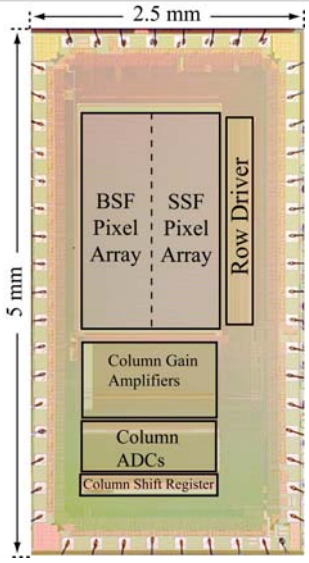

Figure 22.3.7: Die Photograph.

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