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## Column-Parallel Single Slope ADC with Digital Correlated Multiple Sampling for Low Noise CMOS Image Sensors

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### Abstract

This paper presents a low noise CMOS image sensor (CIS) using 10/12 bit configurable column-parallel single slope ADCs (SS-ADCs) and digital correlated multiple sampling (CMS). The sensor used is a conventional 4T active pixel with pinned-photodiode as detector. The test sensor has been fabricated in 0.18  $\mu\text{m}$  CMOS image sensor process from TSMC. The ADC nonlinearity measurement result shows totally 0.58% nonlinearity. Using the proposed column-parallel SS-ADC with digital CMS technique, 65% random noise reduction is obtained. The significant noise reduction enhances the sensor's SNR with 9 dB.

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*Keywords:* CMOS image sensor; column-parallel ADC; digital correlated multiple sampling;

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### 1. Introduction

CMOS image sensors for low light level imaging require a decent low noise performance. The most popular way to reach such a low noise level is using a preamplifier at the foremost stage of pixel readout chain with a high analog gain [1]. Another approach is using CMS technique to reduce the readout random noise [2]. However, both approaches need extra circuits in the column readout chain and increase the chip power consumption as well. Therefore, certain cost-effective readout chain circuits are necessary for low noise CISs. Column-parallel ADCs allow for low bandwidth readouts which eliminate the wide-

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band analog output buffer so that they enable CIS to gain low noise performance [3]. Moreover, a so-called digital CMS technique can be implemented with such column-parallel ADCs. In this paper, a low noise CIS using 10/12 bit configurable column-parallel SS-ADCs and digital CMS is presented.

## 2. Design and Operation

Fig. 1 shows the simplified schematic diagram of the 4T pixel with a pinned-photodiode and a column-parallel SS-ADC. The column SS-ADC consists of a comparator, driven by a ramp voltage  $V_{ramp}$  and a bit-wise inversion (BWI) counter [4]. This so-called BWI counters provide 32% reduction of power consumption and 2.4 times improvement of maximum speed over the conventional up/down counter [4].

Fig.2 shows the timing chart for the sensor operation with 4-times digital CMS process. Firstly, the reset signal resets the pixel sensing node causing the reset level output to appear at the pixel output. After pixel sensing node reset, the input and output of the comparators are connected by  $T_{az}$  to eliminate the offset of the comparators and the pixel outputs. The reset level is then compared with the ramp voltage  $V_{ramp}$  and the BWI counter is set to count up synchronously. Whenever the reset level is higher than  $V_{ramp}$ , the comparator output toggles from digital “high” to digital “low” and this stops the BWI counter from counting.  $V_{ramp}$  will be up and down ramping for 4-times to configure the 4-times sampling. After the signal charges are transferred and VSF goes down to the pixel signal level. During the charge transfer period, every bit of the BWI counter is inverted to perform 1’s complement operation by applying the control signal  $B_1$  and  $B_2$ . The BWI counter then set to up counting again from this negative ADC result for the pixel signal level sampling. The ramp voltage is configured as the same manner of 4-times pixel reset level sampling. Finally the counter will digitally subtract the conversion of the 4-times sampling of reset signal from the sensor signal, and then do the averaging of ADC output in digital domain.

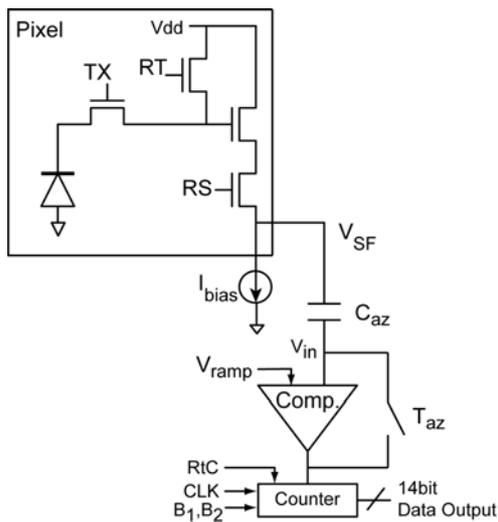


Fig. 1. Schematic diagram of pixel and the proposed column readout circuits

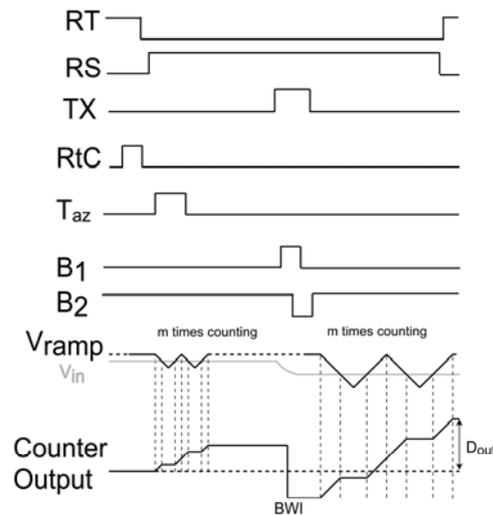


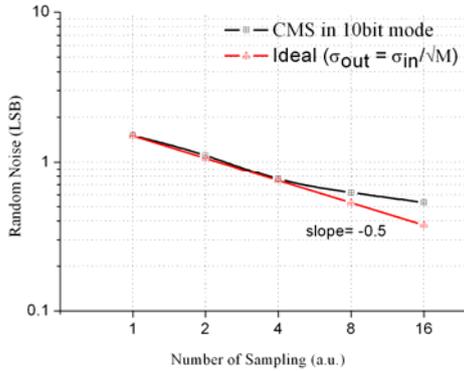
Fig. 2. Schematic diagram of pixel and the proposed column readout circuits

### 3. Measurement Results and Conclusion

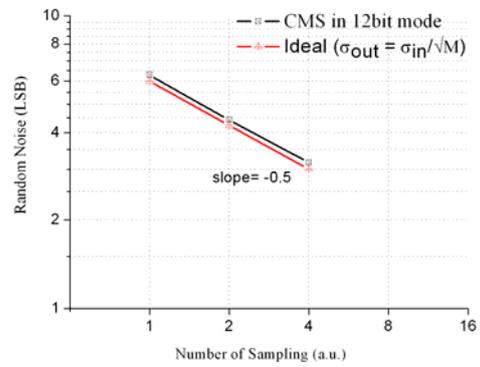
The specifications of the test sensor are summarized in Table II. Fig.3 (a)&(b) show the dark random noise measurement results in 10b and 12b ADC mode. A 120 MHz clock is supplied to the column ADC by an on-board PLL cell. Each pixel is read out in 65  $\mu$ s for 16-times CMS in 10b ADC mode, and in 62  $\mu$ s for 4-times CMS in 12b ADC mode. The dark random noise is reduced from 6.3 to 3.2 LSB, gaining 50% reduction in 12b ADC mode with 4-time CMS and from 1.5 to 0.53 LSB, gaining 65% in 10b ADC mode with 16-time CMS.

TABLE II

Specification	Value
Process	TSMC 0.18 $\mu$ m 1p4m CIS
Chip Size	2.34mm (H) $\times$ 1.46mm (V)
Pixel Type	4T APS with pinned-photodiode
Pixel Size	10 $\mu$ m (H) $\times$ 10 $\mu$ m (V)
Input Clock Rate	120 MHz
Power Supply	3.3V (A) / 1.8V (D)
Output	10/12 bit digital resolution
Digital CMS Mode	1, 2, 4, 8, 16 in 10bit resolution 1, 2, 4 in 12bit resolution



(a)



(b)

Fig. 3. Measured input referred dark random noise of the sensor in: (a) 10bit, and (b) 12bit ADC resolution mode

Fig. 4 (a) & (b) show the measured differential nonlinearity (DNL) and integral nonlinearity (INL) plot of the column-parallel SS-ADC. From the measured results, the worst DNL is within  $-0.8/+0.6$  LSB and INL is within  $-2.0/+4.0$  LSB, which corresponds to a 0.58% nonlinearity. As a conclusion, the column-parallel SS-ADC with digital CMS can effectively reduce the pixel readout random noise for low noise CMOS imagers.

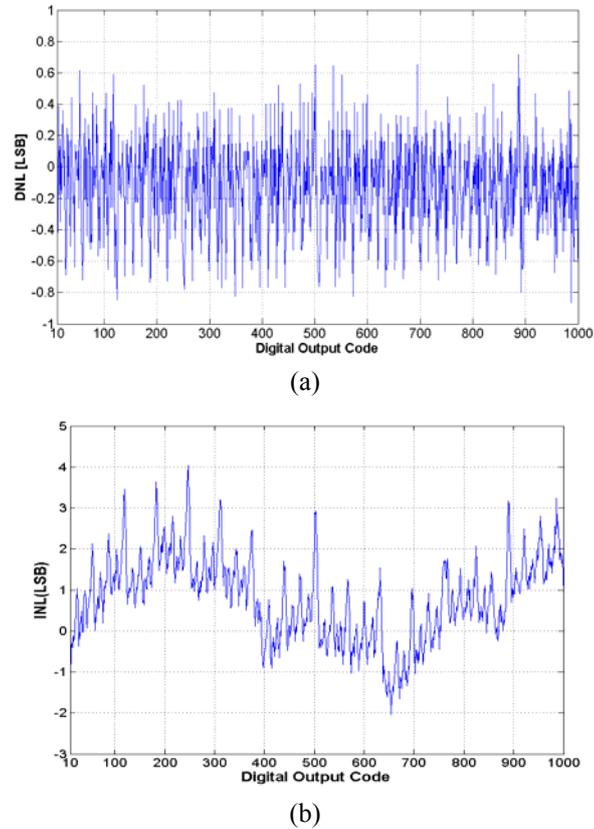


Fig. 4. Measured column ADC nonlinearity: (a) DNL and (b) INL in 10b resolution mode

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