High dynamic range hybrid pixel sensor

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A new readout imaging system with enhanced dynamic range (DR) and low power consumption is presented. The DR is enhanced by using feedback to control the integration time of the sensor. The feedback is implemented within an in-pixel-level ADC. The power consumption is reduced by switching the bias circuit off when it is not needed for the system, this readout circuit is used for a hybrid sensor: the photodiode and the readout circuits are placed in two different layers, the interconnections are made through bond pads.

Introduction: Dynamic range (DR) in image sensors is defined as the ratio of the largest to the smallest light levels that can be measured, in reality being the ratio between the saturation level and the noise floor of the imager. In [1], the DR of the sensor is enhanced by having several integration times within one frame period. One sample of the image is read out after each integration. Because several samples need to be read in one frame period, the power consumption increases with increase in DR.

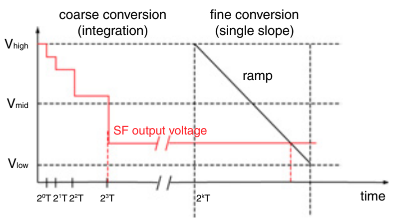

Fig. 1 *Conversion algorithm of proposed pixel-level ADC*

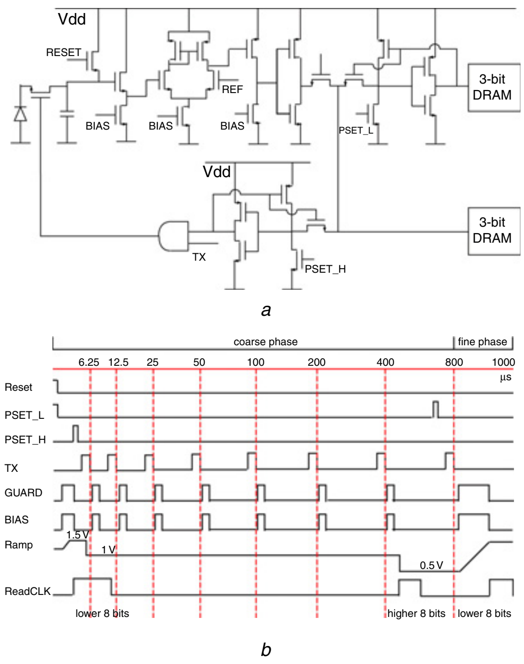

Fig. 2 *Schematic diagram, and timing of pixel ADC*

a Schematic diagram
b Timing

Local transfer gate control method: In this method described in this Letter, the integration time for each pixel depends on the incoming light intensity. The conversion algorithm is shown in Fig. 1. There are two phases: coarse conversion and fine conversion. The coarse conversion period is used to choose the integration time (MSBs). The fine conversion period converts the voltage after integration using a single slope ADC (LSBs). The reset level is converted and stored before the first charge transfer for digital correlated double sampling (CDS) and is not shown in the Figure. Let us define the maximum integration time as $2^k T$, with k being an integer larger than one. After a certain time interval T, the charge that has been integrated on the photodiode is transferred to the floating diffusion. After this transfer the voltage at the output of the source follower is compared to a reference voltage V_{mid}. If this voltage is below the reference level, no further charge transfers will happen and the voltage in the floating diffusion is held until the end of the integration time to be used in the fine conversion phase. Otherwise, another charge transfer happens at $2 \cdot T$ and a comparison is performed again. The process is repeated m times (with $0 \leq m < k$) until the maximum integration time ($2^k T$) is reached.

The schematic and timing of the pixel level ADC is shown in Fig. 2. The output of the source follower is connected to the input of a three-stage comparator. Latches are placed between the comparator and the memory cell in order to write the correct code. During the coarse conversion phase, the comparator and the source follower are only switched on during the reset signal conversion and during the comparisons happening after the charge transfers, in order to save power. The GUARD signal (see Fig. 2) is used to disconnect the output of the comparator from the latch, because while the comparator is switched off, its output is unpredictable. The signals PRE_L and PRE_H are used to initialise the latches [2]. The output of the latch and the global transfer gate control signal TX generate the pixel transfer gate control signal.

Simulation results: The sensor is specified for a frame rate of 1000 frames/second. The coarse conversion phase takes 800 µs, and the fine conversion phase takes 25.6 µs. The remaining time (174.4 µs) is used for the memory readout. The simulated SNR curve is shown in Fig. 3. The noise is dominated by the ADC quantisation noise, which is doubled because of the digital CDS. The peak SNR of the sensor is 38.91 dB. The DR of the sensor is enhanced from 43.05 to 85.29 dB with only 2.2% additional power consumption. The final specifications of the pixel are shown in Table 1. The pixel size does not contain the photodiode as it is placed in a different layer as mentioned before.

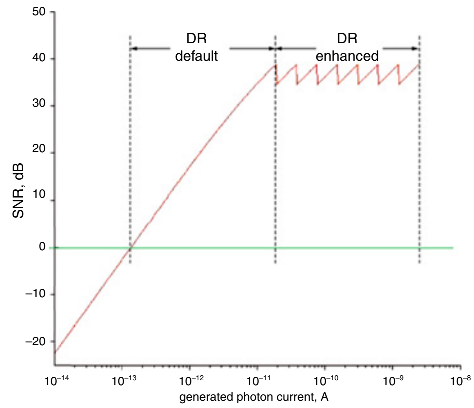

Fig. 3 *Simulated SNR curve of proposed ADC*

Table 1: Pixel specifications

Technology	0.18 µm
Pixel size (without photodiode)	18 µm × 18 µm
ADC resolution	8 bits
Frame rate	1000 frames/second
Supply voltage	1.8 V
Power consumption	63 nW/pixel
DR	85.29 dB
Peak SNR	38.91 dB

Conclusion: The proposed method enhances the DR of the sensor by generating local charge transfer control signal pulses based on the incoming light intensity. Because both the source follower and the comparator are switched off when they are not used, the DR can be enhanced by 7 bits with only 2.2% additional power consumption.

3 April 2011
doi: 10.1049/el.2011.0808
One or more of the Figures in this Letter are available in colour online.

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