In-Pixel Buried-Channel Source Follower in CMOS Image Sensors Exposed to X-Ray Radiation

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***Abstract*—This paper presents a CMOS image sensor (CIS) with pinned-photodiode 5T active pixels which use an in-pixel buried channel source follower (BSF) with an optimized row selector (RS). According to our previous work [1][2], using in-pixel BSFs with optimized RS can achieve significant pixel dark random noise reduction, i.e. 50% reduction, specially for random telegraph signal (RTS) noise, and an increase of the pixel output swing and dynamic range. With significant dark random noise reduction, in order to evaluate the performance for perspective space or medical imaging application, this proposed pixel structure using 0.18μm CMOS image sensor process is also further characterized under X-ray radiation. The results show that X-ray radiation induces additional acceptor-like interface traps which will increase dark random noise of the BSF pixels, to make BSF pixels less sensitive to radiation exposure, further optimization is necessary.**

I. INTRODUCTION

During the past few years, research has revealed that the random noise in CMOS imagers is mainly composed out of 1/f and the so-called Random Telegraph Signal (RTS) noise [3]. The dominant noise sources in CMOS image sensors (CIS) are due to the lattice defects at Si-SiO_2 interface of the in-pixel source follower (SF) transistor [4, 5]. As CMOS processes scale down, the gate area of the transistors becomes so small that it happens to have only one active interface trap underneath the transistor's gate, which will induce the RTS noise. Our previous work [1, 2] has revealed that taking the conducting carriers away from the Si-SiO_2 interface by creating a buried-channel nMOS SF transistor in a modern CMOS imager process can dramatically reduce the dark random noise within pixels, which will improve the image quality under low-light conditions [5]. Moreover, the output swing and dynamic range of the pixels is further improved by the buried-channel source follower (BSF) transistor together with an optimized row selector (RS). However, up to now, there is yet no research or characterization done on such BSF pixels with radiation test. As soon as such pixels are used for medical or outer-space applications, the performance of BSF pixels within radiation exposure circumstances will become a concern. Therefore, the pixel's noise characterization due to radiation are analyzed and discussed in this paper.

In section II, the working principle of buried-channel nMOS transistors is presented. In section III and IV, the results of the sensor characterization with the proposed pixels are discussed and analyzed. The initial noise characterization results due to X-ray radiation exposure are also presented in section IV. Finally, conclusions are drawn in section V.

II. TRANSISTOR WORKING PRINCIPLE

In principle, the buried-channel transistors stand for transistors of which the majority of their conducting carriers flow far beneath the gate Si-SiO_2 interface during operation. Actually in modern CMOS processes, the p-type MOS transistors are naturally buried channel devices because of the threshold voltage (V_t) adjust doping process during fabrication. Therefore, the expected structure of a buried-channel nMOS transistor is very straightforward, i.e. a total region reversing of a pMOS transistor, as shown in Fig. 1. The desired operation modes for such a device are shown in Fig. 2. Simulations are based on an "ideal" CMOS process, which means all parameters and process flow can be adjusted freely. The dashed lines stand for the boundaries of the depletion regions. As shown in Fig. 2, during switch off, the gate interface region is fully depleted and no current flows from the drain to the source. While during the linear operation, the two depletion regions are separated from each other, which allows current to flow. In the saturation region, the channel is pinched off near the drain side. Because of the buried-channel doping, the V_t of this nMOS transistor is shifted towards a negative value. This will help to increase the pixel output swing.

III. SENSOR DESIGN

The test sensor was fabricated in a 0.18 μm 1P4M CMOS image sensor process by TSMC. The chip micrograph with several fundamental functional blocks of the prototype chip is shown in Fig. 3. The pixel array is 200 rows × 150 columns with 10 μm pixel pitches. The pixels are implemented with pinned photodiode 4T structures with BSFs and optimized RSs. The schematic of the proposed pixel is shown in Fig. 4, in which a transmission gate is implemented as the row selector. The system clock frequency is 10MHz. The front-end read timing is supplied by an external FPGA. The outputs of

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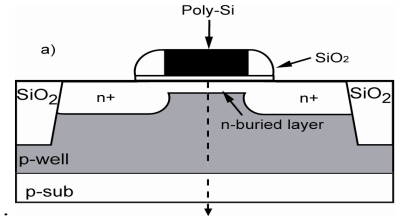

Figure 1. Cross section of a buried-channel nMOS transistor

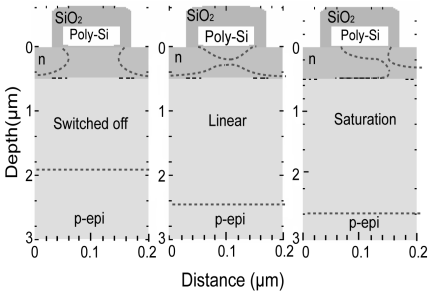

Figure 2. Expected operation modes of a buried-channel nMOS transistor

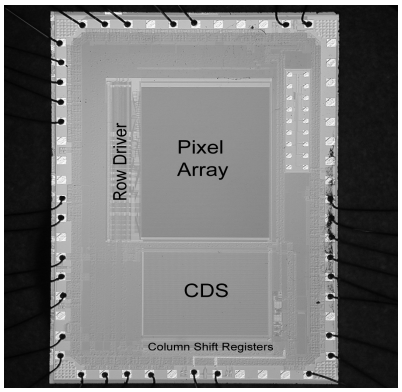

Figure 3. Chip micrograph of the test imager

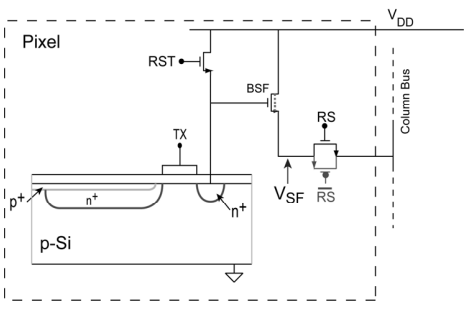

Figure 4. Schematic of pixels of the new test imager

the imager are analog signals, being converted into digital by an off-chip image processor with 12bit ADC. The test imager was successfully fabricated and tested. The measurement results are presented and discussed in the following section.

IV. Sensor Characterization Results

A. Pixel Output Swing

Fig. 5 shows the pixel output swing measurement results. During the measurement, the reset transistor (RST) gate is tied to the highest voltage of the pixel and the transfer gate is grounded. Therefore, the floating diffusion (FD) node voltage equals to the power supply minus one threshold voltage of RST transistor. The column bias current remains constant for all pixels.

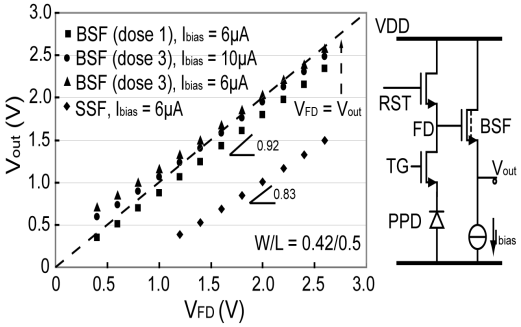

Figure 5. Pixel output swing measurement with different implantation doping and bias currents

As shown, the output swing of the BSF pixels is about 2 V, gaining almost 100% improvement compared that of surface-channel SF (SSF) pixels. If the bias current is reduced while the implantation dose remains the same, the pixel output further approaches or even exceeds the line of $V_{FD}=V_{out}$, which indicates that the channel is buried deeper into the silicon. If the bias current remains constant, increasing the implantation dose also pushes the channel deeper. The measured voltage gain of the source follower is improved from 0.83 of the surface-mode devices to about 0.92~0.95 of a buried-channel transistor. As a conclusion, both the pixel output swing and the source follower voltage gain are improved by using the BSF inside the pixel.

B. Quantum Efficiency

The quantum efficiency (QE) is measured with a monochromator in a 5nm bandwidth. The wavelength of the photons falling on the pixels is changed from 330nm to 1000 nm. The quantum efficiency is defined by the output signal of the pixel (expressed in electrons) over the photons impinging on the pixel.

Fig. 6 shows the QE measurement results of the pinned-photodiode in SSF and BSF with optimized RS pixels, respectively. For the results, the fill factor of pixels is not included. As shown in Fig. 4, the optimized RS contains a pMOS transistor which will introduce an n-well inside of pixel. During pixel configuration, this n-well will be always biased to a high voltage, i.e. power supply, which will make it as an additional photon-generated-electron sink during exposure, thus hurts QE of the pinned-photodiode, especially for longer wavelengths of light detection.

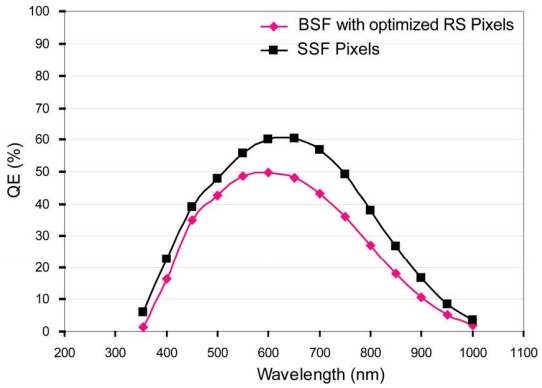

Figure 6. Quantum efficiency of pinned-photodiode in SSF and BSF with optimized RS pixels (without microlens)

C. *Signal-to-Noise Ratio (SNR)*

Fig. 7 shows the SNR measurement results for BSF with optimized RS pixels. The measurement is done by means of photon transfer curve (PTC) method [7]. The measurement is implemented with a DC current controlled monochrome light source. During the measurements, the light intensity is varied and the exposure time is kept constant, i.e. 200 line times (1 line time=0.3 ms). SNR of the target pixels reaches 41.6 dB at saturation.

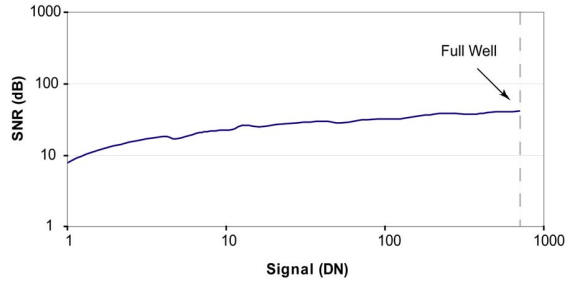

Figure 7. SNR measurement results for BSF with optimized RS Pixels

D. *Dark Random Noise*

The dark random noise of BSF and SSF pixels is measured. The sensors are also exposed to X-ray radiation with total ionizing dose of 31 krad and then 117 krad. During X-ray radiation, there is no bias source or power supply on the sensors. During the measurement, both the BSFs and SSFs are biased with 6 μA current, 3.3 V power supply and 3.3 V FD node voltage (V_{FD}=3.3 V). The random noise of each pixel is measured by calculating the standard deviation of pixel outputs through 20 frames. In order to exclude the contribution of the photon shot noise from the total noise floor, all the noise measurements are carried out in complete darkness. The transistor dimension for both BSFs and SSFs are W/L=0.42 μm/0.5 μm. The measurements were processed with an analog sensor gain of 10, at 17fps and with a 12bit board-level ADC. The conversion gain is 41 μV/e^-. The CDS interval is 1.5 μs with transfer gate (TX) transistor grounded.

Fig.8 shows the histogram of dark random noise of BSF pixels before and after X-ray radiation. During radiation, free electrons and holes are generated at Si-SiO_2 interface, the generated free electrons will then recombine with holes which will not play a significant role in the radiation effect on the devices, but, from equation (1), the generated holes will bombard onto Si-H bond to make it into a weak Si-Si bond, leaving a dangling bond (Si_{db}) behind [9] which will act as acceptor-like interface traps at Si-SiO_2 interface:

$$Si\text{-}H + Si\text{=}Si \leftrightarrow Si\text{-}H\text{-}Si + Si_{db} \quad (1)$$

Therefore, a certain number of additional acceptor-like interface traps will appear at the initially passivated Si-SiO_2 interface. On the other hand, for the BSF transistor, FD node reset voltage (SF transistor gate bias) has a strong influence on

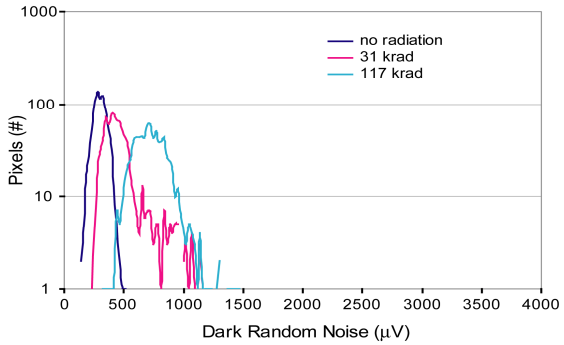

Figure 8. Histograms of dark random noise of BSF pixels before/after radiation

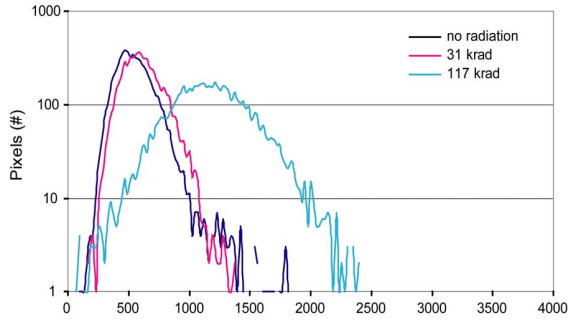

Figure 9. Histograms of dark random noise of SSF pixels before/after radiation

the potential distance and depletion region at the Si-SiO_2 interface. Increasing the gate bias will make the buried channel shallow, i.e. electrons will flow more closer to Si-SiO_2 interface, then have more chances to be caught by those interface traps [2]. Therefore, the dark random noise after X-ray radiation will increase. As shown in Fig. 8, the average dark random noise is increased from 270 μV_{rms} to 700 μV_{rms} with an increasing radiation dose.

Fig. 9 shows dark random noise of SSF pixels before and after X-ray radiation respectively. Although the radiation-induced positive charges increase dark random noise of both BSF and SSF pixels, the average dark random noise of the BSF pixels is still nearly 40% lower, compared to the SSF pixels, even after irradiated to 117 krad. The drastic increase of random noise spread due to X-ray radiation is also constrained in the case of BSF pixels.

Fig. 10 shows a comparison for the relative increase of dark random noise of SSF, BSF pixel with 3.3 V and 1.6 V FD node reset voltage before and after X-ray radiation, respectively. The relative increase is defined as the ratio of the radiation induced average random noise increase over the average random noise before X-ray radiation. Due to the initially passivated Si-SiO_2 interface and a buried channel, the dark average random noise will be brought down to very low levels, but the X-ray radiation introduced additional acceptor-like interface traps and the relative shallow buried channel caused by 3.3 V SF gate bias voltage (V_{FD}) will result in BSF pixels having a larger increase of random noise than the SSF pixels. Therefore, as shown in Fig. 10, BSF pixels have a higher relative increase of radiation induced random noise than SSF pixels. However, on contrary, with a low V_{FD}, e.g. 1.6 V, the buried channel is pushed deeper to force the electrons to move away from Si-SiO_2 interface during current flow underneath the gate. Therefore, X-ray radiation introduced additional acceptor-like interface traps will not cause a significant increase of dark random noise. This is also clearly shown in Fig. 10. However, in practice, a low FD voltage may introduce image lag because of the incomplete charge transfer and therefore is not recommended.

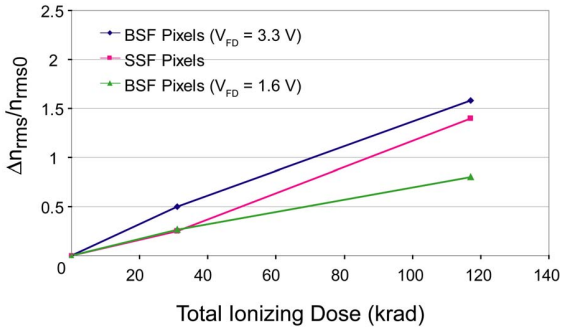

Figure 10. Relative increase of dark random noise of for SSF and BSF pixels before/after radiation

V. CONCLUSIONS

A CMOS image sensor with an in-pixel buried-channel source follower and an optimized RS is presented. The results show that, compared to a regular imager with the standard nMOS transistor SSF, the new pixel structure improves the output swing by almost 100%, but due to an extra n-well inside the pixel, the quantum efficiency of pinned-photodiode is attenuated, especially for long-wavelength light detection. The proposed pixels can reach 41.6 dB of SNR at full well. X-ray radiation exposure is applied to both proposed BSF and SSF pixels. X-ray radiation induces additional acceptor-like interface traps and an increase in dark random noise. But due to the buried-channel implantation, BSF pixels show a better random noise performance than SSF pixels, which is mainly dominated by RTS noise. However, the radiation induced influences on the performance of transistors is rather complicated, especially for buried-channel transistors. In order to understand the radiation influences on buried-channel components completely, more characterization together with simulation work is necessary.

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