A CMOS Image Sensor with Charge Domain Interlace Scan

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***Abstract*— This paper presents the first CMOS image sensor which implements a charge domain interlacing principle to improve the signal-to-noise ratio (SNR) under the same exposure condition (integration time and light intensity). A novel pixel is designed to fit the charge domain interlacing principle, which works in field integration and frame integration mode. This CMOS image sensor also contains a programmable universal image sensor peripheral circuit, thus this sensor can also be used in progressive scan. Comparing the performances of the sensor working in charge domain interlacing and in the progressive scan, the chip measurement results prove that under the same exposure condition, the light response of the charge domain interlacing is the twice that of the progressive scan. The SNR performance can be increased by 6 dB in low light level.**

I. INTRODUCTION

Over the past decade, fueled by the demands of multimedia applications, digital still and video cameras are rapidly becoming widespread. Image sensors being a key component in modern digital cameras convert the light intensity to electric signals. To evaluate the performance of the image sensor we should consider a lot of aspects and constraints. The SNR is one of the important parameters. Because CMOS image sensors in general have higher temporal noise, higher fixed pattern noise, higher dark current, and small full well charge capacitance compared with CCD image sensor, to improve the overall quality of the image, high SNR and high dynamic range are desired. Improving the SNR, the challenge can be stated as more signal with less noise. Going through the history of CMOS image sensor development we found that a lot progress of CMOS image sensors were aimed to achieve less noise to improve the SNR and dynamic range. Like the Active Pixel Sensor (APS) [1] technology, achieving a lower readout noise, improved scalability to large array formats. The pinned photodiode 4T pixel structure and Correlated Double Sampling (CDS) method together reduce the kTC noise and fixed pattern noise. All of these technologies improve the SNR by reducing the noise. On the other hand, the SNR can be further improved by enhancing the signal level under the same exposure condition (time and light intensity).

In this paper, we use a charge domain interlacing principle to increase the signal level. The interlace scan format was used due to its good compromise between spatial and temporal resolution as well as flicker reduction on one hand, and small bandwidth on the other hand. Interlace scan mechanism does not transmit the scan lines of a frame in their logical order. Instead, each frame is divided into the readout of two parts, an odd field and an even field. Basically two kinds of interlace scan readout modes are implemented, which are introduced in more detail in the following: frame integration mode and field integration mode.

Frame integration mode: during the first field, the odd lines (1,3,5,…) were scanned and output as line 1,3,5,… The second field consists of the even lines (2,4,6,…), and also output as even lines (2,4,6,…). The SNR and temporal resolution for a CMOS image sensor implementing this frame integration mode is the same as for the progressive scan. The advantage of the frame integration mode is the full spatial resolution defined by the pixel geometry and its easy implementation. Because the fact that its integration time is equal to the frame time, so it is called frame integration mode.

Field integration mode: in this mode, the two adjacent scanning lines are added together. In the odd field, the lines 1+2, 3+4, 5+6,… are output as the lines 1, 3, 5,… The lines 2+3, 4+5, 6+7,… are used to make the even field and output as the line 2, 4, 6,… The integration time is the field time which is half of the frame time.

The characteristics of the field integration mode can be concluded as follows: First, no field time lag is present [2]. Due to the shorter integration time for the field integration mode, the time delay between two images (called "field time lag") is much less than in the case of the frame integration mode. Secondly, it is reducing the flicker at vertical edges in the image since the field integration mode doubles the vertical aperture. Thirdly, the vertical

resolution of the field is lower than in the case of progressive scan and frame integration mode. And last but not least, it has a high sensitivity compared to the frame integration mode or progressive scan if the integration time is the same. Because the field integration mode combines two scanning lines together, this is equal to enlarge the pixel size two times and means better light sensitivity [3]. In this situation, the high temporal resolution of the field integration mode will be trade off with the high sensitivity advantage.

II. DESIGN AND OPERATION

A. Charge Domain Interlacing Principle

The easiest realization of interlaced readout is the addition of the pixel signal in the voltage or even in the digital domain. However, this comprises the summation of all noise sources from the whole sensor readout chain as well having a negative effect on the final signal to noise ratio.

Another realization of field integration mode interlace scan is the charge domain interlacing principle, which is based on the charge binning method. Since the signal is added already in the charge domain before readout, the total readout noise floor is not affected by the signal summation at all. Thus, under certain circumstances this method shows a higher SNR than the interlacing method in the digital domain,, which is mathematically proven in the following.

The equation (1)-(3) give the different SNR performance for the charge domain interlace scan, normal progressive scan, and digital domain interlace scan respectively.

$$\mathrm{SNR\_charge} = 20\log\left(\frac{2S}{\sqrt{N_r^2 + 2N_s^2}}\right) = 20\log\left(\frac{2S}{\sqrt{N_r^2 + 2S}}\right) \quad (1)$$

$$\mathrm{SNR\_progressive} = 20\log\left(\frac{S}{\sqrt{N_r^2 + N_s^2}}\right) = 20\log\left(\frac{S}{\sqrt{N_r^2 + S}}\right) \quad (2)$$

$$\mathrm{SNR\_digital} = 20\log\left(\frac{2S}{\sqrt{2N_r^2 + 2N_s^2}}\right) = 20\log\left(\frac{2S}{\sqrt{2N_r^2 + 2S}}\right) \quad (3)$$

$$\mathrm{SNR\_charge} / \mathrm{SNR\_progressive} = 20\log\left(2\sqrt{\frac{N_r^2 + S}{N_r^2 + 2S}}\right) \quad (4)$$

$$\mathrm{SNR\_charge} / \mathrm{SNR\_digital} = 20\log\left(\frac{\sqrt{2(N_r^2 + S)}}{\sqrt{N_r^2 + 2S}}\right) \quad (5)$$

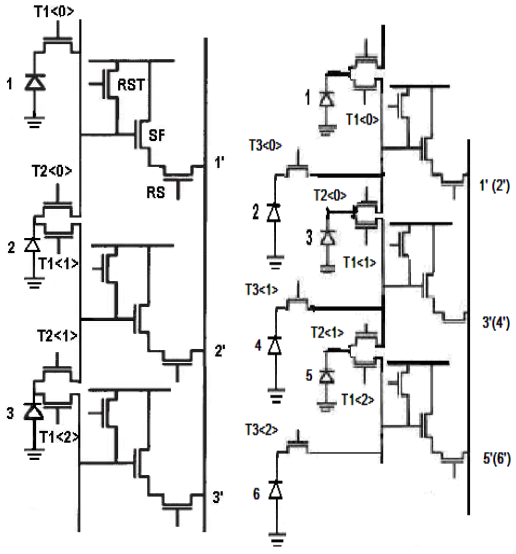
Where N_r is the input-referred noise coming from the readout circuit, and N_s is the photon shot noise of the signal, which has the square-root relationship with the signal S itself (N_s=sqrt(S)). All parameters are given in the number of electrons. From (4) we can derive that in the low light level ($N_r >> N_s$) the charge domain interlace scan gives a maximum 6dB improvement compared with progressive scan, in the photon shot noise dominate part ($N_r << N_s$), the improvement is 3dB. From (5), it can be found that, in low light level, the charge domain interlace can have 3dB advantage compared with digital domain interlace. In the photon shot noise dominate part, these two binning technologies will have the same performance.

To practically verify the charge binning interlace scan we proposed a pixel structure that allows for combining the collected charges of two pixels in the charge domain, and reading them out subsequently.

The binning technology in the charge domain is based on the idea of sharing the readout circuitry among pixels. In 2004, Matsushita [4] and Canon [5] both presented shared readout circuit pixels. The concept of sharing the readout circuit by 4 pixels is a time-division multiplex readout. These shared readout structure pixels were intended to produce small pixels with a high fill factor.

B. Pixel Structure

To implement the charge domain interlacing principle, this paper proposes a pixel structure (Fig.1 (a)) based on the pinned-photodiode (PD) 4T structure and inspired by the shared readout circuit pixel. The proposed pixel design perfectly and naturally matches the field integration mode in the charge domain which is equal to doubling the pixel size. In the field integration mode, each row will be scanned twice (both odd field and even field), not only the readout structure will be shared by two photodiodes (1, 2) placed in two rows, but also the individual photodiodes (2) will be connected and readout by two neighboring readout structures (1', 2'). In the odd field scan, charges accumulated in "1" and "2" are transferred to one common floating diffusion by turning on T1<0> and T2<0> at the same time. The corresponding output voltage 1' is the combination of the signal produced by "1" and "2". This



(a) (b)

Figure 1. Proposed two/three PDs shared pixel structures

structure also can be used in the progressive scan without the sensitivity benefit. The advantage of this structure is that the two signals (eg: signal produced by photodiodes in Row 1 and Row 2) are combined in the charge domain at the front-end and not in the voltage domain or digital domain like traditional interlace scan in CMOS imagers. And these two fields of the interlace scan perfectly fit and have an offset for one row.

This proposed two-PDs shared pixel structure adds one more transfer gate per pixel which achieves 5 transistors per pixel (photodiode), so the fill factor is lower than the classical 4T pixel. Compared with the three-PDs shared pixel structure in Fig1 (b) [6], the two-PDs shared pixel structure is more symmetric, easily implement, and has a smaller floating diffusion (FD) capacitance and consequently a bigger conversion gain.

C. *Image Sensor Implementation*

Fig. 2 shows the complete architecture of the sensor, which contains the pixel array, the current source array, the column multiplexer, the CDS circuitry, the row/column driver array, the programmable pulse generator, a Gray code counter and the output buffer.

The pixel array contains two types of pixel designs. From row 0 to row 62, there is the two-PDs shared amplifier pixel structure. The pitch of this structure is 10um $\times$10um. The fill factor is 46.4%. From row 63 to row 124, there is the three-PDs shared amplifier pixel structure. This structure contains one more PD and one more transfer gate. And one readout structure can be used in two neighboring row both in odd and even field. Because this structure is hard to layout completely symmetric, so when it used in progressive scan, the neighboring row have the different light sensitivity, then you can see some stripes on the image.

Because the proposed two photodiodes shared pixel structure is used in interlacing design, the PD will be shared by different readout circuits and charges stored in the PD will be transferred in two different directions. Thus,

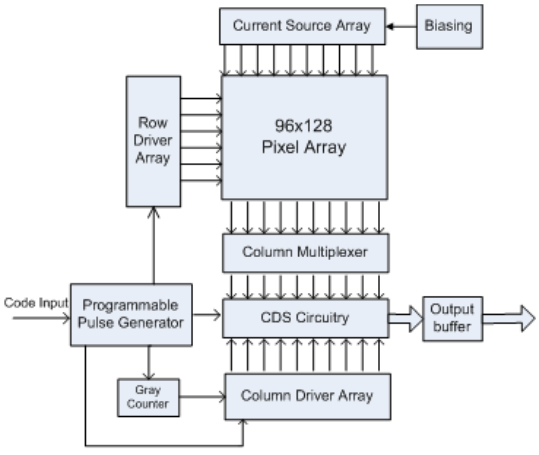


Figure 2. Architecture of charge domain interlacing CMOS

the readout circuit should be fully symmetric with respect to the readout structure of the pixel. Another aspect about the layout design is to control the capacitance of floating diffusion to optimize the conversion gain. The capacitance of the floating diffusion should not be too large. In this project, the floating diffusion of two/three photodiodes connected together for one readout circuit, which will be larger than normal design. In this situation, the layout should try to control the area of the floating diffusion to improve the conversion gain.

To test this pixel design and the working principle of the interlacing technology, a programmable universal image sensor driving circuit was proposed, which can drive and readout the pixel array flexible, efficient, and easily changes the working mode through a different programming. This sensor can not only support progressive scan, frame integration interlace scan mode, field integration interlace scan in voltage domain, but also can realize the charge domain interlacing principle. This is a unique feature of this CMOS image sensor, and without the shared pixel concept, charge domain interlacing was only possible with CCDs.

The test sensor was fabricated in a 0.18-um 1P4M CMOS process by TSMC. The outputs of the image sensor are analog signals, being converted into digital signal by an off-chip 12 bit ADC.

III. MEASUREMENT RESULTS

First, we compare the noise performance of the charge domain interlace scan with progressive scan. In the sensor signal-variance analysis of Fig.3, the plots for the two PDs shared pixel structure in progressive scan and interlace scan coincide with each other. It is the same situation for the three-PDs shared pixel structure. Thus, the two-PDs shared pixel structure has the same conversion gain (slope) of 0.0146DN/e^- in both scan modes. The three-PDs shared pixel has a smaller conversion gain of 0.0094DN/e- due to its larger FD capacitance.

Secondly, to prove the higher light sensitivity of the charge domain interlace scan, Fig.4 compares the light response of the charge domain interlace scan with the progressive scan based on the two-PDs shared pixel structure. Under the same light level conditions, the light response of the charge domain interlace scan is 15.9DN/ms (1089e-/ms) which is nearly twice the value of the progressive scan (8.01DN/ms, 548 e-/ms). This means with the same light level input and integration time, the average signal level of the interlace scan is twice the value of the progressive scan.

Thirdly, we can also compare the charge domain interlace scan with progressive scan in the SNR aspects. In Fig. 5(also based on the two-PDs shared pixel structure), under the same optical input level, in the relative low light level conditions [0…100e^-/um^2], field integration mode interlace scan will improve the SNR by 5~6dB compared with progressive scan. In this case, the readout noise is the main noise source. When the photon shot noise dominates the noise sources, the interlace scan can have about 3~4dB

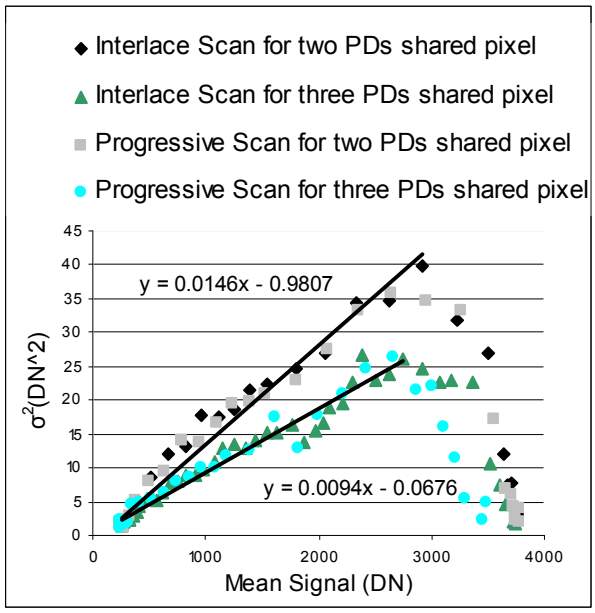


Figure 3. Noise performance of two pixel structures
(DN: digital number; σ^2: variance; σ: noise)

SNR improvement compared with progressive scan. This result confirms the expectation and the analysis of the field integration interlace design.

On the other hand, the original data of the progressive scan can be processed as well to achieve the field integration interlace scan in digital domain. In Fig. 5, the SNR performances of both the charge domain and digital

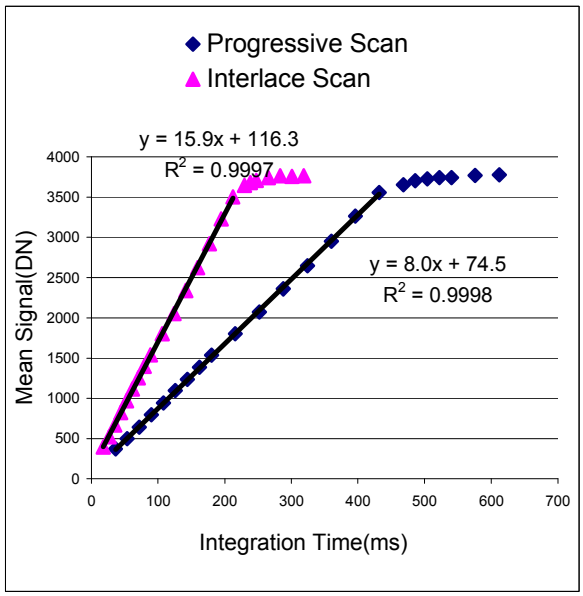


Figure 4. Light response of progressive scan and interlace scan

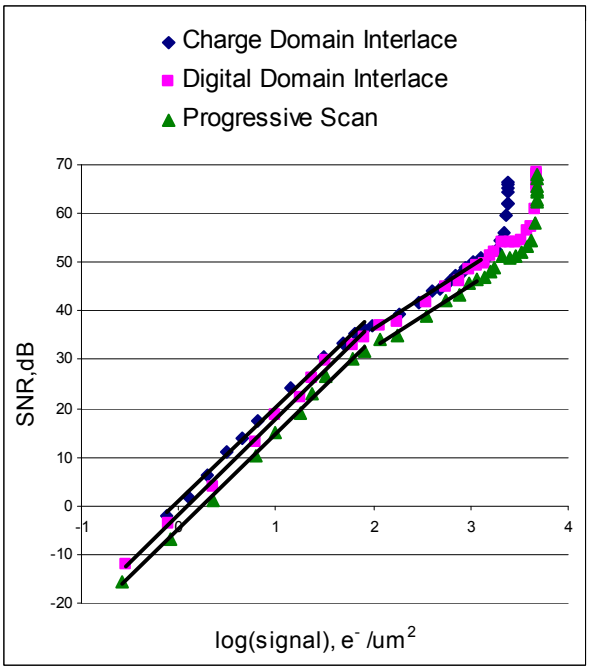
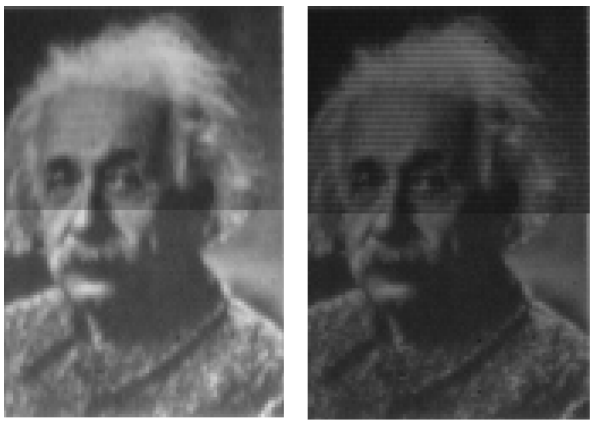


Figure 5. SNR for two PDs shared pixel interlace scan

domain interlace scan are also compared. Under the low light level conditions, the charge domain interlacing improves the SNR by 2.7dB compared to the digital domain interlacing. With the signal increasing, the SNR is the same for both interlacing methods. Those observations confirm the theoretical studies from the section above.

Finally, two images of the progressive scan and the charge domain interlace scan under the same exposure conditions are shown in Fig 6. The improvement of light sensitivity is clearly visible.



(a) Charge Domain Interlace Scan (b) Progressive Scan

Figure 6. Reproduced images from a 82×124 pixel array

(Upper half is three PDs shared pixel array;
lower half is two PDs shared pixel array)

In summary, the measurement results prove that the proposed charge domain interlacing CMOS image sensor can enhance the light sensitivity of the sensor and indeed improve the SNR under the same exposure condition.

IV. CONCLUSION

The first CMOS image sensor implementing the charge domain interlacing principle has been presented. Compared with the normal progressive scan, the SNR can be improved by enhancing the signal level under the same exposure conditions. A new pixel structure based on the shared amplifier pixel structure was proposed to fit the charge domain interlacing principle. This structure can naturally match the field integration interlace scan in the charge domain, and it makes the two fields of the interlace scan can perfectly fit and have a spatial offset of one row. The measurement results prove that under the same exposure time conditions the charge domain interlace scan can achieve two times the signal value of the progressive scan, which gives an SNR improvement of maximum 6dB under low light conditions.

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