Radiation Effects on CMOS Image Sensors due to X-Rays

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This work presents a study on X-Ray radiation induced degradation mechanism on both CMOS Image Sensors (CIS) with 4-Transistor (4T) pixels and its elementary test structures. The major degradation shows an increase of dark random noise and leakage current for both the sensor and the test structures. Moreover, the quantum efficiency of the pinned-photodiode (PPD) shows a post-irradiation variation at the short wavelength region. It is found that the Si-SiO$_2$ interface trap generation and charge trapping in the shallow trench isolation oxide are the main failure mechanisms.

1. Introduction

Nowadays, CMOS image sensors are getting popular to be used for the medical/space application thanks to their advantage of low power, low cost and high integration capability compared with CCD sensors. However, the radiation tolerance then becomes a great concern since the sensors will be degraded by the radiation environment during the application. Based on a wide study about the radiation performance of 3-Transistor Active Pixel Sensors (3T APS), it was found that oxide trapped charges will induce a total dose effect on the dark current increase[1]. However, very few papers have been published on the radiation effects on 4T APS and its in-pixel elementary devices so far. Since the 4T APS has different pixel architectures and a different device fabrication process compared with the 3T ones due to the pinned-photodiode, the transfer gate (TG) and the reset transistor, the previous knowledge about the radiation effect on 3T APS cannot be directly applied to 4T pixels[2]. This work aims to get an initial insight of the X-Ray radiation induced degradation mechanism of a 4T APS sensor and its test structures fabricated in a commercially available 0.18 μm technology.

2. Radiation Degradation of CMOS Image Sensors and Elementary Test Structures

In order to characterize the post-irradiation performance of a 4T APS CIS due to X-Rays, some elementary in-pixel test structures and an image sensor are designed and fabricated. These devices were irradiated by an X-ray source at Philips Health Care at room temperature with a total ionizing dose (TID) level of 31krad, 86krad, 106krad, 109krad and 137krad after 3-turn radiation, with an average energy of 46.2keV. Meanwhile, some simulations have been implemented as well in order to get some supplementary insights into the device performance.

2.1 Test Structures and its Simulation

In the test structures several single MOSFETs with different implants, sizes and gate-shapes are designed to be compared with each other. Moreover, several in-pixel devices consisting of pinned-photodiodes and transfer-gate transistors are also included. Fig.1 (a) shows the schematic of a 4T APS pixel, which consists of a PPD, a TG transistor, a reset

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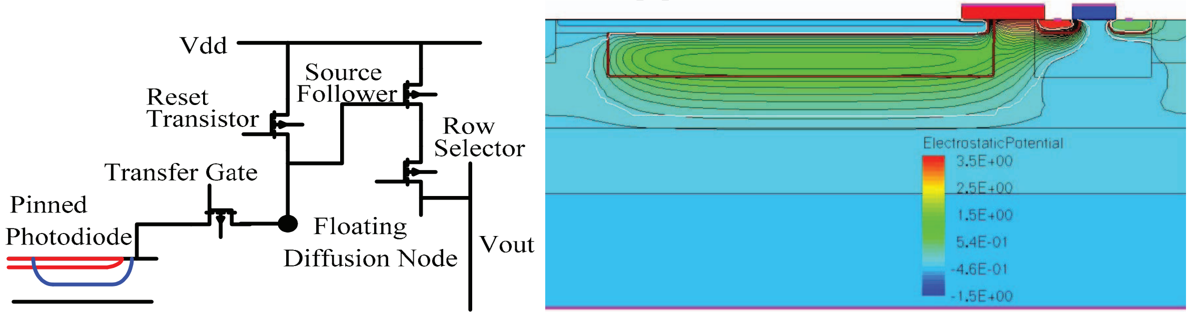
transistor and a source follower, while Fig.1 (b) demonstrates a cross section of a PPD, a TG transistor and a reset transistor from the simulator[3].



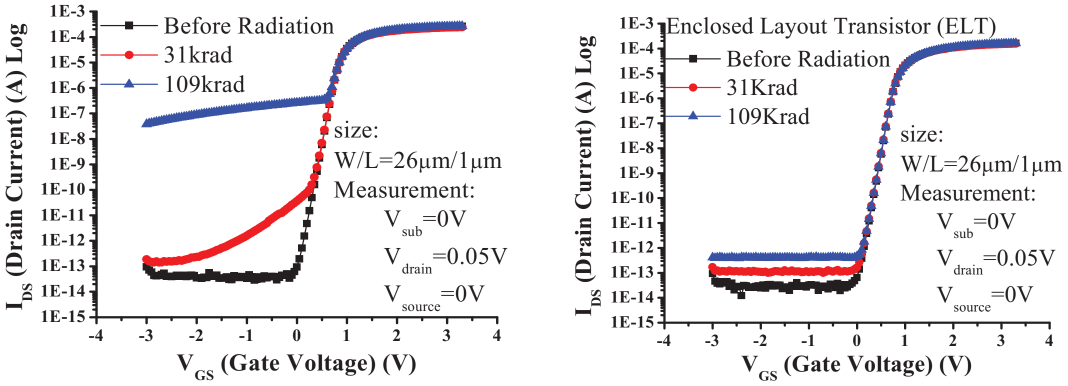
(a) (b)

Figure.1 A 4T APS pixel architecture (a) the schematic, (b) the simulated cross section

The transfer-gate transistor takes the pinned photodiode as its source region and is overlapping with the pinning layer of the PPD[2]. It can be seen in Fig. 1 (b) that there is a high electric field distribution in that overlapping region. Together with the gate oxide layer, these kinds of high electric field regions inside the pixel will be very sensitive to the radiation degradation.

2.2 Degradation of MOSFETs

Since the MOSFETs are the elementary devices inside the pixel, it is always necessary to assess their post-irradiation performance to study the basic degradation mechanism within the pixel.



(a) (b)

Figure. 2 N-type MOSFET characteristic after different radiation doses (a) standard layout transistor, (b) enclosed layout transistor

Fig.2 (a) shows the ionizing radiation effects on a transistor with a standard layout. It shows only a large drain leakage current increase, while the threshold voltage (V_{th}) does not shift due to the thin gate oxide thickness of this technology node. The shallow trench isolation oxide used to isolate the devices in this technology node can trap some holes generated from radiation. Due to these trapped charges, a lateral leakage path forms between the transistor's source and drain nodes by a parasitic field oxide transistor[4], which is the reason for a large increase of drain leakage current in Fig.2 (a). Compared with Fig.2 (a), the result from an enclosed layout transistor in Fig.2 (b) shows a much lower drain leakage current increase and meanwhile there is neither a shift of V_{th}. That is because the enclosed layout transistor (ELT) has an edgeless drain/source node which can suppress the parasitic transistor formation. Therefore the drain leakage current increase is much lower compared to the standard layout after a certain radiation dose level[4]. But there is still a tiny post-irradiation drain leakage current increase of the ELT transistor, which can be originated from some interface trap generation at the $Si\text{-}SiO_2$ interface. These donor-like interface traps are mostly located in the lower half of the band gap, which mainly make the drain leakage current up while it has no effect on the sub-threshold slope and threshold voltage shift[5].

2.3 Post-irradiation Dark Random Noise Degradation of CMOS Image Sensors

The device noise performance will be closely correlated with the interface trap generation. Therefore, the dark random noise of the CIS is measured before and after radiation by taking an average of the pixel output of several continuous frames. The sample is irradiated up to 31krad and 109krad. In the meanwhile, the transfer gate transistor is turned off in order to exclude the noise source from the PPD and the TG transistor.

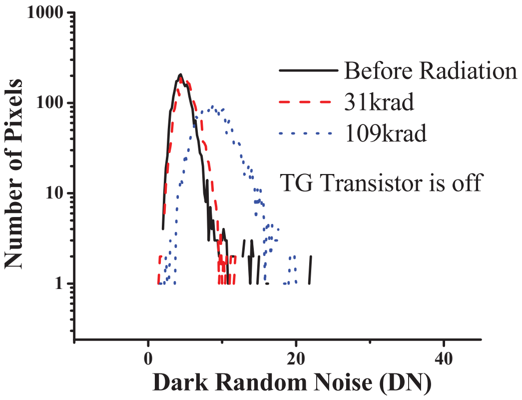


Figure. 3 Dark random noise histogram of a 4T APS CIS before and after radiation

As seen in Fig. 3, after the radiation the sensor presents a right shift of the dark random noise histogram with a larger digital number (DN) and meanwhile the width or the distribution of the histogram is getting wider. During the radiation, the passivated $Si\text{-}SiO_2$ surface beneath the transistor gate oxide is damaged and is generating some interface traps again after the incidence of the X-Rays, which will leave some holes transporting in the gate oxide to the $Si\text{-}SiO_2$ interface. Taking the noise histogram after 109krad radiation in Fig.3 as an example, a larger tail is present, compared to the original one. This presents a higher random telegraph signal noise due to the increasing number of interface traps[6]. Therefore, it can be concluded that the post-irradiation noise performance of the sensor is becoming worse due to the interface trap generation induced by the X-Ray radiation. Since during the measurement, the TG transistor is off, the noise performance shown in Fig. 3 mainly comes from the reset transistor and the source follower. Thus, it confirms that the X-Ray radiation does increase the interface trap generation of the elementary MOSFETs inside the pixel.

2.4 Quantum Efficiency Variation due to Radiation

The quantum efficiency is defined as the pixel output signal (expressed in electrons) over input photons on a pixel. It is measured before and after radiation for the dose level of 86krad and 106krad. As shown in Fig. 4, there is no significant degradation of the quantum efficiency for most of the wavelengths after the radiation, while there is a small reduction at the short wavelength region between 400nm and 550nm.

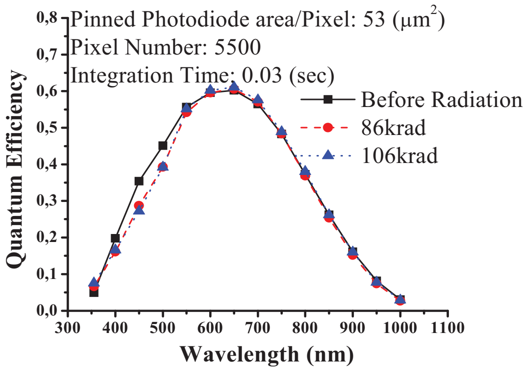


Figure 4. Quantum efficiency of a pinned photodiode of 4T CIS

The pinned-photodiode has a shallow p^+ pinning layer used to reduce the generation of dark current. But the passivated interface states will be damaged after the radiation. Then, some generated interface traps can attenuate the sensor's output and reduce the quantum efficiency as shown in Fig. 4.

3. Conclusion

Radiation effects on 4T APS are evaluated based on the measurements implemented on elementary MOSFETs in the pixel and complete CMOS image sensors. STI charge trapping induces a parasitic leakage path formation inside the MOSFETs and between devices, which raises the post-irradiation leakage current. Furthermore, the interface trap generation after X-Ray radiation can also increase the leakage current of a MOSFET. The shift of the dark random noise histogram and the reduction of quantum efficiency at the short wavelength region measured from a sensor confirm the radiation-induced interface trap generation.

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