A CMOS Image Sensor With In-Pixel Buried-Channel Source Follower and Optimized Row Selector

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***Abstract*—This paper presents a CMOS imager sensor with pinned-photodiode 4T active pixels which use in-pixel buried-channel source followers (SFs) and optimized row selectors. The test sensor has been fabricated in a 0.18-μm CMOS process. The sensor characterization was carried out successfully, and the results show that, compared with a regular imager with the standard nMOS transistor surface-mode SF, the new pixel structure reduces dark random noise by 50% and improves the output swing by almost 100% without any conflicts to the signal readout operation of the pixels. Furthermore, the new pixel structure is able to drastically minimize in-pixel random-telegraph-signal noise.**

***Index Terms*—Buried-channel source follower (BSF), CMOS image sensor (CIS), optimized row selector, random-telegraph-signal (RTS) noise, 4T-active-pixel sensor.**

I. Introduction

RECENTLY, a lot of efforts have been made on reducing the random noise in CMOS imagers, which is mainly composed of the $1/f$ and the so-called random-telegraph-signal (RTS) noises [1]. Research has revealed that the dominated random noise sources in CMOS image sensors (CISs) are due to the lattice defects at the Si-SiO_2 interface of the in-pixel source follower (SF) transistor [2], [3]. However, the exact mechanism of the RTS and the $1/f$ noises is still not completely clear [4], and the use of correlated double sampling (CDS) cannot fully eliminate $1/f$ and RTS noises [5], [6]. Therefore, reducing these noises becomes very difficult. Moreover, as CMOS processes scale down, the gate area of the transistors becomes so small that it easily happens to have only one active interface trap underneath the transistor's gate, which will induce the RTS noise. Because of this single-electron trapping and detrapping during the transistor operation, the RTS appears in pixels which have only one active interface defect and dominates the pixel temporal noise, and RTS noise limits the imaging quality under low-light conditions [6], [7]. Therefore, as long as a perfect clean gate interface cannot be guaranteed, the $1/f$ or RTS noise will stay dominant in the random noise in pixels.

It has been proved that it is difficult to reduce these noises using circuit techniques [8]. Therefore, the effective techniques are mainly the improvements of the processing technology. On the other hand, reducing the gate-oxide thickness should improve the gate control over the channel region, and the converse is also true. However, because the image-sensor process flow has constraints on reducing the gate-oxide thickness, e.g., increase of dark current due to gate-induced drain leakage, RTS cannot be reduced beyond a certain point for a given trap density. One common method is to adjust the annealing process in order to optimize the gate-oxide properties [1], [9]. However, such an approach is very process dependent and needs precise control on annealing temperatures and time. Furthermore, from the noise point of view, simply reducing the amount of Si-SiO_2 interface traps through annealing optimization may not help too much since a single interface defect can already introduce RTS noise as high as millivolts [10]. Consequently, the reduction of the interface-defect-induced noise by improving the annealing process will become less significant.

In order to deal with the imperfection Si-SiO_2 interface-introduced random noise, an alternative approach can be used, i.e., taking the conducting carriers away from the Si-SiO_2 interface by creating a buried-channel nMOS transistor (nMOST) in a modern CMOS imager process. In this paper, an in-pixel SF based on a buried-channel nMOST is introduced. The buried channel requires only one extra implantation, which pushes the highest potential in the channel away from the Si-SiO_2 interface. Thus, the possibility of carriers being trapped by lattice defects can be minimized, and the $1/f$ and RTS noises can be reduced. As a result, the random noise level of the imager can be significantly reduced. Furthermore, because the buried-channel transistor has a negative threshold voltage, the output swing of the pixels can be drastically improved by the buried-channel SF (BSF) transistor together with an optimized row selector. This means that "digital" transistors with reduced power-supply voltages can be used in the pixel without limiting the pixel's output swing, saturation level, and dynamic range.

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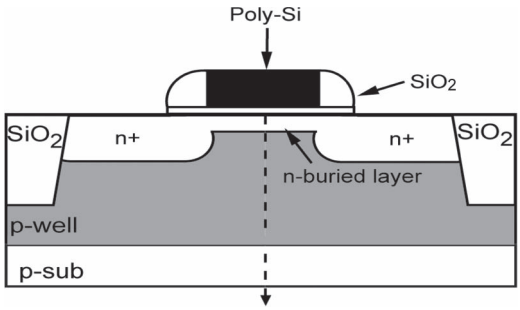

Fig. 1. Cross section of a buried-channel nMOST.

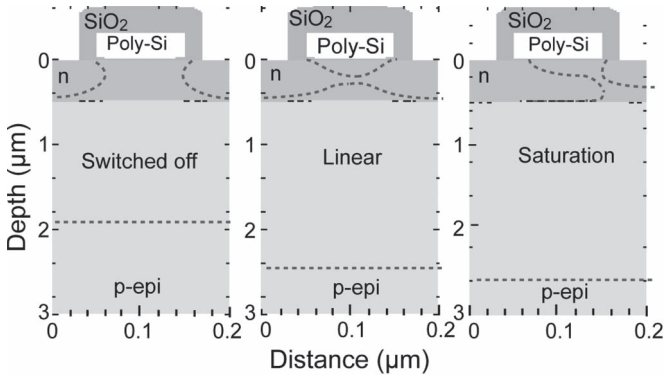

Fig. 2. Expected operation modes of a buried-channel nMOST.

II. Working Principle of Buried-Channel nMOST

In principle, the buried-channel transistors stand for transistors of which the majority of their conducting carriers flow far beneath the gate Si-SiO_2 interface during operation. In a modern CMOS process that uses a single-gate poly process, the p-type MOS transistors are naturally buried-channel devices because of the compensation threshold voltage (V_t) adjust implantation process during fabrication. Therefore, the expected structure of a buried-channel nMOST is very straightforward, i.e., a total region reversing of a pMOS transistor, as shown in Fig. 1. The desired operation modes for such a device are shown in Fig. 2. It was simulated from an "ideal" CMOS process, which means that all parameters and process flows can be adjusted freely. The dashed lines stand for the boundaries of the depletion regions. As shown in Fig. 2, during switch OFF, the gate interface region is fully depleted, and no current flows from the drain to the source. While during the linear operation, the two depletion regions are separated from each other, which allows current to flow. In the saturation region, the channel is pinched off near the drain side.

Because of the buried-channel doping, the V_t of this nMOST is shifted toward a negative value. This will help to increase the pixel output swing, which will be discussed in detail with measurement results later.

III. Device Simulations

The device simulations were done with MEDICI, and the device structure, material, and doping information was generated by the process simulator TSUPREM. The original simulation files were supplied by TSMC, which described the standard fabrication steps of an in-pixel SF transistor in a 0.18-μm CMOS process.

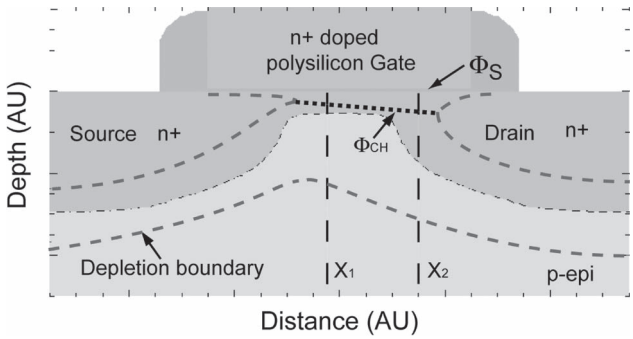

Fig. 3. Cross section of simulated BSF under SF operation bias condition.

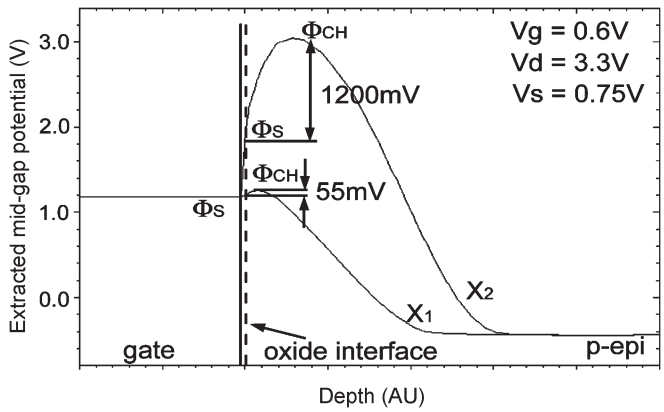

Fig. 4. Middle-gap potential curve extracted along the different locations of the gate length.

A. Potential Distance Simulations

According to [11], to avoid the interaction between the carriers and the gate Si-SiO_2 interface traps, the "potential distance" between the channel and gate Si-SiO_2 interface needs to be greater than kT/q (-25.8 mV at room temperature), which is also expected in the buried-channel nMOS SF. The simulated device cross section with the SF bias conditions is shown in Fig. 3. The boundary of the depletion region is shown as well as the location of $\Phi_{\rm CH}$ which means the potential distance between the highest channel potential along the gate length. In this case, the implantation was simulated with phosphorus doping, with a total dose of 6.5×10^{12} atoms/cm^2, and implantation energy of 70 keV, bias current density of 12 μA/μm. It is important to note that the $\Phi_{\rm CH}$ dashed line along the gate is a slanting line instead of a horizontal one. It can be seen that the difference of $\Phi_{\rm CH}$ at the various locations along the channel is rather significant, which means that the trap-related noise-reduction efficiency will highly depend on the trap location along the gate length. From the middle gap potential curves extracted along X_1 and X_2, shown in Fig. 4, it can be seen that, although both the potential distances between the channel potential $\Phi_{\rm CH}$ and the gate interface potential Φ_S at X_1 and X_2 are greater than kT/q (25.8 mV), the channel may turn back to surface mode near the source.

TABLE I
SIMULATED CHANNEL DEPTH OF DIFFERENT DOPINGS

Implantation Energy(keV) /Dose(atom/cm^2)	Channel depth(nm) (Vgate = 2.6 V)	Channel depth(nm) (Vgate = 1.6 V)	Channel depth(nm) (Vgate = 0.6 V)
70/7.5 x 10^{12} (P)	20	30	40
80/7.5 x 10^{12} (P)	20	30	40
90/8.5 x 10^{12} (P)	25	40	55
100/9.0 x 10^{12} (P)	25	40	60

B. Channel-Depth Simulations

Aside from the potential distance, the channel depth, i.e., the actual physical distance between the channel (the maximum potential) and the gate Si-SiO_2 interface, was also investigated by simulations. The channel depths of four different doping solutions as a function of the gate bias are shown in Table I. The implantation was still simulated with phosphorus doping, and the source/drain regions are both with a standard shallow n^+ implant. As shown, the maximum channel buried depth is determined by the doping energy and dose. Comparing with the channel depth of a buried-channel CCD [11], i.e., $\sim 0.8\ \mu$m, the channel depth is, in fact, shallow, such that, in saturation condition, it is possible that the device turns into partly surface mode. This condition is believed mainly due to the extremely thin gate oxide in modern CMOS technology, which is actually a fundamental technology limitation.

Although the channel depth cannot be optimized the same as the condition in a buried-channel CCD, the simulation results of the potential distance can already provide very important evidence that buried-channel devices can be made by means of the current CMOS process technology and that the buried condition can be achieved as well. The "buried" concept and feasibility of creating such devices in a modern CMOS process are also proved by means of the simulations. Test structures were then developed based on the TSMC 0.18-μm CMOS process with different buried-channel implant-energy and dose combinations.

C. Test Transistor Characterization

The comparison of the simulated and measured gate characteristics of the surface- and buried-channel transistors is shown in Fig. 5. These buried-channel devices were made through different total doses but with the same implantation energy. The transistor size is the same.

It can be seen that, as expected, increasing the implantation dose will shift the transistor threshold voltage toward a more negative value. The simulated and measured I–V curves of the standard surface-channel device match very well. Increasing the implantation dose will lower the V_t of the transistors. The V_t extracted from the measurement is slightly higher than the simulated one. Such difference becomes larger with higher implantation dose.

As shown in Fig. 5, under the same gate bias condition, the slope of the I–V curve, i.e., the transconductance (g_m), increases with increasing the implantation dose. For the SF application in CMOS imagers, the transistors operate under very small biasing current in order to maintain a weak inversion operation; therefore, it is important to compare the g_m's at the

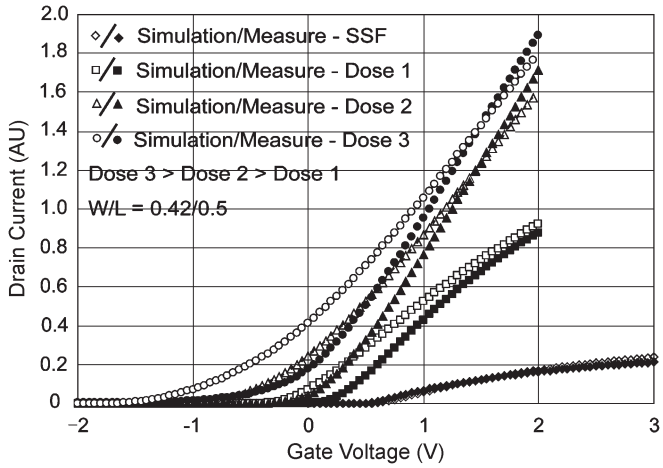

Fig. 5. Simulated and measured gate characteristic of transistors with different implantations.

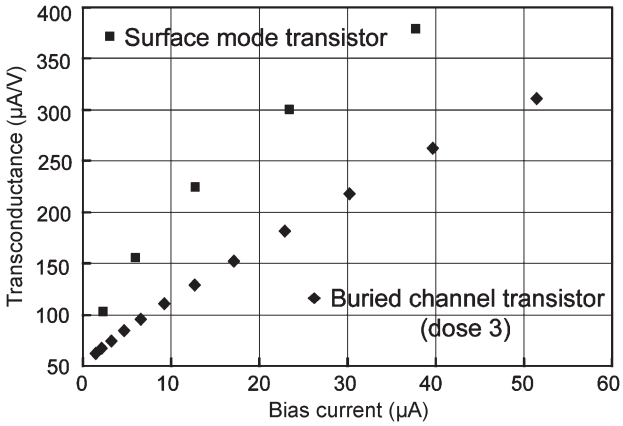

Fig. 6. Measured g_m of the surface and buried-channel transistor.

expected operation points. In Fig. 6, the measured g_m of the surface- and buried-channel transistors is shown as a function of the bias current. The experiment was done with a fixed source voltage in order to include the body effect. The gate voltage is swept to acquire all the dc points. As shown, with the same bias current, the g_m of the buried-channel device is almost half of that of the surface-mode device, which is due to the fact that the channel is buried into bulk silicon, and, thus, less gate-modulation efficiency; such effect is similar to increasing the gate-oxide thickness. The decreased g_m may cause a longer settling time, but this difference of buried- and surface-mode devices is rather unimportant. In imaging applications, the signal on the SF gate normally varies between reset and video signals, and the settling time of the column is mainly dominated by the slew rate (charge/discharge of the column capacitor).

The buried-channel implantation, in fact, also changes the gate capacitance of SF; thus, a change of g_m is observed. BSF pixels should have a higher capacitance of floating diffusion (FD) node. However, the capacitance of the FD node measured consists of FD active capacitance, SF capacitance (only 1/3), TG overlap capacitance, and other parasitic capacitances; thus, an increase due to buried-channel implantation is not so obvious.

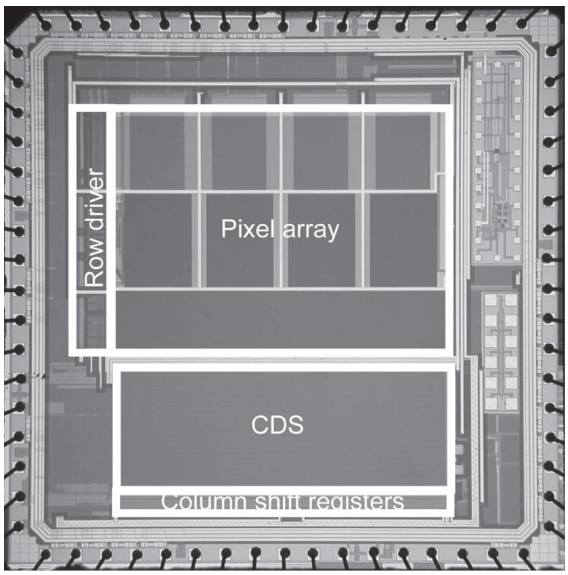

Fig. 7. Chip micrograph of the prototype imager.

Based on the simulation results and test transistor characterization, it is shown that the buried-channel conditions, i.e., maximum channel potential and buried depth, and the threshold voltage of transistors are strongly dependent on implantation energy and dose. Increasing the implantation energy will slightly increase the channel depth, however, with the risk of a large leakage current. Therefore, the implantation dose and energy need to be adjusted carefully to obtain an optimized channel depth and threshold voltage. On the other hand, in order to inspect how much CMOS imagers may benefit from BSFs in terms of read-out noise, a large number of buried-channel nMOSTs need to be measured to acquire enough statistical data. Thus, the benefits from BSFs in terms of read-out noise can only be proved by measuring the actual sensors.

IV. Sensor Design

A prototype sensor with BSFs was first fabricated in a 0.18-μm 1P3M CMOS process by TSMC. The chip micrograph with several fundamental functional blocks of the prototype chip is shown in Fig. 7. The pixel array is 240 rows $\times$ 300 columns with three different pixel pitches, i.e., 6, 7.4, and 10 μm. All pixels are pinned-photodiode 4T designs with both BSF and surface-channel SF (SSF) pixels on the same sensor. In the pixel design, the gate signal of all transistors, i.e., the reset transistor (RT), the charge transfer transistor, and the row select transistor, can be supplied individually. The fill factors for 6- and 7.4-μm pixels are quite low in order to give flexibility to the SF sizing. The row and the column addressing circuitry are realized through a shift register structure. The CDS at each column is used to cancel out the offset, the reset (kTC) noise, and the $1/f$ noise. The pixel output can be amplified ten times by the CDS amplifier to lift the signal and the noise floor already from chip level in order to achieve good accuracy of the noise measurement. The front-end read timing is supplied by an external FPGA. The sensor clock frequency is 10 MHz, which is a unit clock signal (clk) applied through the FPGA. The sensor signal will be read out during each line time, which is 3000 clk cycles for this case. During these 3000 clk cycles, one line of pixels is being read out to the column bus, CDS will be performed, and video signals will be read out by an output amplifier one by one from that line of pixels. Integration time is set by n times of line time, and n can be adjusted through I2C interface on an FPGA coding program. The sensor has a rolling shutter operation. The SF settling time is 0.5 μs, which is five clk cycles. For the noise measurement, the CDS time interval is 1.5 μs, and the charge transfer period is 1 μs. The outputs of the imager are analog signals, being converted into digital by an off-chip image processor with a 12-b ADC. The exact analog signal processing chain of a CMOS imager was well explained in [12].

The characterization results of the prototype sensor were already presented and well analyzed in [10] and [13]. The noise improvement achieved by using BSFs inside the pixels was rather significant. However, as explained in [10], a fundamental tradeoff between the maximum pixel output and the image lag did exist in the prototype BSF pixels.

As mentioned in Section II, the maximum pixel output swing can be significantly improved because of the negative V_t of the BSF transistor. However, such improvement is limited by the row select switch, which is normally realized by a standard nMOST. The maximum voltage which can pass through the row select switch is then determined by the gate voltage and threshold voltage of this row select transistor. Therefore, the FD node reset voltage is expected to be reasonably low in order to ensure that the video signal can be properly read out by the row select switch. Meanwhile, a small FD voltage is also preferred in relation to the random noise [13]. However, reducing the FD reset voltage brings a potential risk of incomplete charge transfer from the photodiode to the FD region, thus introducing image lag. Therefore, this tradeoff between the noise reduction and improvement of the output swing (the possibility of introducing image lag) is limiting the feasibility and performance of the BSF pixels. A solution to this issue is proposed and applied to the following design, i.e., a new test sensor with in-pixel BSFs and optimized row select switches.

The new test sensor was fabricated in a 0.18-μm 1P4M CMOS process by TSMC. The chip micrograph with several fundamental functional blocks of the prototype chip is shown in Fig. 8. The pixel array is 200 rows $\times$ 150 columns with 10-μm pixel pitches. All pixels are pinned-photodiode 4T designs with BSF, in which five columns of pixels are with both BSF and an optimized row selector. The schematic of the pixel is shown in Fig. 9, in which a transmission gate is implemented as the row selector. All the other readout structures and techniques were being used as the prototype sensor. The system clock frequency is still 10 MHz. The front-end read timing is supplied by an external FPGA. For the noise measurement, the CDS time interval and the charge transfer period are also the same with the prototype sensor, i.e., 1.5 and 1 μs, respectively. The outputs of the imager are analog signals, being converted into digital signals by an off-chip image processor with a 12-b ADC.

Both prototype and new test imager were successfully fabricated and tested. The measurement results are presented and discussed in the following section.

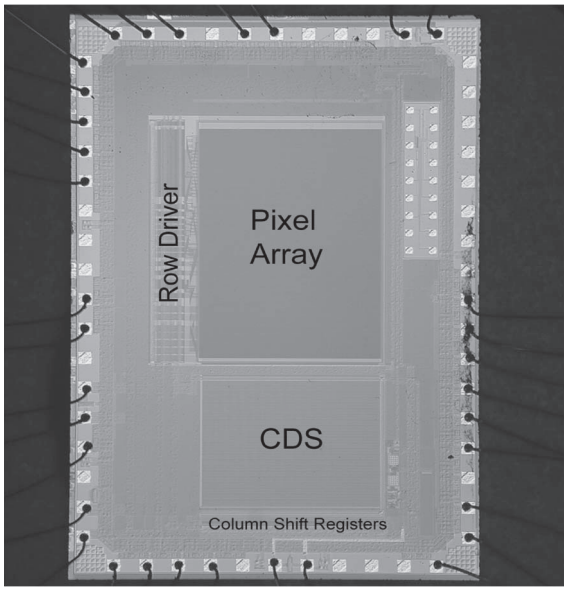

Fig. 8. Chip micrograph of the new test imager.

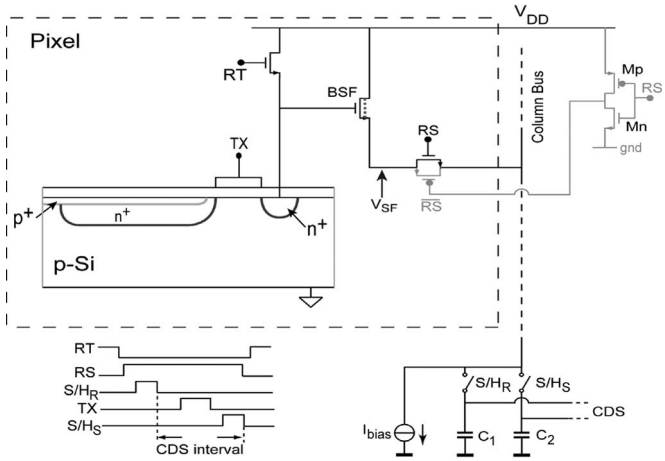

Fig. 9. Pixel schematic and front-end readout timing.

V. Measurement Results

A. Pixel Output Swing

The pixel output swing was measured from the 6-μm pitch pixels in the prototype sensor. The measurement results are shown in Fig. 10. During the measurement, the RT gate is tied to the highest voltage of the pixel, i.e., performing hard reset, and the transfer gate (TX) is grounded. Therefore, the FD voltage equals the RT power supply. The column bias current remains constant for all pixels.

As shown, the output swing of the BSF pixels is about 2 V, nearly double that of the SSF pixels. If the bias current is reduced while the implantation dose remains the same, the pixel output further approaches or even exceeds the line of $V_{\mathrm{FD}} = V_{\mathrm{out}}$, which indicates that the channel is buried deeper into the silicon. If the bias current remains constant, increasing the implantation dose also pushes the channel deeper. Therefore, in principle, the pixel readout noise level, if dominated by the interface trap related noise, will be smaller in case of a smaller bias current or higher implantation dose of the BSF.

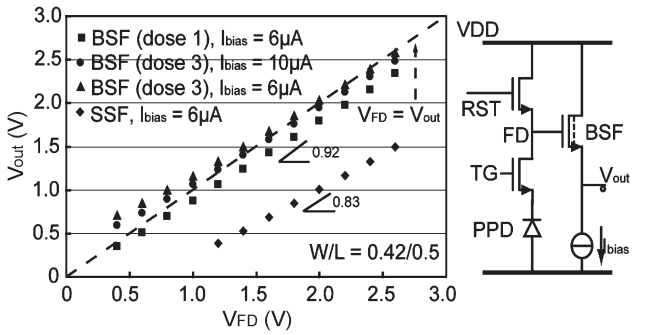

Fig. 10. Pixel output swing measurement with different implantation doping and bias currents.

Furthermore, it can be seen that, regardless of the bias current and implantation dose, all output swing curves tend toward $V_{\mathrm{out}} > V_{\mathrm{FD}}$ at a lower FD voltage, i.e., the SF operates further into the buried mode. Therefore, the pixel readout noise is expected to be reduced as well. The measured voltage gain of the SF is improved from 0.83 of the surface-mode devices to about 0.92–0.95 of a buried-channel transistor. To make a conclusion, both the pixel output swing and the SF voltage gain are improved by using the BSFs inside the pixel.

B. Dark Random Noise

The pixel random noise can be measured by calculating the standard deviation of each pixel output among multiframes. However, in order to distinguish that the random noise is from the APS pixel or from the analog processing, one common approach is to ground the row select transistor during operation; thus, the pixel output node can be considered as floating, and the measured random noise is the noise of the analog chain. Therefore, if any changes of the in-pixel transistor or photodiode operation status during the imager operation, e.g., the integration times, the bias current of the SF, and the reduction of the CDS period, introduce significant effect on the random noise, it can be confirmed that the measured noise is indeed from the pixel-level noise sources instead of the analog chain. In order to exclude the contribution of the photon shot noise from the total noise floor, all the noise measurements were carried out in complete darkness.

The dark random noise of BSF and SSF pixels was measured with both the prototype and new test sensor. Both the BSFs and SSFs were biased with 6-μA current. The FD reset voltage of the SSF pixels was 3.3 V, while in order to ensure that the row select transistor works properly, the measurement was done with a low FD reset voltage on the BSF pixels in the prototype sensor, i.e., 1.8 V. However, with the optimized row selector, the dark random noise can be measured with a much higher FD reset voltage on the BSF pixels in the new test sensor, i.e., 3.3 V.

The measurement results from the prototype sensor were presented in [13]. A test image captured in the dark is shown in Fig. 11. The test image was measured in the dark with an analog sensor gain of ten, at 30 ft/s and 33.3-ms integration time and with a 12-b board-level ADC. The CDS interval is 1.5 μs, and the charge transfer period is 1 μs. The upper part of the figure

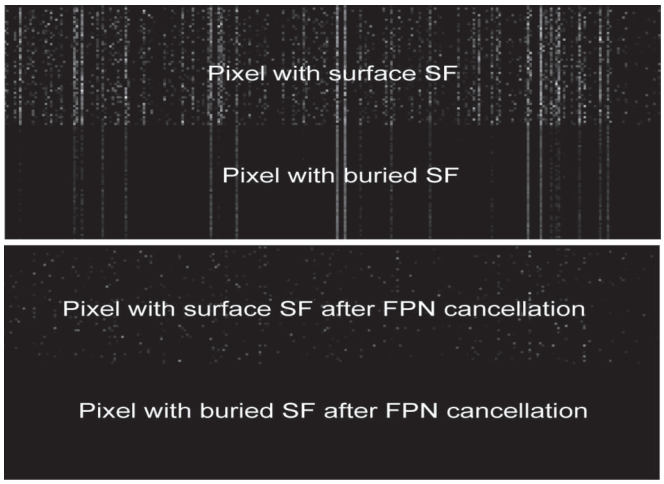

Fig. 11. Test image in the dark, 10× sensor gain [13].

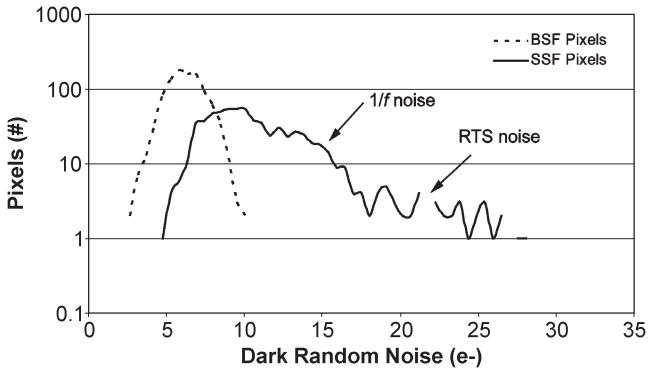

Fig. 12. Histograms of the dark random noise for BSF and SSF pixels in the new test sensor.

shows the raw data, while the lower part shows the data after a digital column-fixed-pattern noise cancellation. About 0.5% of the pixels in the SSF array were observed to be RTS pixels, compared to none in the BSF array.

The results from the new BSF pixels with optimized row selector are shown in Fig. 12. The transistor dimension for both BSFs and SSFs are the same in prototype and new test sensors, i.e., $W/L = 0.42/0.5\ \mu$m. The measurements were processed with an analog sensor gain of 10, at 17 ft/s and with a 12-b board-level ADC. The CDS interval is 1.5 μs with the TX transistor grounded. The FD reset voltage of both the new BSF pixels with optimized row selector and the SSF pixels is 3.3 V. For the new BSF pixels with optimized row selector (10-μm pixel pitch), the fill factor is 33%, and the conversion gain is 41 $\mu\mathrm{V/e^-}$.

The random noise of each pixel is obtained by calculating the standard deviation over 20 frames' outputs. The asymmetric distribution of the pixels around the peak of the SSF pixel curve indicates the dominance of the $1/f$ and RTS noises of the SSF [2]. Comparing with previous results [13], the same random noise improvement is still shown in the pixels with BSFs and optimized row selectors. The average dark random noise of the BSF pixels is about 5 $\mathrm{e^-}$, reduced around 50% comparing with the SSF pixels, and the noise histogram of the BSF pixels closely approximates a true Gaussian distribution with significantly reduced noise spread. Moreover, no hot pixel (high $1/f$ noise) or blinking pixel (RTS pixel) has been found in the 200 row × 150 column BSF pixel array of the new test sensor.

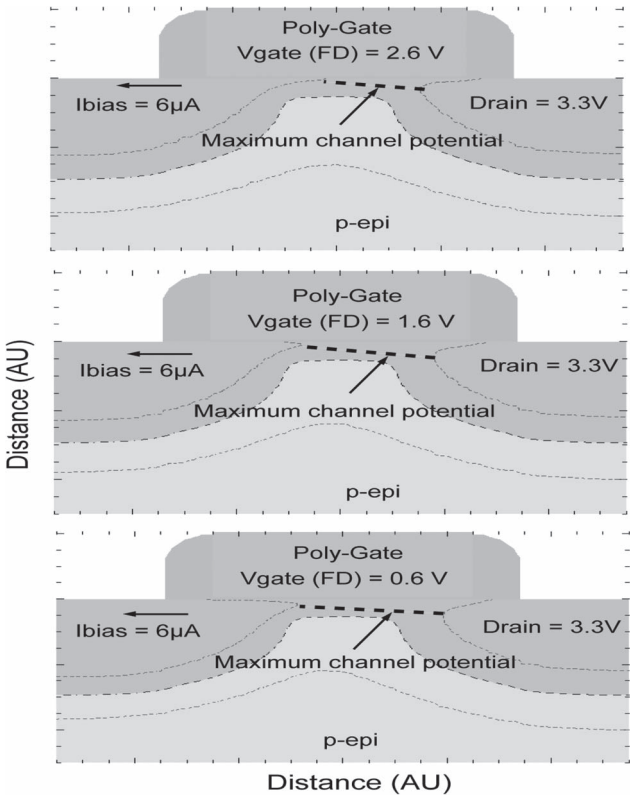

Fig. 13. Simulation of the depletion region and the channel location of a BSF with different gate bias.

As shown in Fig. 13, the simulation results of the depletion region and the channel location change of a BSF pixel with varying FD voltages are presented. It can be seen that the FD reset voltage (gate bias) has strong influence on the potential distance and depletion region at the Si-SiO_2 interface. Reducing the gate bias helps to push the channel deeper; this extends the depletion region at the interface further toward the source side. This condition means that the total channel length will have more area working as a buried-channel mode rather than surface mode; in other words, it can be understood such that the total buried-channel length is increased by reducing the gate bias.

From the new test sensor, the measurement result of the average dark random noise as a function of different FD voltages is shown in Fig. 14. Apparently, the relationship between pixel random noise and SF channel depth is confirmed by the results. The channel is buried deeper by lower FD voltages; therefore, the measured random noise is smaller for lower FD voltages. However, a low FD voltage may introduce image lag because of the incomplete charge transfer.

VI. Conclusion

A CIS with an in-pixel BSF and an optimized row selector has been presented. Compared with a conventional surface-mode SF design, the BSF can gain the following: 1) a reduction

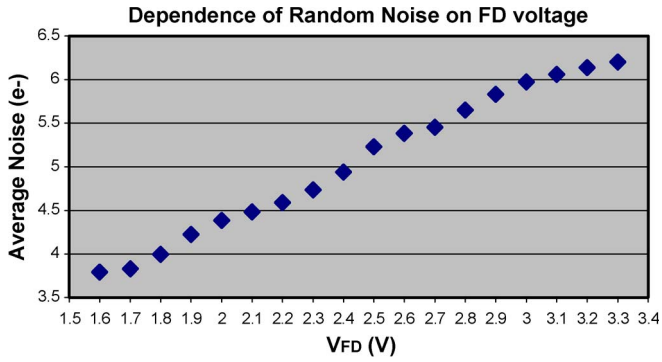

Fig. 14. Dark random noise measurement with different FD voltages.

of more than 50% in dark random noise and improvement of noise spread; 2) a significant reduction of the RTS noise component; 3) a nearly 100% improvement in pixel output swing; and 4) an increase in the voltage gain of the in-pixel SF. Comparing with our previous work [13], the new designed BSF with an optimized row selector still shows the same attractive dark random noise performance and, moreover, is able to get rid of the tradeoff between the noise reduction and the improvement of the pixel output swing.

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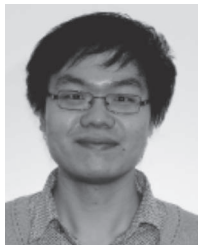

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