

Characterization of In-Pixel Buried-Channel Source Follower with Optimized Row Selector in CMOS Image Sensors

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Abstract — This paper presents a CMOS image sensor with pinned-photodiode 5T active pixels which use in-pixel buried channel source follower (BSF) and optimized row selector (RS). According to our previous work [1], using in-pixel BSFs can achieve significant pixel dark random noise reduction, specially for in-pixel random telegraph signal (RTS) noise, but due to the positively-shifted threshold voltage of the nMOS BSF, it will also introduce a fundamental trade-off between the maximum pixel output and image lag. Also due to this trade-off, our previous results were only measured in dark [1]. Therefore further optimization is necessary. To solve this trade-off but without any influences of the noise improvement from the BSF, a further optimized pixel structure, i.e. in-pixel BSF with optimized RS, is proposed and implemented in 0.18 μm CMOS process.

I INTRODUCTION

During the past few years, a lot of efforts have been made on reducing the random noise in CMOS imagers, which is mainly composed out of $1/f$ and the so called Random Telegraph Signal (RTS) noise [2]. Research has revealed that the dominated random noise sources in CMOS image sensors (CIS) are due to the lattice defects at Si-SiO₂ interface of the in-pixel source follower (SF) transistor [3, 4]. As CMOS processes scale down, the gate area of the transistors becomes so small that it easily happens to have only one active interface trap underneath the transistor's gate, which will induce the RTS noise. Because of this single electron trapping and de-trapping during the transistor operation, the RTS appears in pixels which have only one active interface defect and dominates the pixel temporal noise, which limits the imaging quality under low-light conditions [5]. Therefore, as long as a perfect clean gate interface can not be guaranteed, the $1/f$ or RTS noise will stay dominant in the random noise in pixels.

Our previous work [1] has revealed that taking the conducting carriers away from the Si-SiO₂

interface by creating a buried-channel nMOS SF transistor in a modern CMOS imager process can reduce the dark random noise within pixels dramatically. In this paper, the CIS pixels based on buried-channel nMOS SF transistors with further enhanced performance, i.e. improved output swing and high dynamic range, is introduced. Moreover, because of the drastically improved output swing of the pixels by the buried-channel source follower (BSF) transistor together with an optimized row selector (RS), “digital” transistors with reduced power supply voltages can be used in the pixel without limiting the pixel's output swing, saturation level and dynamic range.

II WORKING PRINCIPLE

In principle, the buried-channel transistors stand for transistors of which the majority of their conducting carriers flow far beneath the gate Si-SiO₂ interface during operation. Actually in modern CMOS processes, the p-type MOS transistors are naturally buried channel devices because of the threshold voltage (V_t) adjust doping process during fabrication. Therefore, the expected structure of a buried-channel nMOS transistor is very straightforward, i.e. a total region reversing of a pMOS transistor, as shown in Fig. 1. The desired operation modes for such a device are shown in Fig. 2. It was simulated from an “ideal” CMOS process, which means all parameters and process flow can be adjusted freely. The dashed lines stand for the boundaries of the depletion regions. As shown in Fig. 2, during switch off, the gate interface region is fully depleted and no current flows from the drain to the source. While during the linear operation, the two depletion regions are separated from each other, which allows current to flow. In the saturation region, the channel is pinched off near the drain side.

Because of the buried-channel doping, the V_t of this nMOS transistor is shifted towards a negative

value. This will help to increase the pixel output swing.

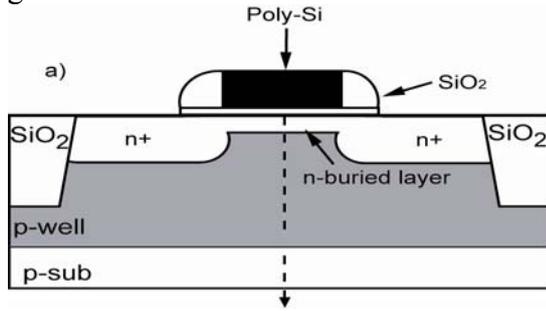


Figure 1. Cross section of a buried-channel Nmos transistor

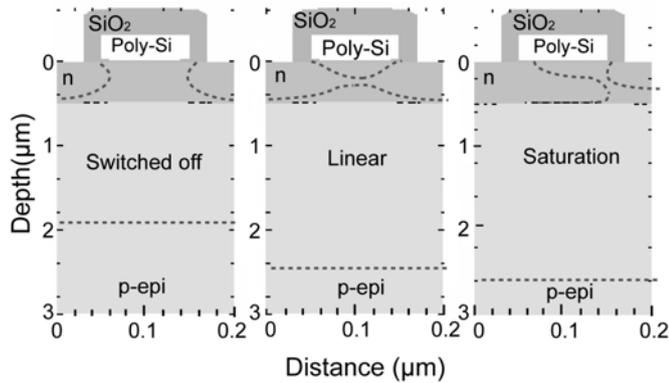


Figure 2. Expected operation modes of a buried-channel nMOS transistor

III SENSOR DESIGN

As mentioned, the maximum pixel output swing can be significantly improved because of the negative V_t of the BSF transistor. However, such improvement is limited by the row select switch, which is normally realized by a standard nMOS transistor. The maximum voltage which can pass through the row select switch is then determined by the gate voltage and threshold voltage of this row select transistor. Therefore, the floating diffusion (FD) node reset voltage is expected to be reasonable low in order to ensure that the video signal can be properly readout by the row select switch. However, reducing the FD reset voltage brings a potential risk of incomplete charge transfer from the photodiode to the FD region, thus introducing image lag. Therefore, this trade-off between the noise reduction and improvement of the output swing (the possibility of introducing image lag) is limiting the feasibility and performance of the BSFs pixels. A solution to this issue is proposed and applied to the following

design, i.e. a test sensor with in-pixel BSFs and optimized row select switches.

The test sensor was fabricated in a 0.18 μm 1P4M CMOS process by TSMC. The chip micrograph with several fundamental functional blocks of the prototype chip is shown in Fig. 3. The pixel array is 200 rows \times 150 columns with 10 μm pixel pitches. The Pixels are implemented with pinned photodiode 4T structures with BSFs and optimized RSs, 5 columns of which are still with conventional SSFs for noise comparison. The schematic of the pixel is shown in Fig. 4, in which a transmission gate is implemented as the row selector. The system clock frequency is 10MHz. The front-end read timing is supplied by an external FPGA. For the noise measurement, the CDS time interval and the charge transfer period are 1.5 μs and 1 μs , respectively. The outputs of the imager are analog signals, being converted into digital by an off-chip image processor with 12bit ADC. The test imager was successfully fabricated and tested. The measurement results are presented and discussed in the following section.

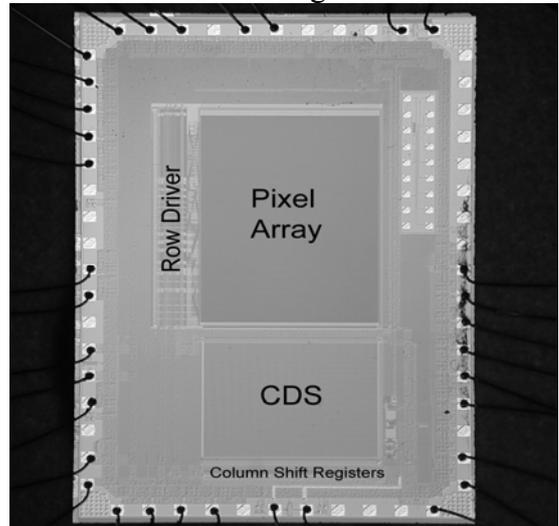


Figure 3. Chip micrograph of the test imager

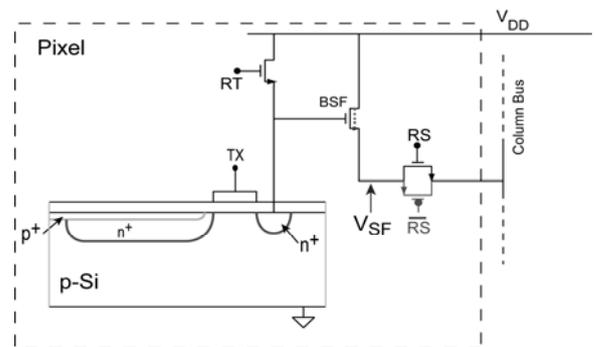


Figure 4. Schematic of pixels of the new test imager

IV MEASUREMENT RESULTS

Compared to [1], the sensor characterization is done not only in dark but also with light injection, such that more detailed performances of pixels with BSF can be revealed accordingly, e.g. conversion gain and dynamic range.

The pixel output swing is measured. The measurement results are shown in Fig. 5. During the measurement, the reset transistor (RT) gate is tied to the highest voltage of the pixel and the transfer gate is grounded. Therefore, the FD voltage equals the reset transistor power supply. The column bias current remains constant for all pixels.

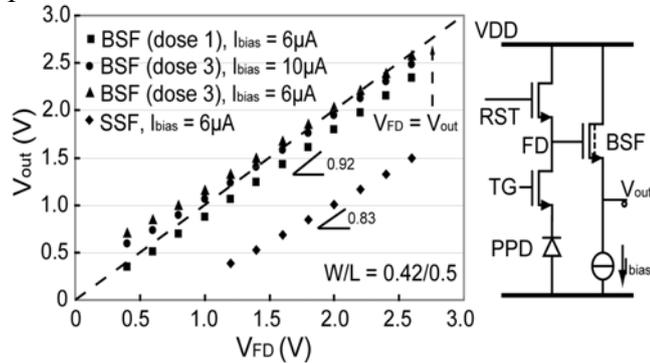


Figure 5. Pixel output swing measurement with different implantation doping and bias currents

As shown, the output swing of the BSF pixels is about 2 V, gaining almost 100% improvement compared that of SSF pixels. If the bias current is reduced while the implantation dose remains the same, the pixel output further approaches or even exceeds the line of $V_{FD}=V_{out}$, which indicates that the channel is buried deeper into the silicon. If the bias current remains constant, increasing the implantation dose also pushes the channel deeper. Therefore, in principle, the pixel read-out noise level, if dominated by the interface trap related noise, will be smaller in case of a smaller bias current or higher implantation dose of the buried-channel source follower. Furthermore, it can be seen that regardless the bias current and implantation dose, all output swing curves tend towards $V_{out} > V_{FD}$ at a lower FD voltage, i.e. the source follower operates further into the buried mode. And therefore, the pixel read-out noise is expected to be reduced as well. The measured voltage gain of the source follower is improved

from 0.83 of the surface-mode devices to about 0.92~0.95 of a buried-channel transistor. As a conclusion, both the pixel output swing and the source follower voltage gain are improved by using the BSFs inside the pixel.

The dark random noise of BSF and SSF pixels is measured with the sensor. Both the BSFs and SSFs are biased with 6 μA current and 3.3 V power supply. The random noise of each pixel is taken by calculating the standard deviation of pixel outputs through 20 frames. In order to exclude the contribution of the photon shot noise from the total noise floor, all the noise measurements are carried out in complete darkness. The transistor dimension for both BSFs and SSFs are $W/L=0.42\ \mu\text{m}/0.5\ \mu\text{m}$. The measurements were processed with an analog sensor gain of 10, at 17fps and with a 12bit board-level ADC. The CDS interval is 1.5 μs with transfer gate (TX) transistor grounded. Hard reset is performed both on the new BSF pixels with optimized RS and SSF pixels. For the new BSF pixels with optimized RS (10 μm pixel pitch), the fill factor is 33% and the conversion gain is 41 $\mu\text{V}/e^-$.

As shown in Fig. 6, the asymmetric distribution of the pixels around the peak of the SSFs pixel curve indicates the dominance of the $1/f$ and RTS noise of the SSFs. The average dark random noise of the BSF pixels is about 5 e^- , reduced around 50% comparing with the SSF pixels, and the noise histogram of the BSF pixels closely approximates a true Gaussian distribution with significantly reduced noise spread.

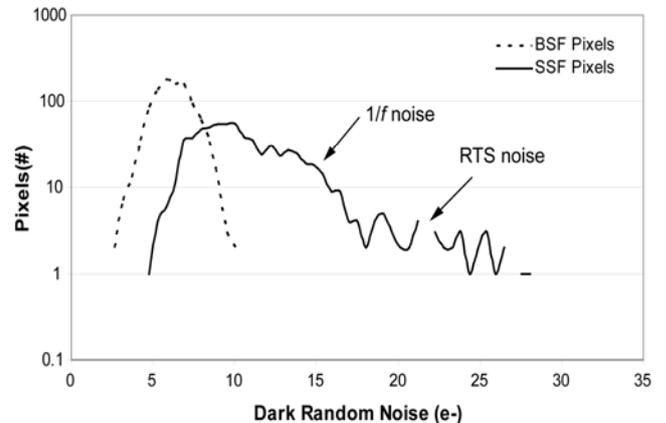


Figure 6. Histograms of the dark random noise for BSF and SSF pixels

The measurement result of the average dark random noise as a function of different FD voltages is shown in Fig. 7. Apparently, the relationship between pixel random noise and source-follower channel depth is confirmed by the results. The channel is buried deeper by lower FD voltages; therefore, the measured random noise is smaller for lower FD voltages. However, a low FD voltage is not recommended because of the incomplete charge transfer introduced image lag.

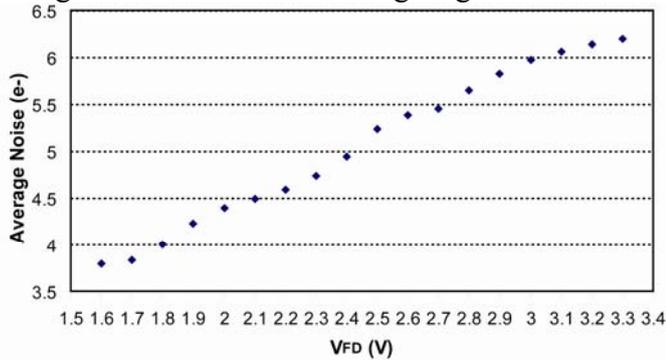


Figure 7. Dark random noise measurement with different FD voltages

Photon transfer curve (PTC) measurement for the BSF pixels with optimized RS is implemented with a DC current controlled monochromic light source. During the measurements, the light intensity is varied and the exposure time is kept constant, i.e. 200 line times (1 line time=0.3 ms). The reset voltage on floating diffusion (FD) node was set to be 3.3 V, i.e. performing hard reset. The measurement is processed under a room temperature. The system analog gain is set to be unit.

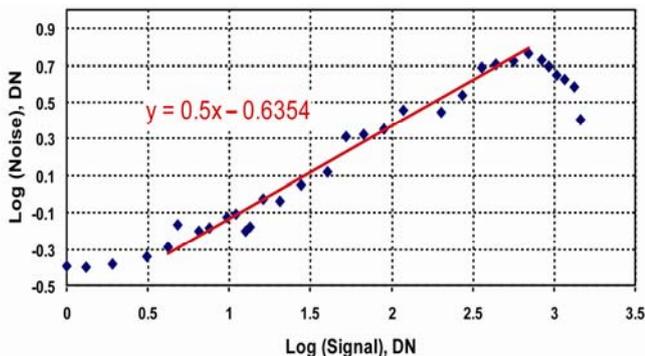


Figure 8. PTC of pixels with BSF and optimized RS

By calculating from Fig.8, the full well of pixels with BSF and optimized RS is 19500 e⁻, while read

noise is around 7 e⁻. The dynamic range achieved is 68 dB.

V CONCLUSIONS

A CMOS image sensor with an in-pixel buried-channel source follower and an optimized RS is presented. The results show that compared to a regular imager with the standard nMOS transistor SSF, the new pixel structure improves output swing by almost 100% without any conflicts to the signal readout operation of the pixels and still can reduce dark random noise by 50%. Moreover, with optimized RS, hard reset on the pixel FD node can be operated, together with the output swing and noise improvement, it finally achieves 68 dB dynamic range. As a conclusion, the new pixel structure is able to not only drastically minimize in-pixel RTS noise but also improve output swing and dynamic range.

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