A CMOS Image Sensor with Row and Column Profiling Means

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Abstract—**This paper describes the implementation and first measurement results of a new way that obtains row and column profile data from a CMOS Image Sensor, which is developed for a micro-Digital Sun Sensor (μDSS).The basic profiling action is achieved by the pixels with p-type MOS transistors which realize a so-called "Winner Takes It All (WTIA) [1][2]" principle. The WTIA implementation improves the μDSS system greatly on speed and power consumption. In this way the sensor is ideally suited for a digital sun sensor intended for astronomy applications.**

I. Introduction

The micro-Digital Sun Sensor (μDSS) is a System-on-Chip (SoC) solution developed for micro satellites. The μDSS system is employed to detect the satellite's attitude angle with respect to the sun. With the angle information, the satellite's location in space can be achieved by a dedicated algorithm.

Figure 1 illustrates the working principle of the μDSS. The sun is considered as a point light source in this application. The sun sensor, which is placed on the satellite, has a thin membrane above the chip surface. This membrane has a pinhole on the top. In this way, the sunlight goes through this pinhole leaving a sun spot on the image sensor array. The image sensor within the μDSS system reads out this sun spot's location on the focal plane. With this location information, the algorithm circuit will calculate the attitude angle of the satellite with respect to the sun. The attitude angle is fully determined by angels α and θ in Figure 1. The specification is to detect values for θ within $\pm 64^0$. In order to fully cover 360^0 range, three μDSS are needed for one satellite. For the application of μDSS, the size of the image sensor array is 512×512. The pixel pitch is 6.5μm.

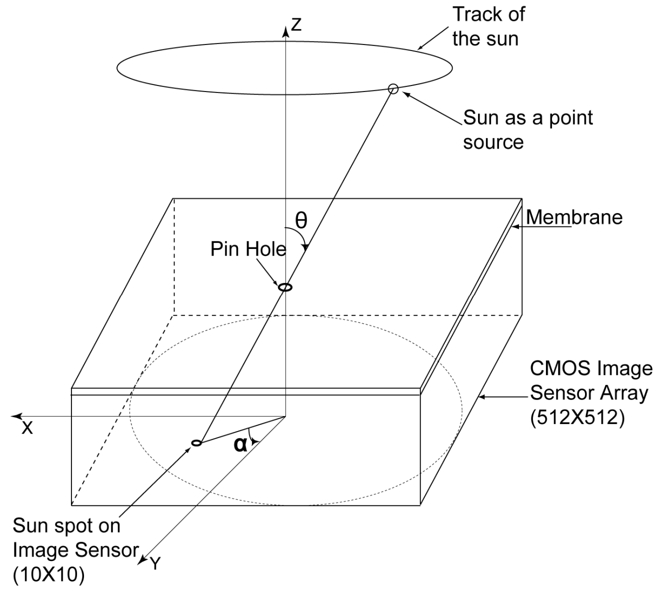

Figure 1. μDSS system

For an ordinary sun sensor, the location of the sun spot is detected based on the readout data of every pixel. Therefore, the sun spot cannot be located before every pixel in the 512×512 pixel array has been read out. In order to accomplish the process more quickly in speed wise and more efficiently in power wise, the μDSS applies a two-fold working mode: acquisition mode and tracking mode, which operate successively.

Acquisition mode: In the μDSS application, the sun approximately illuminates 10×10 pixels of the array. Therefore only this sub-array is of interest within the complete pixel array. The technique of reading out the sub window which contains the useful information is called

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"Region Of Interest" (ROI). The purpose of the acquisition mode is to determine a 21×21 pixels region which contains the 10×10 pixels sun spot. In other words, a rough location of the sun spot is detected. [3][4] With this rough location information, only 21×21 pixels, instead of the complete 512×512 pixel array, are going to be readout in the next working stage. The 21×21 pixels readout data will be sufficient for the algorithm to calculate the center of the sun spot. The 21×21 pixel region is decided by means of a profiling technique called "Winner Takes It All". Figure 2 illustrates the WTIA principle. At the end of the integration time, all column/row buses on the image sensor contain the information of the strongest illuminated pixel (the "winner") on each particular column/ row respectively. In this way, the profile along column/row direction can be achieved (indicated by red lines). The "winner" occupies the column/ row bus; this is the reason that the principle is called "Winner Takes It All". With this working mode, profiles are achieved within readout time for two lines.

Tracking mode: At the end of the acquisition mode, the 21×21 pixel region of interest (ROI) is identified. The sensor will be switched into the sun tracking mode, in which it works the same way as an ordinary 3T APS image sensor: every pixel in the 21×21 sub- array is readout one by one. The ROI will be read out with the highest accuracy because the data read out in this mode will ultimately determine the accuracy of the complete sensor.

By this acquisition- tracking mode operation, the μDSS can locate the sun spot within the readout time of two lines (acquisition mode) plus 21×21 pixels (tracking mode). Therefore, compared with an ordinary sun sensor, the μDSS has a faster speed and lower power consumption.

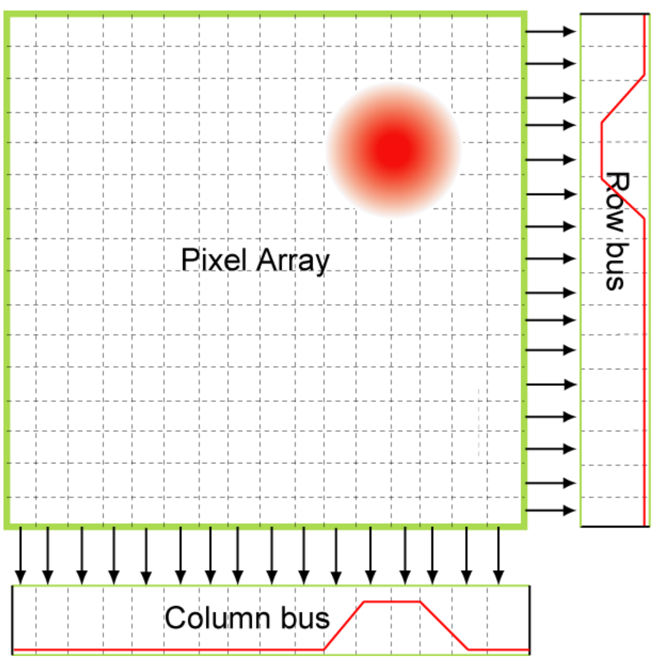

Figure 2. Profiling on column and row directions

II. Circuit Design

A. *"Winner Take It All" principle*

In the μDSS application, the "winner" is the pixel which is illuminated the most heavily in the pixel array. Due to the working principle of a CMOS pixel, these pixels will have the lowest voltage level after an integration time. So "Winner Takes It All" in an image sensor means the voltage level on the column bus and row bus should be decided by these lowest voltage levels.

The working principle of "Winner Takes It All" is demonstrated in Figure 3. The pixel structure, employing this principle, is basically the same as an ordinary 3-T APS pixel, consisting of a photodiode, a source follower and a row select transistor, except that all transistors are p-MOS type. Take a column of three pixels as an example. In the acquisition mode, the light input is not uniform. The second pixel is assumed to be the most illuminated one and the first pixel is the second most illuminated. After the integration time, the voltages across the photodiodes will be: $V2<V1<V3$. Next, the circuit works in the following steps:

1. At the end of integration time, all row select switches (RS) are turned off; the voltage at the column bus (Vc) is high due to the current source and capacitive load on the column bus. When integration is completed, RS1, RS2 and RS3 are turned on at the same time. At this moment, Vc is high enough to turn on the three source followers (SF1, SF2 and SF3); the current going through these three transistors will force Vc start to decrease.

2. Due to the lowest photodiode voltage, the second source follower (SF2) has the largest current among the three. SF2 sinks most of the current from the current source and forces Vc decreasing until Vc reaches V2+Vth, where Vth is the threshold voltage of the source follower transistors.

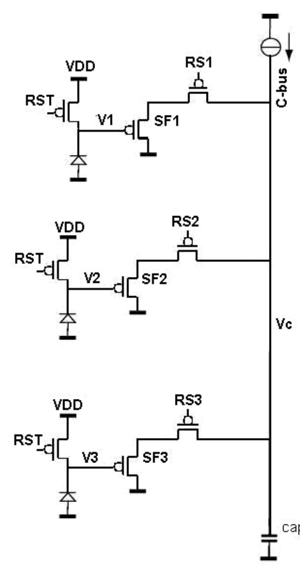

Figure 3. "Winner Takes It All" on one column

3. Vc becomes stable at V2+Vth, which means the column bus voltage is now determined by the most illuminated pixel on the specific column. This is the so-called “Winner Takes It All” working principle.

The discussion above demonstrates the operational principle of “Winner Takes It All”. It can process the data very fast because it does not need to readout every pixel on the same column. In this way, this technique also helps to save power.

B. Modified pixel structure

The pixel structure in Figure 3 can only implement the profiling on column direction. In order to fulfill both column and row profiling with one pixel, the pixel is modified with an extra column select switch (CS) as well as a row bus (R-bus), as illustrated in Figure 4. With this modification, row direction “WTIA” principle works in the same way as on the column direction. Profiling information is presented on the row buses. In this way, both column and row profiling information are achieved by identical pixel configuration.

C. Image sensor design in μDSS

As illustrated in Figure 5, the image sensor in μDSS is composed of five parts: pixel array, current mirror array, column sample-hold array, two address decoders (one in column direction and one in row direction), and a chip level analog chain which processes the signals and generates the sensor output in analog domain. [5] This architecture is almost the same as an ordinary 3-T APS image sensor. The only difference is that the μDSS needs two address decoders, comparing with an ordinary 3-T APS image sensor has only one row decoder. The two decoders enable the pixel array randomly accessible. This is very useful in the tracking mode when a 21× 21 pixel region is going to be addressed.

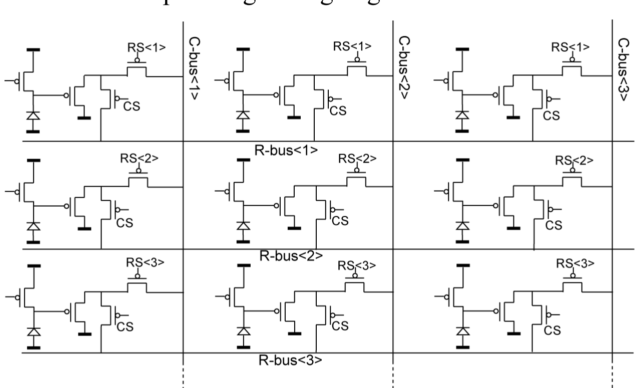

Figure 4. The pixel structure which can implemnet both column and row profiling

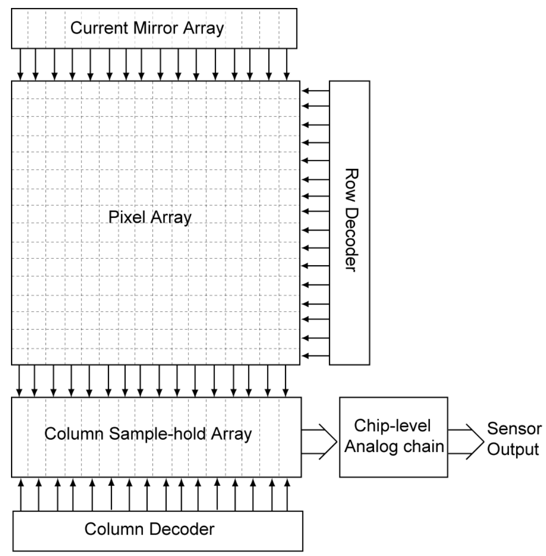

Figure 5. μDSS image sensor

III. TEST RESULTS

A first test chip has been realized: 368 × 368 pixels, 6.5μm pixel pitch, manufactured in a 0.18μm CMOS process. The profiling function is tested in the acquisition mode, as illustrated in Figure 6. The results demonstrate the WTIA principle works well on both column and row directions. The x and y coordinate of the light spot’s location is implied by the peak of each curve.

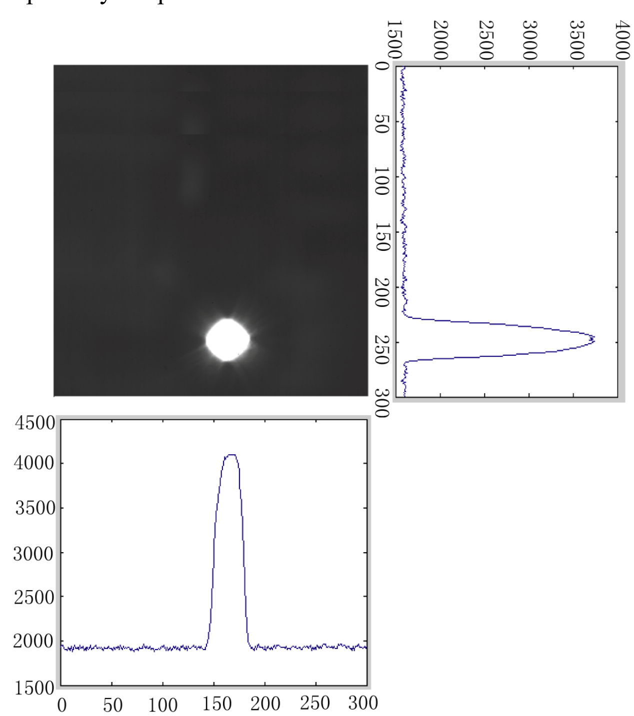

Figure 6. Measurement results for “WTIA” on column and row

Besides WTIA principle, the µDSS can also operate as an ordinary image sensor in the tracking mode. Figure 7 shows an image taken by the test chip.

Another important parameter for the image sensor of µDSS is the full well capacity. The typical value for sun radiation reaching the µDSS surface is $1500W/m^2$. If the full intensity goes through the pin hole without attenuation, the pixels will be constantly saturated. Therefore a filter above the membrane is necessarily used to limit the amount of sun light to a reasonable value. For this reason, the filter will be designed according to the full well capacity to make sure the photodiode is not saturated by the number of photons reaching the sensor.

"Photon Transfer Curve" is a measurement tool which can be used to evaluate many parameters of an image sensor, including full well capacity (e-/pixel), conversion gain K (DN/e-), conversion factor CF (V/e-), etc. The test results of the test chip, illustrate this curve in Figure 8. In the first regime, the read out noise floor is ultimately limited by on-chip amplifier noise. Therefore the curve slope equals to 0. As the illumination is increased, the photon shot noise becomes dominating, which is characterized by a slope of 0.5. In the third regime, the noise drops down dramatically due to the saturation. TABLE I shows the parameters derived from this curve.

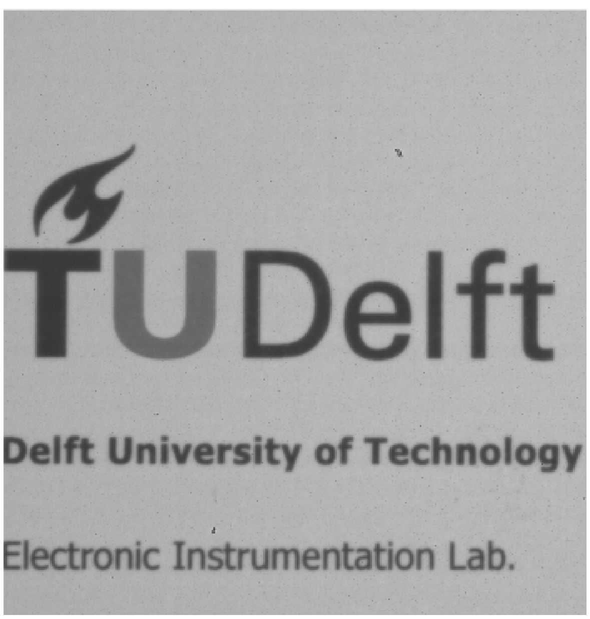

Figure 7. Image captured by the test chip

TABLE I. IMAGE SENSOR PARAMETERS

Full Well Capacity, Q (e-/pixel)	**Conversion gain, K (DN/e-)**	**Pixel capacity, C (fF)**	**Conversion factor, CF (µV/e-)**
37,000	0.045	5.3	30

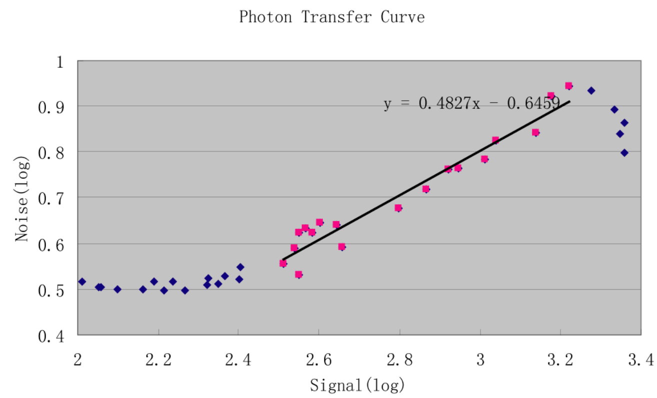

Figure 8. Measurement results of the "Photon Transfer Curve"

IV. CONCLUSION

This paper describes the implementation and first test results of a new way to obtain row and column profile data from a CMOS Image Sensor. The µDSS image sensor works in two stages: First, in the acquisition mode, the sun spot's location is roughly detected. This process is very fast, since the determined region will be readout accurately in the next stage. Next, in the tracking mode, the ROI which was derived from the previous mode are read out one by one. The final location of the sun spot will be calculated based on the results in this mode. The basic profiling action is implemented by pixels with p-type MOS transistors that can be switched in a so-called "Winner Takes It All (WTIA)"configuration. With features like fast speed and low power consumption, the WTIA implementation makes the image sensor ideally suitable for µDSS which is intended for astronomy applications.

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