CCD structures implemented in standard 0.18 μm CMOS technology

P.R. Rao, X. Wang and A.J.P. Theuwissen

A novel concept of implementing charge-coupled devices (CCDs) in a 0.18 μm CMOS technology is developed. This structure is targeted towards large pixels for medical applications. No major process modifications are necessary for implementing this structure.

Introduction: Charge-coupled devices (CCDs) have conventionally used overlapping (0.5–2.5 μm) polysilicon gates to achieve charge transfer between gates with a very high charge transfer efficiency (CTE) [1]. Since conventional CMOS processes do not allow poly-overlaps, it was not possible to achieve a 'true' CCD structure in this process until now, though efforts were made in this direction [2]. With the aggressive scaling of CMOS technology to deep sub-micron dimensions, the design rules permit fabrication of polysilicon gates very close (~0.24 μm) to each other. From device simulations, we find that this would allow the gate potentials to overlap, and create sufficient transverse field to transfer charges between adjacent gates. The size of the gap is critical and, from simulation studies, the minimum gap required for efficient charge transfer in 0.18 μm CMOS technology is found to be less than 0.4 μm. The actual gate gap used in our design was 0.24 μm, which ensures a smooth transfer of charges without potential 'bumps'. Since medical applications require the use of very large pixels (30 × 30 μm) (both photodiodes as well as photo-gates), complete charge transfer is a major issue. If CCD structures could be implemented in current CMOS technologies, this problem can be circumvented. Photo-gate sensors suffer from lower sensitivity to lower wavelength photons ($\lambda < 450$ nm) owing to absorption of these photons in the polysilicon layer ($t_{poly} \sim 150$ nm). For specific applications where a scintillator layer converts the incoming radiation (ex. X-rays) to a particular wavelength in the visible spectrum (e.g. Gd_2O_2S:Tb; 545 nm) such problems can be eliminated. Moreover, since deep sub-micron technology is highly radiation tolerant, such pixels can be effectively used in applications involving harsh environments [3].

Device simulation and fabrication: The proposed pixel structure is shown in Fig. 1. It consists of at least two photo-gate pixels separated by a gap, a transfer gate (TX1) to transfer charges to the n^+ floating-diffusion node (D) after the integration, and a reset transistor (Rst) to reset the node after read-out through the source follower (SF). The gate-oxide thickness was 7 nm for the simulation and CMOS 0.18 μm technology parameters were used for the simulation. To evaluate the performance of the CCD without using visible radiation, the fabricated structure has a source (S) for 'injecting' electrons, controlled by a transfer gate (TX2).

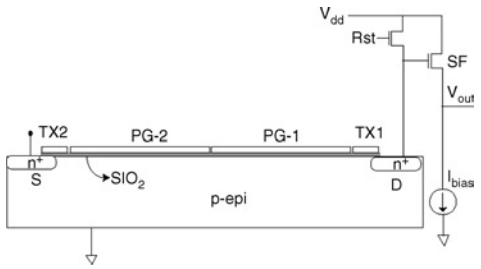

Fig. 1 *Proposed device structure*

Fig. 2 shows the layout schematic of the proposed pixel. A metal layer is used to shield non-light sensing parts of the sensor. This layer is connected to ground to avoid it being floating. The size of the photo-gate region is 26 × 31.5 μm and the transfer-gate regions have a length of 1 μm. The floating-diffusion node has a size of 3.7 × 31.5 μm, resulting in a theoretical capacitance of 7.4 fF (reset voltage = 1.18 V), and a conversion gain of 22 $\mu V/e^-$. The drain region length is 3.7 μm, W/L (Rst transistor) = 2.0 and W/L (SF transistor) = 2.5. Since the gates are placed very close to each other, the spacers that are used for the n^+ source/drain implant merge together, thus preventing the formation of silicides in the gap. Since no 'n-LDD' (n-type low doping) depositions were defined, the gaps can be ensured to be free from any kind of implants.

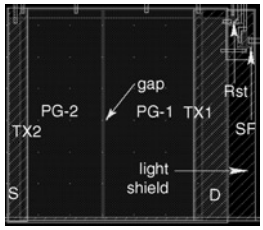

Fig. 2 *Layout of proposed structure*

The simulation of the surface potential of such a structure is shown in Fig. 3, where the gap between the gates is varied from 0.28 to 0.8 μm. As the gap is increased, the surface potential between the gaps tends towards the bulk potential ϕ_B, which would hinder the charge transfer process. Fig. 4 shows a 3-D simulation of the condition after charge-transfer carried out using the simulation tool *Spectra*®. A barrier between the two gates when they are at equal potential suggests that these allow the gates to act as 'pockets'. These pockets provide confinement of charges and hence the ability to perform multi-resolution techniques within each pixel. It also opens up possibilities for various other interesting operations within a pixel, including multiple read-outs for achieving high dynamic range, charge addition within each sub-pixel for higher sensitivity, etc.

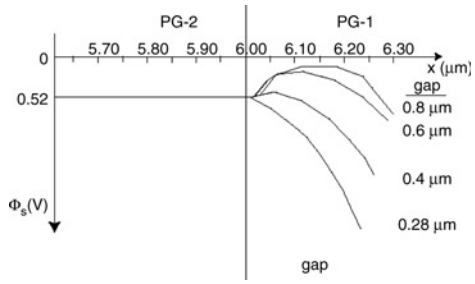

Fig. 3 *Simulation of surface potential during condition PG-1 = 3.3 V, PG-2 = 0 V*

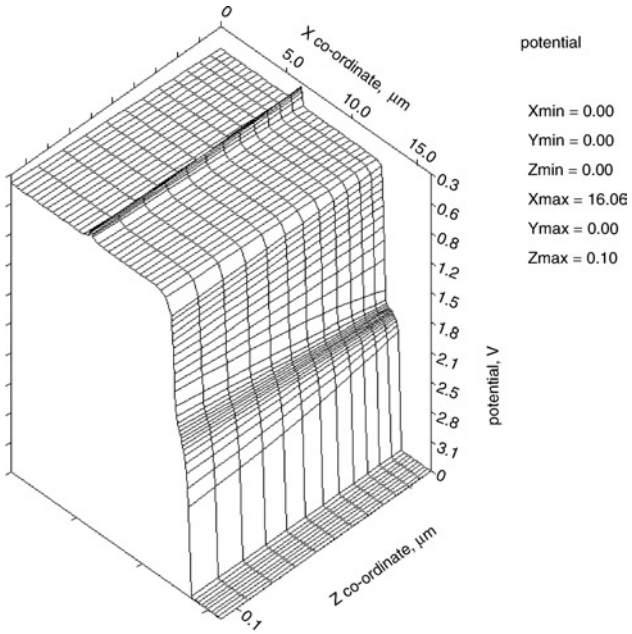

Fig. 4 *3-D simulation of surface potentials after charge transfer cycle (PG-1 = PG-2 = 0 V; TX1 = 1.5 V; V (D) = 3.3 V)*

Results: The dark current from the structure (PG-1, PG-2 = [0, 3.3] V; TX2 = −0.2 V) for the floating-diffusion node reset to a high potential of 1.18 V is approximately $1 nA/cm^2$ at room temperature. Fig. 5 shows the output for the pixel (in the dark) with electrons induced through the source ($V_{source} = 0$ V) via TX2 ([0.4, −0.3] V). The charges that are collected during the integration period ($t_{int} = 0.73$ ms; PG1 = PG2 = [0, 3.3] V) are then transferred to the floating-diffusion node which

had been reset to a high potential, 1.18 V in this case. The drop in the voltage is an indication of the number of charges that were transferred. The output of the two photo-gate structure with an increasing charge injection by means of controlling the duty cycle (4%–16%) of TX2 is shown in the inset and exhibits a good linear relationship. This linear trend is observed until the pixel saturation level of 1.18 V. The light sensitivity of the pixel was tested by illuminating the sensor with a light-source. The sensor was found to be light-sensitive (Fig. 6), but a light leakage is obviously present that has to be considered for optimised pixels in the future. We are working on assessing the CTE as well as the quantum efficiency of multiple photo-gates (up to five gates) and correlating their characteristics to develop a suitable model. Work will also be done on issues such as radiation hardness and noise.

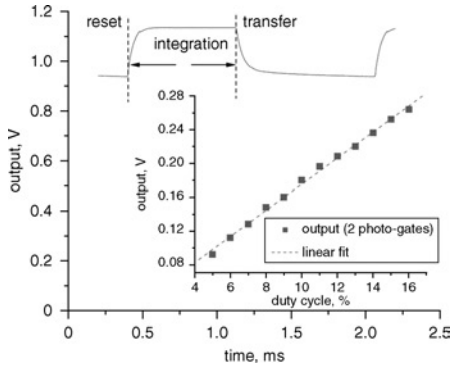

Fig. 5 *Output of pixel and response to increasing charge injection via source region (inset)*

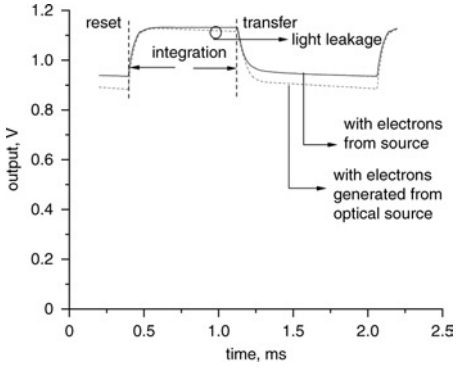

Fig. 6 *Output of two photo-gate structure in response to charge injection via source region as well as optical source*

Conclusions: A CCD-like image sensor in CMOS technology has been realised. The results show that CCD-like structures are feasible in standard deep sub-micron CMOS technologies without the need for process modification. This idea can be utilised for very large area pixels for applications such as medical imaging.

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