

COLUMN-PARALLEL SINGLE-SLOPE ADCS FOR CMOS IMAGE SENSORS

Martijn Snoeij, Albert Theuwissen, Kofi Makinwa and Johan Huijsing

Electronic Instrumentation Laboratory
Delft University of Technology
Mekelweg 4, 2628CD Delft, The Netherlands

Corresponding author: Martijn Snoeij
Phone: +31 15 2786466, Fax: +31 15 2785755
Email: M.F.Snoeij@tudelft.nl

Abstract: In recent years, CMOS imagers have evolved as the imaging technology of choice for high volume mobile applications. The ever-increasing resolution of such imagers has had a profound impact on the analog readout electronics, and, in particular, the ADC architecture. This paper gives an overview of the development of column-parallel ADCs that enable the high-speed, power-efficient readout of high-resolution CMOS imagers.
Keywords: CMOS imagers, interface electronics, A/D conversion, column-parallel ADC.

I INTRODUCTION

CMOS image sensors have several advantages over the more conventional CCDs [1,2]. Firstly, they have a significantly lower power consumption, making them attractive in battery-powered applications. Secondly, the use of CMOS technology enables the design of a 'smart' sensor, i.e. an image sensor with signal processing circuitry co-integrated on the same die, thus making it possible to realize a camera-on-a-chip. This greatly reduces the total size of the camera system, which is important in portable applications, such as cell phones and PDAs. These advantages have resulted in a rapidly growing high-volume market for inexpensive, 'smart' CMOS image sensors in recent years. Within this market, the trend for CMOS imagers is to increase the amount of pixels on the sensor. This has had a profound impact on the on-chip analog interface circuits.

The interface circuitry of a CMOS imager (fig. 1a)

can be divided into two main parts: the pixel readout (front-end) and the A/D conversion (back-end). Fig. 1b depicts a typical front-end of an imager. Three transistors are located inside the pixel, while a biasing source and sample-and-hold capacitors are located outside the imaging array. The latter is usually referred to as the 'column circuit'. The read-out cycle is started by resetting the photodiode with transistor M1. Because of the parasitic capacitance of the photodiode, this defines an initial voltage on the diode. Light incident on the photodiode will create a photocurrent that decreases the initial reset voltage. After a certain time-period, typically several milliseconds, the resulting voltage at the gate of M2, which is proportional to the amount of light, will be read-out. This is done by connecting a row of pixels to the column circuits via transistor M3, controlled by the 'row-select' signal, to the column circuits. The column circuit provides a bias current to transistor M2 that is used as a source follower, and the

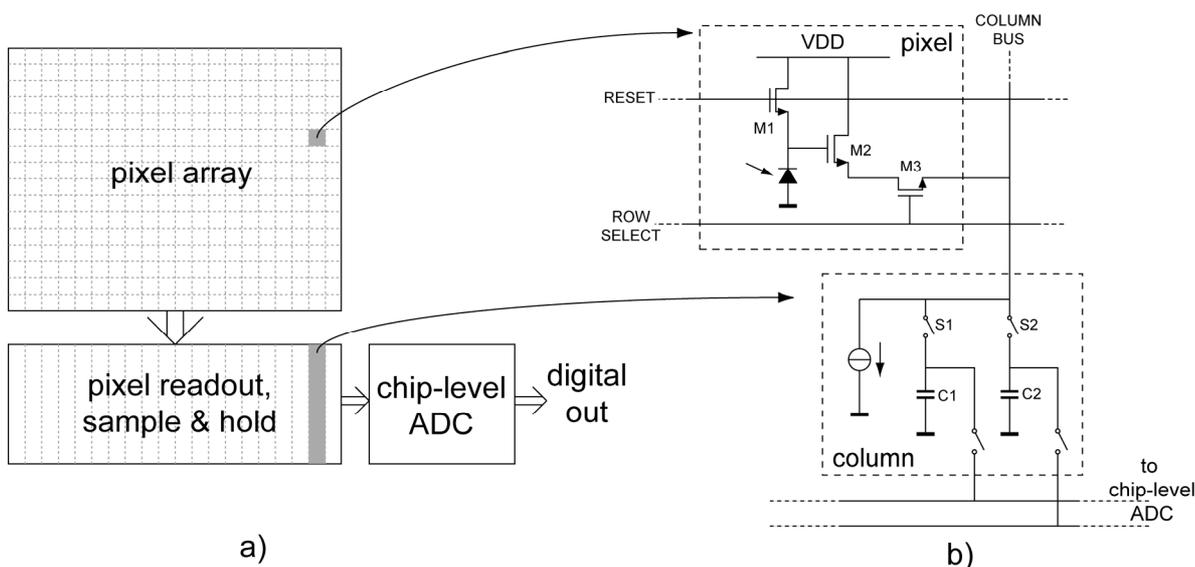


Figure 1 a) Overview of a CMOS image sensor read-out architecture with chip-level ADC b) detailed figure of the in-pixel and column-level front-end circuit

output voltage can be sampled on capacitor C1 with switch S1. After this, the pixel is reset via M1 for a next read-out cycle, and this reset voltage is also read-out and sampled on capacitor C2 via S2. By subtracting the voltages on C1 and C2, the offset as well as $1/f$ noise of the source-follower can be compensated for.

After the pixel readout, the back-end circuit subtracts the analog signals stored in the capacitor array and converts them into the digital domain. In conventional CMOS imagers, this is done by a chip-level amplifier that reads out the capacitors one by one, followed by a single ADC [3]. However, as the pixel-count of CMOS imagers is ever increasing (e.g. in [6], a 6.4Mpixel CMOS imager is presented), it becomes more and more difficult to use this approach, as the readout speed of such an ADC will be directly proportional to the pixel resolution. For a high-resolution imager, the output rate of the ADC would have to be several hundred MSPS, which is difficult to realize. An alternative to a single ADC is to move the task of analog-to-digital conversion into the readout column (fig. 2a); thereby creating a large number of parallel readout channels [4-6]. The resulting readout structure, usually called a column-level ADC is suitable for very-high resolution imagers. This paper gives an overview of the design challenges involved in designing column-level ADCs.

II ADC ARCHITECTURE

In designing a column-level ADC, three design targets must be simultaneously met. Firstly, it is imperative that the read-out channels have a uniform response compared to one another. Any difference in response between the column ADCs will be highly visible as vertical stripes in the produced image. These artifacts are even visible if the magnitude of the non-uniformity is lower than

that of other temporal noise sources in the read-out circuit. Secondly, the required chip area for each readout column should be minimized, since the column ADC should have the same width as a pixel on the chip, which is typically less than $10\mu\text{m}$. Thirdly, the power consumption of the column ADC should be minimized in order to enable battery-powered operation of the imager.

All design targets favor an ADC architecture that uses the simplest possible column circuit. Although several ADC architectures achieve for the required resolution and speed, most of them need either an accurate amplifier or DAC for each ADC channel, and therefore do not satisfy the three above requirements. Therefore, the column-parallel single-slope architecture (fig. 2b) is usually favored because it reduces the required in-column analog circuitry to an absolute minimum: only a comparator is required. It operates as follows: in each column, the sampled input signal is compared to a centrally generated ramp voltage. A central digital counter runs synchronously with the ramp and is connected to digital memories in each column. When the input signal in a certain column equals the ramp voltage, the comparator triggers and the digital memory stores the corresponding counter output.

Reducing the analog circuitry to a single comparator in each column not only has the obvious advantage of low chip area and low power consumption, but also makes it relatively easy to ensure uniformity between the column circuits, since to first approximation, only the comparator offset can cause non-uniformities. Therefore, since the comparator determines the performance of the A/D converter to a large extent, it will be discussed in detail in the next section.

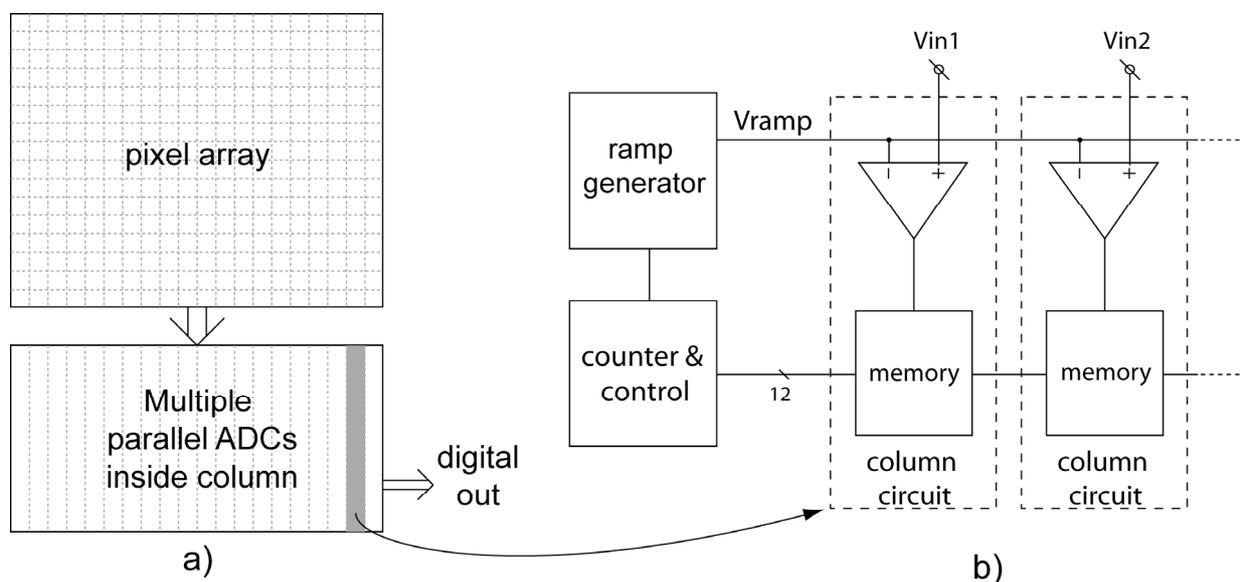


Figure 2 a) Overview of a CMOS image sensor read-out architecture with column-level ADC b) Column-level single-slope ADC architecture

III ANALOG COLUMN CIRCUITRY

A. Comparator input circuitry

As explained in section I, the output of the front-end consists of two voltages that are stored on sampling capacitors. These voltages should be subtracted and the result should be fed into one input of the column comparator, while a ramp voltage should be applied to the other input. In fig. 3, two column circuits are shown that implement the required subtraction. In both circuits, the current source that biases the front-end is omitted for clarity; this current source is connected to the input in both cases. In fig. 3a, a fully differential approach is shown [5, 7]. Signal and reset voltages are sampled consecutively onto capacitors C1 and C2 by closing switches S1 and S2, while the ramp generator outputs a reference voltage. After this sampling phase, a differential ramp voltage ($V_{ramp1} - V_{ramp2}$) is applied. This differential ramp voltage will compensate for the differential voltage on the capacitors that is initially present on the input of the comparator. The comparator will trigger when the ramp voltage equals the differential voltage across the capacitors.

Fig. 3b shows a single-ended approach [4]. First, the signal is sampled onto capacitor C2 via switch S1 while switch S3 is also closed. As a result, both the signal voltage and the offset voltage of amplifier A1 are stored on capacitor C2. Next, switch S3 is opened and switch S2 is closed, after which the reset voltage can be sampled on capacitor C1. Finally, switch S1 is opened and the ramp voltage is applied via S2. Since C1 and C2 are now connected in series with the ramp, signal and reset

voltages are subtracted from each other and from the ramp voltage.

While the circuit of fig. 3a has the potential advantage of higher noise immunity because of the differential circuit used, this advantage is probably limited as the actual sensor front-end is fundamentally single-ended in nature. The circuit of fig. 3b on the other hand has the advantage of combining both offset cancellation of the first comparator stage with signal sampling. As capacitors will usually consume most chip area in the analog column circuit, this combination can save a considerable amount of chip area.

B. Comparator topology

Since the required ADC resolution is usually around 10-12 bits and the full-scale voltage is about 1V, the LSB voltage step will be several hundred μV . The comparator should provide enough gain to amplify this voltage to drive a digital gate. Therefore, it should provide a gain of 60-80dB. Because of the low power consumption required, a multi-stage open-loop configuration is commonly used. There are two classes of circuits available to implement the comparator stages. Firstly, simple, linear gain stages, consisting of input differential pairs with a load can be used. The maximum gain such a stage can provide is about 40dB, requiring 2 or 3 stages to ensure enough gain over process corners. This is shown in fig 3b, where A1 and A2 are both linear gain stages.

Secondly, regenerative latch circuits can be used. These circuits, sometimes also known as *clocked comparators*, use positive feedback by cross-

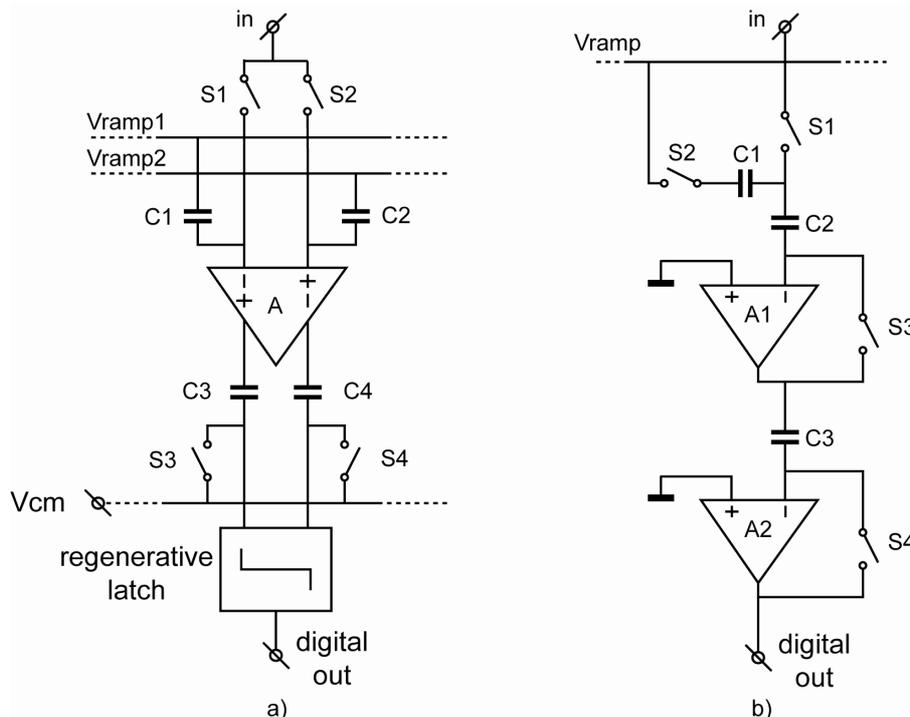


Figure 3 Examples of column circuit topology: a) Differential circuit taken from [5] and [7] b) single-ended circuit topology, taken from [4]

coupling one or more pairs of transistors. Regenerative latch circuits have the advantage of a higher gain-to-power consumption ratio, which can lower overall power consumption. The disadvantage of these circuits is the potential for clock feed-through into the signal path. In particular, they can inject charge back into their inputs at the clock edge. Therefore, if a regenerative latch would be directly connected to the central ramp voltage, it can lead to interference between column circuits, severely degrading quality. To prevent this, a gain stage has to be placed in front of the regenerative latch. In fig 3a, a topology with this combination is shown. First, a linear gain stage A is used, followed by a regenerative latch.

Unfortunately, since most of the research in the field is done in the industry, very few details about comparator circuits have been published. Details of a comparator design made by the authors can be found in [7].

C. Comparator offset and delay

As discussed in the previous section, comparator offset is the main source of non-uniformity between different columns. Since the long, narrow layout required leads to small transistors, and thus, relatively poor transistor matching, the static offset of the comparator will be too high. Therefore, a dynamic offset cancellation technique is required. Since the input signal is already sampled, the auto-zero technique is exclusively used to reduce the input offset of the comparator. If linear gain stages are used, a circuit-auto-zero can be implemented by adding a capacitor to the input or output of the gain stage. In fig 3a, the gain stage A has auto-zero capacitors at its output. By closing switches S1 through S4, the input of the gain stage is shorted (via S1 and S2), and therefore its amplified offset appears at the output. Here, it is sampled by capacitors C3 and C4 through S3 and S4. In fig 3b, the offset is stored by capacitors at the input of each gain stage. As previously discussed, the offset of gain stage A1 is stored onto capacitor C2 together with the input signal. In similar fashion, the offset of gain stage A2 can be stored onto C3 using switch S4.

Apart from the analog auto-zero technique described above, a digital auto-zero is also possible [6,7]. By performing an A/D conversion with a fixed input voltage, we can store and subtract the offset in a digital domain. Since it is difficult to implement a circuit-level auto-zero around a regenerative latch, a digital correction may be required when such a circuit is used.

A digital offset cancellation can also be used to compensate for the comparator's *delay*. In order to ensure a uniform response between column comparators, the delay of each comparator should

be uniform as well. However, this delay usually depends on process parameters, and can therefore vary by about 30%. Therefore, the comparator should be designed such that the delay is less than 3 clock periods, to keep *variation* in the delay between columns within one clock period. Alternatively, if digital offset correction is used, this offset correction can also compensate for the delay of the comparator. As a result, a higher comparator delay can be tolerated, which can lead to lower power consumption.

Finally, in [8] a different technique is presented that can reduce the effect of column non-uniformities. Rather than decreasing the non-uniformities itself, its visibility is reduced by switching each column ADC between different adjacent pixel columns. This spreads out column uniformities making them less noticeable. While it is still necessary to use auto-zeroing, this technique can be very useful to decrease any remaining offset after auto-zero is applied.

IV CONCLUSION

The column-parallel single-slope ADC architecture has evolved in the last years as the preferred solution for increasing the total readout speed of CMOS imagers. The architecture requires only a very simple analog comparator for each ADC channel, reducing chip area, power consumption and uniformity problems. Recent publications show that this architecture is capable of reading out high-resolution CMOS image sensors in a power-efficient manner.

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