

Fixed-Pattern Noise Induced by Transmission Gate in Pinned 4T CMOS Image Sensor Pixels

Xinyang Wang, Padmakumar R. Rao, and Albert J.P. Theuwissen
Department of Microelectronics/DIMES, Delft University of Technology,
Delft, The Netherlands
Xinyang.Wang@tudelft.nl

Abstract—In this paper, we present the characterization and analysis of fixed-pattern noise (FPN) in CMOS Image Sensor (CIS) pixels fabricated in CMOS 0.18- μm process. The experimental results demonstrate that the dark signal degradation of pinned 4T CIS is mainly due to the dark current generated from the transmission gate (TG) instead of the photodiode (PD). From our investigations of gate voltage / charge transfer time – dark current characterization and temperature dependencies, we found that hot-carrier (H-C) induced impact ionization and trap-induced leakage current are the main mechanism of sensor performance degradation.

I. INTRODUCTION

CMOS image sensors have gained great interests in the applications of still imaging, e.g. digital camera, scanning devices, etc. They benefit from low power, low cost and high integration. However, FPN due to pixel dark current is still one of the essential issues regarding sensor performance. Reducing FPN will help to enhance the signal-to-noise ratio and reduce the amount of ‘hot pixels’.

In the history of CIS FPN research, different noise sources have been extensively studied. The implementation of correlated double sampling (CDS) on 4T active pixel sensor (APS) effectively eliminates FPN caused by device mismatch and reset transistor. From then on, the FPN is mainly due to pixel-level dark current. The pinned 4T APS structure is now widely used because of its capability of minimizing dark current generated by silicon-oxide interface defects in PD region [1]. However, because of the scaling of CMOS process, new ‘sub-micron’ FPN sources have emerged. A recent study of pinned 4T imagers made in 0.18- μm CMOS process showed that the edge/sidewall of shallow-trench-isolation (STI) generates enormous dark current, which is collected to the PD. The solution is to fabricate a p^+ layer surrounding the STI to ‘pin’ the sidewall [2].

To get a good insight of the FPN in sub-micron CIS, we studied the dominating FPN source with different test structures fabricated in Philips’ 0.18- μm CMOS imaging process. We found that if the STI is well ‘pinned’, the dominating FPN does not depend on the integration time

but on the charge transfer time, i.e. the time duration for which the transmission gate (TG) transistor is turned on. From our simulation and measurement, for the first time, the TG region, which is normally considered noise free, is observed and studied. We concluded that the majority dark current generated during charge transfer is due to H-C effect, which is induced by the strong electrical field at the TG-PD overlap. In section II, we present the simulation of this H-C mechanism. In section III and IV, we analyze and discuss the results of the sensor characterizations. Finally, conclusions are drawn in section V.

II. PIXEL STRUCTURE AND SIMULATION STUDY

A. Pixel Structure

The structure of a pinned 4T CIS pixel and the device cross section of TG transistor are shown in Fig.1. The pixel contains three standard n-type MOSFETs: reset transistor (RST), source follower (SF) and row select (RS). The pixel output (V_{out}) is connected with the column current source and the CDS circuitry. The TG transistor is a “special” transistor. As shown in Fig.1, its “source region” is the pinned PD, where the whole n^- region is floating underneath a heavy p^+ doping pin layer. Due to the self-aligned doping process, there is approximately 0.2 μm overlap between this pinned layer and the TG gate in our sensor. The “drain” side is the floating diffusion (FD), to which the electrons are transferred and converted into voltage signal.

B. Simulation Study of Charge Transmission Region

The TG transistor is simulated by MEDICI for charge

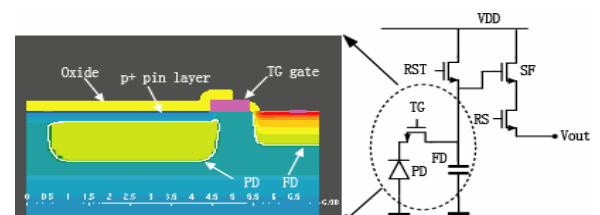


Figure 1. Diagram of 4T APS and cross section of TG transistor

This work is sponsored by Dutch Technology Foundation STW project DSC5869 and Philips/DALSA BV for test structure.

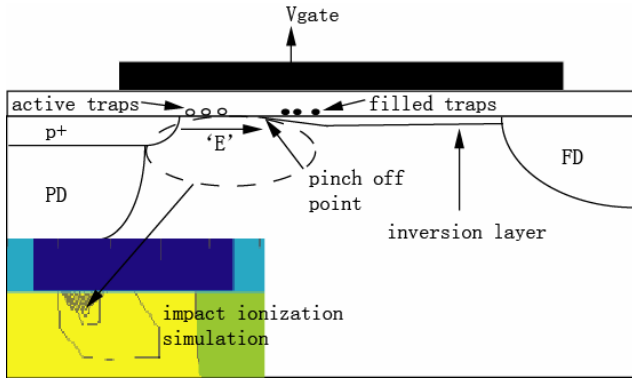


Figure 2. TG cross section and impact ionization simulation

transfer. The process simulator TSUPREM is used to generate the device structure. Before charge transfer, the potential of FD is reset by the RST transistor to VDD. A positive voltage is then applied to the TG gate to transfer the photon generated electrons from PD to FD.

As shown in Fig.2, during charge transfer, the positive V_{gate} creates a strong inversion layer along the interface of silicon-oxide underneath the gate. This inversion channel pinches off because of the heavy doping of p^+ layer near the gate-PD overlap. A strong electrical field is then developed due to pinch-off. The maximum lateral electrical field is approximately given by the voltage drop along the pinch-off region. It is simulated with respect to different TG gate voltages and FD reset voltages in Fig.3. Increasing gate voltage causes the pinch-off point to move towards the PD side because of the doping gradient. Thus, the maximum electrical field increases. Eventually, the gate voltage can not further extend the strong inversion region. The maximum electrical field will then saturate.

As shown in Fig.3, when the FD voltage is as low as 2V, the maximum lateral electrical field along the channel reaches more than 3×10^5 V/cm, which is strong enough to induce H-C effects [3]. As a result, some of the photon-generated carriers from the PD will gain enough kinetic energy and turn into “hot carriers” by the high electrical field during the charge transfer. Those “hot carriers” can hit the silicon-oxide interface, rupture Si-H bonds and create stress and fast interface traps. Because of the high trap density and stress located in the channel interface, trap-induced dark current I_{ti} increases too, which is given as:

$$I_{ti} = qn_i(\sigma_s v_{th} \Delta N_{it} / 2) \quad (1)$$

Where q is the magnitude of electronic charge, n_i is the intrinsic carrier concentration, σ_s is the effective capture cross-section, v_{th} is the thermal velocity and ΔN_{it} is the interface trap density. This trap-induced current mainly depends on the active trap density. The amount of active

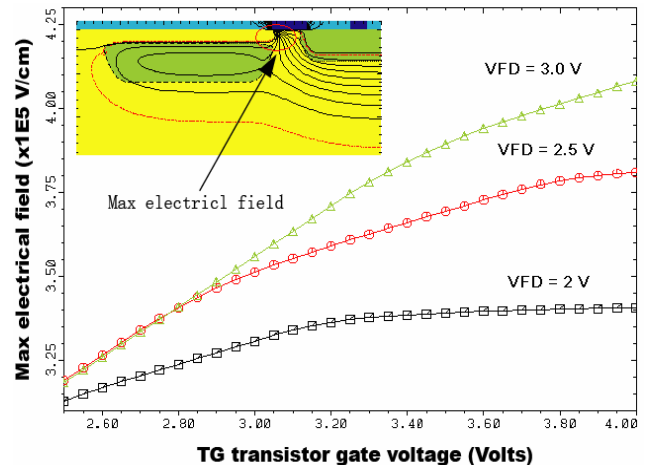


Figure 3. Maximum lateral electrical field Vs. TG on voltage and FD reset voltage (VFD)

traps is reduces with increasing of TG gate voltage because the extended inversion layer will fill the interface traps and deactivate them [4].

The trap-induced excess carriers act as the source of impact ionization, which generates more excess carriers. The simulation of impact ionization leakage current at the channel region is also shown in Fig.2. It is clear that the impact ionization occurs at the location, where the lateral electrical field is the maximum. Therefore, the total dark current generation rate is mainly due to the electron-hole generation rate G_A from impact ionization process, which is given as [5]:

$$G_A = \alpha_n I_{ti} / q \quad (2)$$

Where α_n is the impact ionization rate for electron, which is strongly dependent on lateral electrical field.

III. DEVICE FABRICATION AND CHARACTERIZATION

A. Device Fabrication

Test structures made in Philip's 0.18- μm CMOS imaging process are used to measure this TG induced FPN. To address and distinguish between different FPN sources, eight regions with different pixel structures are made in one chip, as shown in Fig.4. Each Region consists of 128x341 pixels with the same pixel pitch of 3.5 μm x 3.5 μm . In Fig.4, the pinned STI structure stands for the p^+ layer around STI. The thickness of this layer is 0.2 μm if it exists. The term NTA stands for the distance between STI and n^- of PD. TG stands for the length of TG gate from layout. A thick oxide process is used with maximum power supply of 3.3V.

B. Measurement Setup and Consideration

With the help of a computer and a frame grabber, it is possible to address each individual pixel and record its output from thousands of continuous frames. The pixel

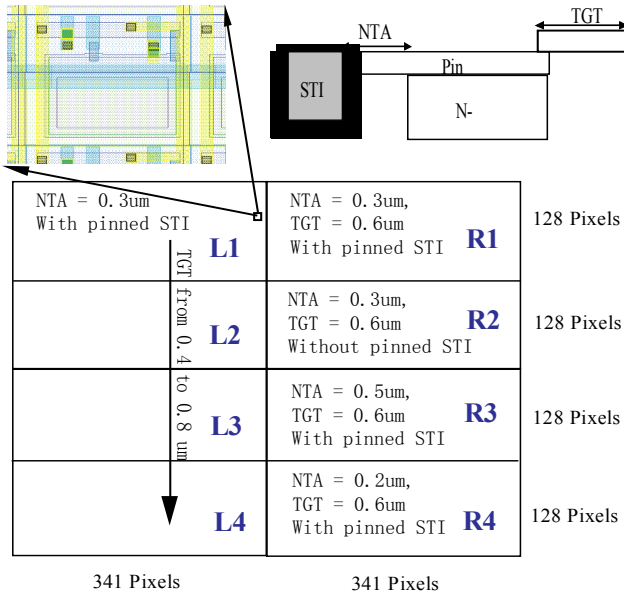


Figure 4. Chip structure and pixel layout

dark signals in our measurement are taken by averaging the pixel output of one hundred continuous frames, thus minimizing the random noise. Through the measurement, VDD of the pixel is set to 2V to minimize well-known H-C effect from SF transistor. CDS is used to eliminate offset because of device mismatch and reset noise. Hard reset is used to acquire good output swing.

C. FPN Measurement and Characterization

1) *FPN due to charge transmission:* Dark signals with various integration times are measured in all pixel structures to observe if the dominating FPN comes from the PD. We found that if the STI is pinned, the exhibited FPN of dark signal is independent with integration time. Fig.5 shows the dark signal histogram of pixels in region L1, with and without charge transfer. The mismatch of two

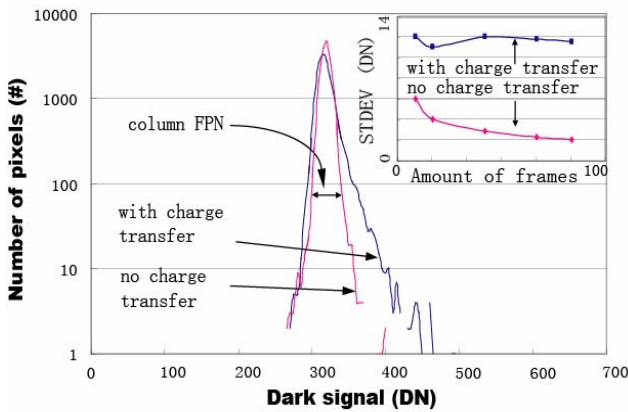


Figure 5. Measurement of dark signal in region L1

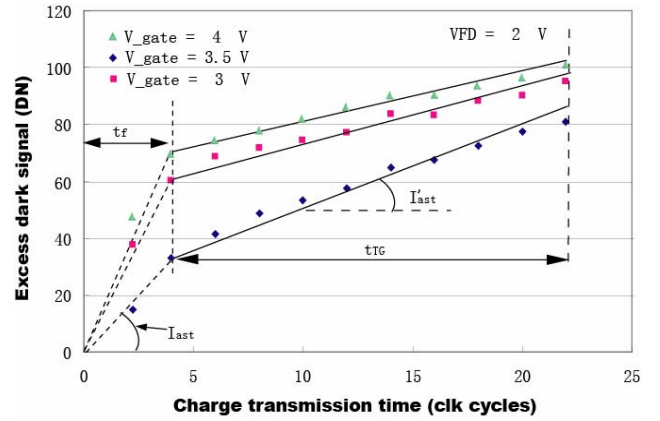


Figure 6. Dark signal dependency of different TG gate voltage and charge transmission time

histograms suggests that by switching the TG transistor on and off, a new FPN source is introduced. To eliminate the influence of column FPN, standard deviation of dark signal from pixels belonging to the same column is plotted. It is shown that if there is no charge transmission, the standard deviation obeys:

$$\sigma_1 / \sigma_2 = N_2 / N_1 \quad (3)$$

Where σ is standard deviation and N is the amount of sample frames. That is to say, the difference among dark signals of pixels in one column is mainly due to random noise, e.g. $1/f$ noise of SF. By averaging more frames, this difference decreases. On the contrary, in the case of with charge transfer, the standard deviation stays the same, independent of the number of sample frames, which strongly confirms the existence of TG introduced FPN.

2) *Dark current dependency of TG gate voltage and charge transmission time:* In order to further investigate the mechanism of this FPN, we studied the dark current dependency of TG gate voltage and charge transmission time, as shown in Fig.6. There is a clear “turn-point” for all TG gate during the measurement. Fig.6 is labeled with t_f and I_{ast} , i.e. the time and dark current generation rate before this point, t_{TG} is the time afterwards and I'_{ast} is the dark current generation rate during t_{TG} .

Before the turn-point, it is shown that t_f is actual the time required for the TG pulse to be stabilized, inversion to form and interface traps inside inversion to be filled. Thus, during this period, almost all the interface traps are active, independent of TG gate voltage. From (2), the dark current generate rate is then equal to:

$$I_{ast} = qG_A = \alpha_n I_{ti} = Ae^{B \cdot E(V)} I_{ti} \quad (4)$$

Where α_n is replaced by the exponential dependency of maximum lateral electrical field $E(v)$ [6], which is decided by TG gate voltage. A and B are constants for impact ionization process. As shown in (4), difference of

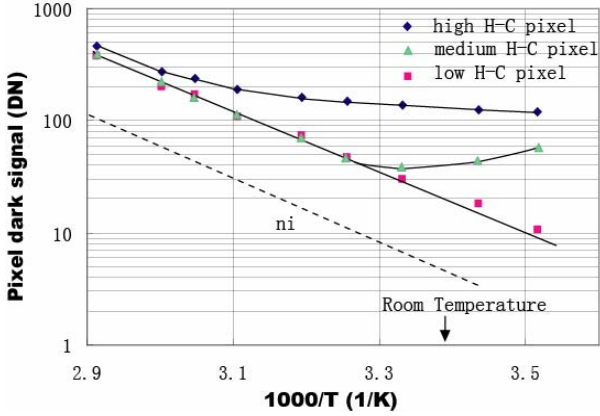


Figure 7. Temperature dependency of pixel dark signal

I_{ast} is only due to lateral electrical field. After the turn-point, the traps located in the inversion layer are filled up; the dark current generation rate can be written as:

$$I'_{ast} = qG_A = Ae^{B \cdot E(V)} I_{ii}(V) \quad (5)$$

As seen from (4), the trap-induced current I_{ii} in (5) depends on the TG gate voltage. Therefore, shown in Fig.6, in case of high gate voltage, even though the lateral electrical field is stronger, the amount of remaining active traps is less; overall, the actual dark generation rate is lower. Therefore, the total excess dark signal output during the whole charge transfer stage can be written as:

$$V_{total} = I_{ast} t_f + I'_{ast} t_{TG} \quad (6)$$

3) *Temperature dependency*: To verify the H-C mechanism, a temperature-varying experiment is conducted for pixels with high, medium and low TG introduced FPN. In Fig.7, it is shown that for low H-C pixel, the temperature dependency of dark signal is exactly the same as that of n_i , which can be written as:

$$n_i = C(T/300)^{3/2} \exp(-E_g / 2kT) \quad (7)$$

Where E_g is energy bandgap. C is a constant. This means thermal generation is the main mechanism of dark current in low H-C pixel. For both medium and high H-C pixels, junction leakage is also dominating at high temperature. Furthermore, for high H-C pixels, decreasing temperature leads to slight reducing of dark signal. This is because the trap-induced current reduces at lower temperature due to the smaller thermal trap-induced current. For medium H-C pixels, it is the impact ionization current mechanism which is shown. The increasing of dark signal at lower temperatures is an evidence of H-C degradation.

IV. DISCUSSION

The reported H-C effect of TG transistor causes degradation of sensor performance and lifetime. At present, it is possible to optimize this TG induced FPN by adjusting the TG gate voltage and the charge transmission

time. However, the penalty we pay is the increase of image lag because of lower TG gate voltage and shorter transfer time. In a pinned 4T APS design, it is very difficult to eliminate the lateral electrical field at the PD-gate overlap. One of the possible solutions for this problem may come from the road we are always following: to 'pin' the interface traps, e.g. by applying negative voltage on TG gate during exposure, holes from p^+ layer are attracted to the interface and fill the traps. In the short charge transmission period, the traps may stay filled; therefore, trap-induced current is reduced.

Scaling down CMOS process does not favor in this case as well. This mechanism will become more serious with shrinking of device dimension because of the increasing electrical field. Furthermore, with reducing pixel pitch, the separation between the stressed TG transistor and pixels nearby reduces. Hot carriers can travel to the PD of nearby pixel, and therefore introduce pixel crosstalk.

V. CONCLUSION

The model of TG induced dark current in pinned 4T APS is developed and experimentally verified by characterization and measurement of test structures fabricated in 0.18- μm CMOS process. From our results, it is shown that the overlap between the heavy doped p^+ layer and the TG gate introduces a strong lateral electrical field, which causes impact ionization and creates more interface traps. The trap-induced dark current and impact ionization leakage current are the main mechanism of this dominating FPN in our test structure.

ACKNOWLEDGMENT

The authors would like to thank their colleague M.F.Snoei from TU Delft and A.Mierop, W.Maes from DALSA BV for the helpful technical discussion and supplying the simulation data.

REFERENCES

- [1] R.M.Guidash, et al. "A 0.6- μm CMOS pinned photodiode color imager technology" IEDM Tech. Dig., pp. 927-929, 1997.
- [2] Hyuck In Kwon, In Man Kang, Byung-Gook Park, Jong Duk Lee, Sang Sik Park and Hyuck In Kwon, "The analysis of dark signals in the CMOS APS imagers from the characterization of test structures" IEEE Transactions on Electron Devices, vol.51, pp. 178-184, Feb 2004.
- [3] Ching-Chun Wang and Sodini, C.G "The effect of hot carriers on the operation of CMOS active pixel sensors" IEDM Tech. Dig., pp. 5.3.1 – 5.3.4, Dec 2001.
- [4] S.S.Chi et al. "Photonic gated-diode method for extracting the energy-dependent and the spatical distribution of interface states in MOSFETs" Journal of the Korean Physical Society, Vol. 43, pp. 884-891, Nov 2003.
- [5] S.M.Sze, Semiconductor Device Physics and Technology, 2nd ed., JOHN WILEY & SONS, INC, 2002, pp. 79-80.
- [6] N.V.Loukianova, et al. "Leakage current modeling of test structure for characterization of dark current in CMOS image sensors" IEEE Transcation on Electron Devices, vol.50, pp. 77-84, Jan 2003.