Fast Hartmann–Shack Wavefront Sensors Manufactured in Standard CMOS Technology

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***Abstract*—This paper discusses the implementation of fast wavefront sensors based on the Hartmann–Shack method in standard complementary metal–oxide semiconductor (CMOS) technology and evaluates the impact of the capabilities and limitations of this technology on the wavefront sensor performance. Aiming at fast operation ($>$ 1 kHz), we compare the applicability of either conventional or dedicated image sensors and investigate how current custom concepts can complement each other. To date, three different custom CMOS-sensor layouts have been implemented. Besides being able to operate at faster rates than conventional sensors, these devices demonstrated the ability to achieve high wavefront-detection accuracy and the potential for use in low-light applications (e.g., ophthalmic diagnostics). The goal is to identify the most important practical issues related to using standard CMOS technology in wavefront sensing.**

***Index Terms*—Adaptive optics, complementary metal–oxide semiconductor (CMOS) technology, image sensor, optical profiling, very large scale integration (VLSI), wavefront sensor.**

I. Introduction

WAVEFRONT SENSORS are used for the dynamic estimation of wavefront distortions, both in stand-alone setups for optical diagnostics and in adaptive optical systems for the compensation of optical aberrations [4]. These distortions can be induced either by a component profile or by variations in the light propagation media. The application fields range from astronomical and scientific to medical and commercial, with an increasing demand for affordable and compact devices. The target accuracy of wavefront reconstruction is indicated with respect to the wavelength (λ), which usually lies within the visible and near infrared spectra. The demanded accuracy varies across applications and must sometimes be smaller than $\lambda/100$ for the diagnostic of prime optical profiles or as large as $\lambda/2$, for coarse estimations of aberrations with large amplitudes ($> \lambda$) and low spatial frequencies, as often encountered in human eyes. Fast wavefront sensing is demanded where the optical aberrations fluctuate at a rapid pace because of, for instance, atmospheric turbulance during sky observation or optical data transmission, eye movements during *in vivo* retinal imaging, and axial spinning during the quality inspection of industrial parts.

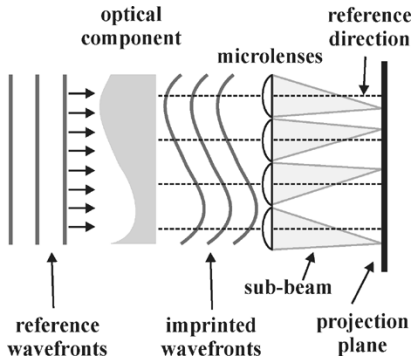

Fig. 1. H–S method, in which the spot displacements on the projection screen represent the incoming arbitrary wavefront.

The Hartmann–Shack (H–S) method is one of the most used wavefront sensing techniques; it is structurally simple and white-light compatible, it prompts straightforward data analysis and it has no 2π-ambiguity limitation, as is the case with most interferometers. In the H–S technique, a microlens array samples an arbitrary wavefront and the light spots at the projection screen deviate from a reference grid according to the local slopes of the wavefront. Essentially, this method enables one to estimate the wavefront shape from the displacements of light spots. Fig. 1 depicts the principle.

In optical shop testing, variations on this principle include, for example, laser-ray tracing (LRT), in which a single laser beam scans an object under test at particular grid points and the inverse Hartmann test, in which small optical fiber heads project a few beams on the object surface, whose deviations upon reflection indicate the object quality.

The projection screen in a H–S sensor is conventionally a camera, which represents a bottleneck to fast operation. Inexpensive off-the-shelf cameras offer limited frame rates usually reaching up to only 150 Hz. High-speed units, operating at frame rates of several hundred Hz or more, are mostly used for scientific applications and require a number of extra fabrication steps and architectural changes, which altogether push the costs up. In the H–S method, one is ultimately interested in the positions of light spots, and the grabbed camera image is solely an intermediate

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step. Therefore, the relatively slow image-processing step to perform the "centroiding" calculations combined with a restricted camera frame rate limit the overall sensor speed. This suggests the development of a custom layout in order to ensure operation at high repetition rates. As an alternative to the conventional camera, one can implement fast H–S wavefront sensors based on an array of optical position-sensitive detectors (PSD) integrated on a single chip, where each light-spot centroid is sensed by a particular PSD.

For custom PSD designs with their appended circuit blocks, charge-coupled device (CCD) technology does not qualify as the first choice. Despite being robust for imaging applications and suitable for very low light levels, this technology is often proprietary and has restricted digital and analog functionality. Complementary metal–oxide semiconductor (CMOS) is a more enticing technology, as flexibility and manufacturing costs are concerned, offering the possibility to integrate photodetectors and reliable analog-digital circuitry together. The steadily growing interest in CMOS devices promotes continuous research and process improvements, rendering a good match between simulated and implemented circuitry. Standard CMOS is a generic and largely accessible process which favors the integration of multiple electronic functions with a high yield and intrinsically enables the implementation of several photosensitive structures. CMOS imaging is a growing niche that complements that of CCD imaging by offering extended embedded functionality on chip.

II. Standard CMOS Technology

The ongoing trend in CMOS technology is the increase in circuit density and speed, and consequently, the reduction of the minimum transistor gate length. Feature sizes from 0.8 down to 0.13 μm are widely established industry standards today and the state-of-the-art manufacturing for logic circuits is 90 nm; offline processes reaching features as small as 65 nm have been investigated.

CMOS is not optimal for photodetection, especially in a standard flow chart. There are no pinned and buried layers to minimize dark current and substrate interference, respectively; multiple charge-packet transfer is not efficient due to the fixed doping profiles and also due to the absence of overlapping polysilicon layers in some processes. Also, in a standard fabrication line, even 10-nm fluctuations, from batch to batch, in the thickness of some dielectric layers on top of silicon lead to unpredicatable antireflective characteristics, considering the number of thin films stacked.

As the trend migrates to submicron features, the disadvantages to photodetection increase, because in such processes the *p-n* junctions that form photodiodes become shallower and the doping becomes higher, resulting in thinner depletion layers. These two factors lead to a lower quantum efficiency for longer wavelengths (> 600 nm). The introduction of silicided drains/sources, to increase speed, as well as silicided polysilicon layers impairs the penetration of incident light. Moreover, the reduction of the supply voltages—and the disproportional scaling of the threshold voltages—constrain the signal swing, which, in the analog-signal domain, can be detrimental. Besides, the fabrication costs for state-of-the-art processes increase drastically making them less convenient for small-scale custom devices and the behavior of novel circuitry becomes less predictable because of insufficiently accurate model parameters due to additional physical phenomena affecting transistor operation.

Recently, CMOS imagers with claimed high image quality have been reported [5], [6]. They often use either four-transistor active pixels or customized steps with well-defined local doping profiles and highly doped layers pinned to the substrate, or a combination of those.

III. CMOS H–S Wavefront Sensor

For a H–S wavefront sensor, two different approaches using CMOS technology can be considered: a camera or a matrix of PSDs. The basic difference between them is that a camera has a limited frame rate and requires image processing, whereas a matrix of PSDs (in which each PSD is associated with a light spot) enables almost direct information about the spot position and circumvents any image processing.

A. CMOS Imagers

A two-dimensional (2-D) imager consists of a densely packed array of adjoining pixels, whose main purpose is to capture an image by mapping a scene into a discrete distribution of light intensities. Obviously, a higher pixel density yields a better image reproduction. In a H–S wavefront sensor, the camera is used to register a picture of the light spots projected with the microlens array. Each microlens is associated with a region on the chip, i.e., with a certain number of pixels $N \times N$, over which the spot is free to move without overlapping with the neighboring ones. The effective focal spot illuminates yet a smaller number of pixels, say $n \times n$, within that delimited region. One calculates the baricenter of the focal spot by using a simple centroiding (center of mass) formula or a precalibrated curve-fitting algorithm, which minimizes the discretization error. In both cases one can achieve subpixel resolution, which increases with the number of illuminated pixels $n \times n$ and with the array fill factor. The fill factor is the ratio between the effective photocollecting area and the total exposed area, including gaps between pixels, circuitry, and interconnections.

In the development of a Hartmann sensor, one should find an optimal compromise between the ratio of the spot size to the pixel size and the ratio between the microlens diameter and the spot size. The first ratio affects the resolution of the centroid calculation and the second ratio dictates the lateral range the spot is able to move (i.e., the maximum local wavefront tilt). The largest possible ratios are desirable, but practical limits are set by the choices of imaging-chip dimensions, pixel size, and parameters of the microlens array (lateral size, pitch, fill factor, and focal length). Conventional chip dimensions extend up to 15 mm and physical pixel sizes range from 5–20 μm, typically. The maximum spot displacement depends on the focal length of the microlenses and on the magnitude of the wavefront aberrations. For a H–S wavefront sensor, color cameras are not recommended because many chips for color imaging have a dis-

tribution of color filters on top of their pixels, which introduces nonuniformities to the intensity reponse.

The wavefront accuracy of the H–S sensor is directly associated with spot centroiding resolution, which is determined by several noise sources, including intrinsic pixel noise, spatial discretization, readout noise, signal-conversion quantization, imaging-chip architecture, and temporal noise.

Intrisic Pixel Noise: It basically comprises dark-current shot noise, thermal noise, pixel response nonuniformity due to process variations over the array, transistor threshold voltage mismatch, and signal-transfer or reset noise (often referred to as kTC noise). The response nonuniformity and the threshold voltage mismatach add together as fixed-pattern noise (FPN), which is observed as a difference in response between pixels in an array which have been submitted to fabrication with identical layouts. If active pixels are used—where a buffer MOSFET copies the photodiode signal to the data line—FPN and kTC can be supressed by double-sampling readout. The dominating intrinsic noise source depends on the choices of photodetection element and on the pixel circuitry.

Spatial Discretization: It derives from the pixalated nature of an imaging chip and its effects can be minimized by having as many possible pixels illuminated by the spot. In practice, at least 5×5 pixels should be illuminated.

Readout Noise: It derives from the current-to-voltage conversion and amplification circuitry and consists frequently of $1/f$ noise (flicker noise), thermal noise, and signal offset. For photodiode pixels, the transimpedance amplifier with a compensation shunt capacitor usually offers the best performance in terms of noise and bandwidth.

Signal Quantization: It occurs when the analog pixel signal is converted to a digital output and its *rms* value is given by the voltage associated with the least-significant bit divided by $\sqrt{12}$.

Architectural Noise: If photodetectors in an array are rectangular rather than square, they introduce a false contribution of astigmatism (cylidrical aberration) in the reconstructed wavefront, unless the image-capture hardware or a dedicated software routine purposedly mitigates this effect.

Temporal Noise: It is often associated with temperature variations and only becomes relevant if its change rate is higher than the wavefront change rate.

A number of important remarks need to be considered when selecting a CMOS imager for a H–S sensor.

Fill Factor: This dictates the amount of impinging light effectively being detected. Wavefront sensing in astronomy and ophthalmology can largely benefit from a high fill factor, provided the intensity levels available or allowed there are low. It is important to observe whether the CMOS chip has focusing microlenses deposited directly on chip, counteracting a possibly low fill factor.

Dynamic Range: CMOS cameras with a very high dynamic range usually make use of logarithmic pixels, which are inconvenient for spot-centroid detection because of the nonlinearity of the response. Several commercial cameras, however, offer the possibility to switch between the logarithmic and the linear modes.

Multiple Framing (Windowing): In some cameras, multiple framing is possible, where several subareas can be defined on the chip. This can be convenient to track individual spots, eliminating the readout of obsolete dark pixels. However, the sequential subframe readout and the switch time between frames slow down the operation. The number and position of spots required to sense a given wavefront aberration depend on the aberration spatial frequency and sometimes the incoming beam does not have a uniform intensity over the optical aperture. In these cases, full random access to pixels in the spatial and time domains can be useful. This could readily reject dark pixels, promote longer integration times exclusively for faint spots and increase the overal acquisition speed by reducing the number of pixels readout.

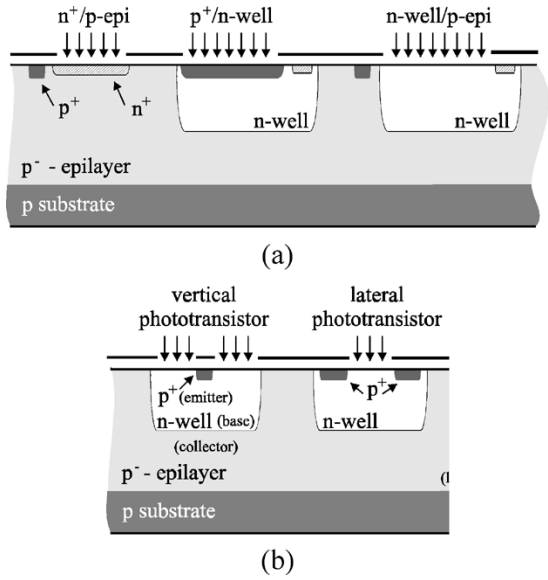

Fig. 2. Some photodetector structures available in standard CMOS technology. (a) Photodiodes. (b) Phototransistors.

Sensitivity: Most commercial CMOS imagers use the n^+*/p-substrate* photodiode (shallow junction), which enables a larger array density, but are more prone to substrate noise. Also, the closer the junction is to the surface, the higher is the contribution of dark-current shot noise and the lower the photocollection efficiency for longer wavelengths ($> 600\ \mu$m), on which most wavefront sensing application are based. High-speed cameras require additional custom fabrication steps and are often manufactured in state-of-the-art processes, for which the smaller feature sizes and the use of silicide layers result in shorter delays (larger operational bandwidth), but yields a lower sensitivity.

B. CMOS Chips With Optical PSDs

These chips comprise full custom designs for H–S sensors. Each design consists of a regular array of PSDs, signal-transfer and/or signal-processing electronics and digital control units (shift registers or demultiplexers). Photodiodes and phototransistors can be implemented in CMOS as depicted in Fig. 2, whereas some possible 2-D PSDs are shown in Fig. 3. The quad cell, alternating, chessboard-like, and spiral structures all yield the x and y coordinates of the light-spot centroid based on the relative photocurrents on rows and columns of photodetectors. The working principle of each of these structures and the performance of the respective implemented CMOS structures was given by de Lima Monteiro *et al.* [7].

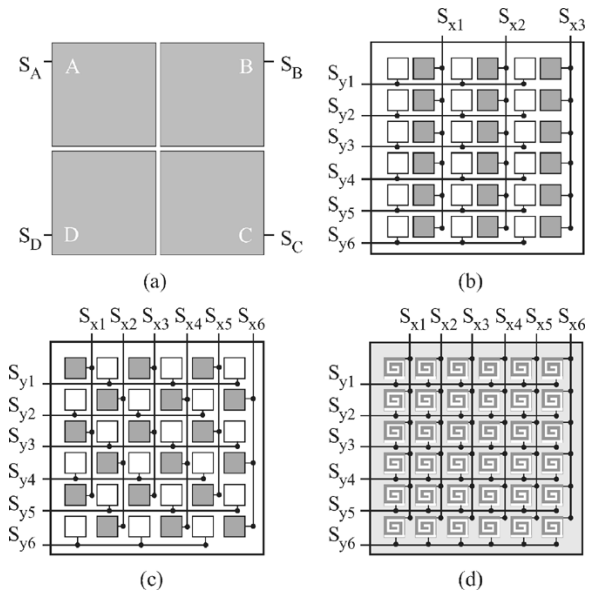

Fig. 3. Two-dimensional PSDs. (a) Quad cell. (b) Alternating. (c) Chessboard-like and (d) spiral structures.

The main advantage of using PSDs is the nearly direct information about the positions of the spots, rendering image processing unnecessary. The three design approaches presented here were fabricated and tested, and they differ from each other in the feature size of the CMOS process used, the type of PSDs chosen and the spot-detection scheme (Fig. 4).

An overview of the technology, layout and circuit parameters for the three implemented CMOS chips is shown in Table I.

The HSSX chip is based on alternating photodiode structures, where the output signals of rows and columns are connected to input nodes of x and y circuit chains, respectively. Each chain contains as many circuit cells as there are rows (or columns). The cells are arranged in a winner-take-all structure (WTA) [8], which generates a high digital output solely to the output node corresponding to the input node with the highest photocurrent. After every millisecond the state of all PSDs is reset. The binary data is then transferred, in daisy-chain architecture, to a data compressor unit for subsequent readout. The PSDs, which detect the position of the largest photocurrent, are linear over the whole dynamic range. The chip features no random access to the individual detectors.

The CeHSSA chip is an enhancement of the previous structure. It uses n-well/p-epilayer photodiodes in a chessboard-like arrangement and a novel topology for the WTA circuit. The lower-junction photodiodes feature capacitance values one order of magnitude lower than the upper-junction photodiodes and the novel WTA architecture is based on several independent and interleaved WTA chains, yielding the possibility of pseudo-centroiding because of the availability of several maxima. After addressing a detector, its data is stored in an internal tristate bus for subsequent parallel or 16-bit multiplexed readout.

The QC-WFS chip features 8×8 quad cells with double-junction photodiodes (p+/nwell and nwell/p-epilayer). An integrated demultiplexer enables random access to the quad cells. The analog output yieds true centroiding, and although the position response is nonlinear, one can characterize it with a sigmoidal function in a precalibration step. The quad-cell signals

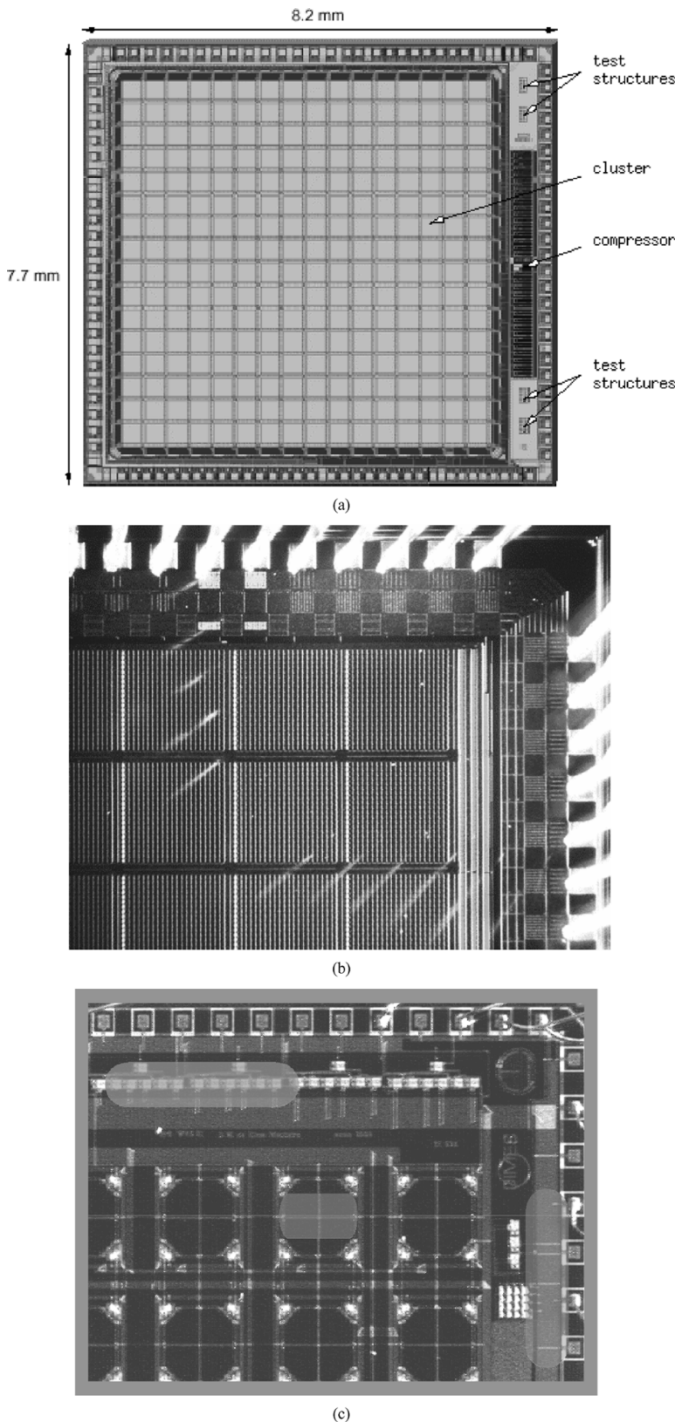

Fig. 4. Photographs of the three implemented chips. (a) HSSX. (b) CeHSSA. (c) QC-WFS.

are multiplexed and delivered to an outup data bus. The geometrical arrangement of a quad cell allows both spot-centroid detection and spot centering. The first is convenient when the sensor is used in diagnostic applications and the latter when it is used to drive a deformable mirror in an adaptive optical system.

IV. Performance of the Custom CMOS Chips

Operational speed, wavefront-sensing accuracy (the minimum *rms* wavefront variation the sensor is able to detect), and light sensitivity are the most important parameters. They all

TABLE I
LAYOUT AND CIRCUIT PARAMETERS OF THE IMPLEMENTED CMOS WAVEFRONT SENSORS

Sensor	Heidelberg 1 (*HSSX*)	Heidelberg 2 (*CeHSSA*)	Delft (*QC-WFS*)
technology (feature size)	AMS 0.6 μm, n-well, double poly, double metal	AMS 0.35 μm, n-well, double poly, double metal	DIMES - 1.6 μm, n-well single poly, double metal
chip size	7.7 mm x 8.2 mm	4.1 mm x 4.1 mm	10 mm x 10 mm
photodetector	17.6 μm x 17.6 μm pixels *p+/ n-well*-photodiodes	17.0 μm x 17.0 μm pixels *n-well/p-epilayer*-photodiodes	300 μm x 300 μm pixels, double-junction photodiodes (p^+/*nwell/p-epilayer*)
PSD layout	alternate structure, 19x19 pixels each (400 μm x 400 μm)	chessboard-like, 21x21 pixels each (400 μm x 400 μm)	quad cell, 2x2 elements (600 μm x 600 μm)
Array	16x16 PSDs (orthogonal)	8x8 PSDs (orthogonal)	8x8 PSDs (orthogonal)
Circuitry	Winner-Take-All circuit + daisy chain data transfer and data compression	resistive network of Winner-Take-All circuits + internal tristate data bus and multiplexed binary output	passive analog switch set per pixel + demultiplexer
spot detection	peak photocurrent, P>200 pW/spot	pseudo-centroiding or peak photocurrent detection P>20 pW/spot	full spot centroiding
Readout	serial digital	16-, 32-, and 42-bit digital output modes	8 analog outputs

TABLE II
OPERATIONAL PARAMETERS OF THE THREE IMPLEMENTED CMOS WAVEFRONT SENSORS

Heidelberg 1 (*HSSX*)			Heidelberg 2 (*CeHSSA*)		Delft (*QC-WFS*)		
quantum efficiency		10% (680nm)	quantum efficiency	40% (680nm)	quantum efficiency		40% (630nm) 70% (680nm)
max. operational frequency		1kHz	max. operational frequency	4kHz	max. operational frequency		3kHz
position resolution/ wavefront accuracy		spot intensity	wavefront accuracy	spot intensity (λ =633nm)	position resolution/ wavefront accuracy		spot intensity (λ =633nm)
33 μm	λ/2	1 nW	λ/2	300 pW	10 μm	λ/10	2.5 μW
13 μm	λ/5	10 nW	λ/12	300 nW	5 μm	λ/20	4 μW
					1 μm	λ/50	10 μW

depend on a number of other core factors related either to the technology used or to the design choices.

The operational speed depends on the pixel capacitance, type of PSD and readout scheme. The wavefront accuracy is associated with the PSD position resolution, which depends on the noise of the photodetector and on the PSD layout. The sensitivity, which can be tagged as the overall quantum efficiency of the photodetector, depends on many factors, such as, for instance, the fill factor of each PSD, the thickness of the oxide and nitride layers on the chip, the doping profile, and the junction depth. Table II shows some performace parameters, followed by a discussion of each chip.

A. HSSX Chip

The position resolution is basically limited by the discrete nature of the PSD (alternating structure), where the pixel size is 17.6 μm, and by FPN, which depends on the spot size and on the frame rate. The WTA circuit is reset at the beginning of every frame. The WTA circuit needs a certain time to establish the output state and that time depends on the input photocurrents. At its maximum frequency, 1 kHz, the WTA circuit may not reach its final state for low light intensities, which results in a larger FPN. For very low intensities, a feedback mode has been implemented with increased bandwidth at the expense of increased position noise. The quantum efficiency of this chip was low (10%) due to a shallow-junction photodiode, especially for $\lambda = 680\ \mu$m, and misfortune in the combination of the thickness of the oxide layers, which were not optimized for optical transmission.

B. CeHSSA Chip

The influence of FPN was cancelled out to a large extent in this chip by using a modified topology for the WTA circuit. The larger quantum efficiency and the reduced parasitic capacitance also increased the bandwidth and the sensitivity. The position resolution above $\sim$ 100 pW per spot is mostly limited by the pixel size (17.0 μm). The sensor can, however, operate up to 4 kHz, and the wavefront accuracy can be as good as $\lambda/12$ ($\lambda = 633\ \mu$m) for 300-nW spots.

C. QC-WFS Chip

The position resolution depends on the process/pixel architecture through the signal-to-noise ratio. The quad cells are based on passive pixels, which consist of a photodiode connected to an analog switch. This architecture couples the large pixel capacitance (50 pF), due to the large photodiode size, to the capacitance of the data bus. The direct transfer of the photocurrent from this capacitor to the data line brings along a large contribuiton of kTC noise, which limits operation at low light levels. The spot position resolution can be as good

as 1 μm, for a 10-μW spot, resulting in a wavefront accuracy of $\lambda/50$ ($\lambda = 633$ μm). Reduction of this noise contribution is a promissing solution for operation at lower light levels. This chip is able to operate up to 3 kHz.

V. Discussion

A. Choice Between a Conventional Imager and a Dedicated Sensor

A generic H–S wavefront sensor should feature a large intensity dynamic range, markedly operable at low-light levels (pico- or nanowatts per spot), while suitable to aberration detection at frequencies larger than 1 kHz. Besides, in order to become widespread in medical and commercial fields, the unit costs should be limited to few thousand dollars, including sensor, sampling plane, and generic software. Also, the portability of the device and the ability to change the number of sampling points, focal plane distance and grid geometry are desirable. None of the devices implemented so far, either with a conventional or with a dedicated imaging chip, fulfill all those wishful requirements at once.

CCD-based sensors still offer the best performance in regard to low-light levels, and scientific CCDs, often cooled, have been deployed in astronomical applications. However, long integration times, sometimes of several seconds, are not uncommon. In terms of speed, fast CCD and CMOS cameras with frame rates in excess of 1 kHz have been developed, some of which are already on the market. The speed, nonetheless, comes at the expense of a reduced number of pixels, which limits the resolution in the computation of the centroid of light spots, or at the expense of a lower sensitivity. Data reduction of the image grabbed from a conventional camera represents an additional delay. CMOS cameras that offer the user full access to pixels can be used to emulate arrays of PSDs, by the division of the imaging array in subregions, skipping the readout of obsolete pixels and increasing speed. One of the great advantages of an imaging chip is the flexibility to use different layouts for the sampling-plane array (geometry and density of microlenses) and the absence of strict alignment requirements. For wavefront detection below 150 Hz, inexpensive and, yet, sensitive, off-the-shelf cameras are available.

Dedicated CMOS sensors based on PSDs are primarily aimed at high operational speed (> 1 kHz), without necessarily compromising the number of operative light spots or the sensitivity. Random access enables the reduction of the number of PSDs to be readout to further increase speed. Some disadvantages compared to a conventional camera are the requirement of precise alignment of the microlenses on top of the chip and the matching of the microlens grid to that of the PSDs. The compatibility with CMOS enables future integration of smart functions on chip without changing the core layout, offering the possibility of fully customized solutions at reasonable low-volume costs and the feasibility of compact sensors with integrated reconstruction algorithms and mirror drivers. Low-light level operation (nanowatt input beams) and good wavefront accuracy ($< \lambda/10$) at high speeds have been proven in independent chips and a combination of these quality parameters on a single chip have been investigated, as suggested in the following section.

Dedicated chips based on position-sentitive detectors could be fabricated in hybrid CCD/CMOS processes, benefiting from the efficiency of CCD and the circuitry functonality of CMOS, with the due extra costs for this additional process, however.

B. Directions for Future Improvement of the Dedicated CMOS Chips

The dedicated chip *HSSX* features high operational speed but does not offer random access to the PSDs. It has a very good light sensitivity (nanowatt range) but the position detection is based solely on the peak intensity of the spot, which limits the position resolution to the pixel pitch. The second chip (*CeHSSA*) represents an enhanced version of the previous one. It enables full random access, enhances the light sensitivity to the sub-nanowatt range, and improves the position resolution (wavefront accuracy) by using pseudocentroiding with multiple peak detections. It is also able to operate at 4 kHz in the centroiding mode. This sensor is suitable for low-light operation but the position resolution still limits its use to low-order aberrations with relatively large magnitudes. The third presented sensor (*QC-WFS*) offers full random access, very good position resolution (wavefront accuracy), but requires light levels in the microwatt range due to the high capacitive noise associate with the large photodiodes and the passive-pixel architecture. Both the *CeHSSA* and the *QC-WFS* chips still offer room for improvement, the first in terms of position resolution and the latter in terms of low-light operation.

The basic limitation of wavefront sensors based on the WTA circuit is the restricted resolution of the spot detection. The design goal with respect to sensitivity (~ 300 pW per spot) has been achieved. The practical limit for the minimum pixel size (and position resolution) in the chosen CMOS process technology is ~ 10 μm. Though in the static case the position resolution is limited to the pixel pitch, this limit can be passed under in the dynamic case, by adequate temporal post-processing of the spot position time series [9], e.g., through adequate Kalman or other filtering techniques. A spatial resolution well below the pixel dimension can be achieved and no different chip architecture is required. In addition, it would be useful to increase the functionality of the sensor by adding a modal wavefront-reconstruction module directly on the chip. A possible implementation would be a hardware artificial neural network [10], which could provide a direct analog output signal for some low order aberrations, like tilt, defocus and astigmatism, useful for modal wavefront correctors. This could result in miniaturized AO systems, which do not need a host computer.

For the chip based on quad cells (*QC-WFS*), the goal is to improve the light sensitivity of this sensor by three orders of magnitude (microwatt $\rightarrow$ nanowatt per spot), while maintaining a good wavefront accuracy ($\leq \lambda/10$). The main limitation is now capacitive noise (kTC). Several basic measures can contribute toward this improvement, still preserving the benefits of the quad-cell architecture and the supra-micron fabrication technology (1.6 μm): substitution of the double-junction photodiodes with *n-well/p-epi* photodiodes, of passive pixels with active pixels, and of simple transimpedance amplifiers with capacitive shunted ones. The junction substitution leads to a capacitance one order of magnitude lower; active pixels, which include a source follower and a reset transistor, ensure the decoupling of

the photodiode capacitance from the line capacitance and enable the cancellation of FPN and kTC noise; and a properly designed shunted amplifier reduces the amplitude of the noise spectral density within a frequency range of interest. These measures will also improve the sensor intrinsic frequency.

VI. Conclusion

CMOS-based wavefront sensors are growing mature and can be beneficial for a number of applications in industry and medicine, e.g., laser diagnostics, direct optical data links and ophthalmology. Off-the-shelf CMOS cameras can substitute the long-used CCD cameras for H–S sensors. However, the choice of an appropriate CMOS camera can be tricky; often, an improved speed performance comes at the cost of lower resolution and/or sensitivity. The most important advantages of CMOS technology is the capability to realize custom designs and the possibility of implementation of reliable digital and analog circuits as well as photosensitive elements on a single chip. The use of CMOS favors the development of custom wavefront sensors with embedded functionality.

The custom CMOS wavefront sensors developed so far are based on integrated matrices of PSDs. This approach enables a faster readout of the spot centroids and circumvents the need for an image-processing step, yielding frame rates in excess of 1 kHz. The sensors independently developed in Delft, The Netherlands, and in Heidelberg, Germany, have also shown that CMOS-based solutions can offer both a good resolution and a good light sensitivity. The challenge is now to combine these two characteristics on a single chip.

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