The Effect of Switched Biasing on 1/f Noise in CMOS Imager Front-Ends

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Abstract - **1/f noise is an important problem in CMOS imager front-end read-out circuitry. In the current generation of imagers based on 4T pixels, 1/f noise is the dominant source of read-out noise. As decreasing transistor sizes tend to increase the 1/f noise, we expect this noise problem to become worse in the future. In this paper, we present the effect of downscaling a transistor to deep submicron level on the 1/f noise. Furthermore, we will present a 1/f noise reduction technique known as switched biasing, and discuss its applicability to CMOS imager front-ends.**

I INTRODUCTION

In the recent past of 3T imaging pixels in CMOS imagers, the kTC or reset noise of the photodiode used to be the dominant random noise source. It typically limited the noise performance to about 30 noise electrons. As a result, relatively little effort had to be made in the front-end of the analog readout circuit to keep the noise levels at an acceptable level. However, with the development of 4T pixels, Correlated Double-Sampling (CDS) can be used to eliminate the reset noise. As a result, the noise performance of the front-end readout circuit has become much more critical.

The in-pixel source follower generates most of the noise of the front-end readout circuit. It exhibits two types of noise: thermal noise and 1/f noise. Thermal noise can be relatively well controlled by changing the size of the sampling capacitor. However, controlling the 1/f noise is a much more difficult problem.

Most of the noise reduction solutions used in conventional analog circuit design do not apply to CMOS imager front-ends. Firstly, increasing the size of the transistor is obviously not a solution for a transistor located inside the pixel. Secondly, although the application of CDS does partly cancel the 1/f noise, the CDS sampling frequency is too low in an imager, and a large portion of the 1/f noise is not removed by CDS as a result [1]. The CDS frequency is limited by the charge transfer time inside the pixel, which is not likely to decrease in future processes due to the decrease in supply voltage. Therefore, 1/f noise already limits the performance of today's CMOS imagers, and it can seriously hamper the migration to smaller pixel geometries if no alternative 1/f noise reduction techniques can be found.

In this paper, we will investigate the effects of 1/f noise on CMOS imagers made in deep submicron processes. In section II, we will briefly discuss the fundamental mechanisms behind 1/f noise. Based on these mechanisms, we will show that for minimum-size transistors in deep submicron processes, the properties of 1/f noise are quite different from the 1/f noise in large transistors. In section III, we will introduce an alternative 1/f noise reduction technique called switched-biasing, and discuss its applicability to CMOS imagers. In section IV, we will present measurement results on test circuits that show the effect of switched biasing on minimum size transistors biased as in a pixel. Finally, we will draw conclusions in section V.

II 1/F NOISE IN DEEP SUBMICRON MOSFETS

In spite of more than 50 years of research into 1/f noise phenomena in electronic devices, there is still discussion about the exact physical mechanisms that give rise to 1/f noise. However, it is generally accepted that traps at the $Si\text{-}SiO_2$ interface play the most important role [2]. As a result, electrons or holes inside the channel can get 'trapped' at the $Si\text{-}SiO_2$ interface, and after a while, they are again 'released' into the channel. As a result, the channel current fluctuates in a random fashion.

It was McWhorter [3] who first showed that the trapping/detrapping process can lead to a 1/f type spectrum. To this end, he described the behaviour of each single trap as a so-called Random Telegraph Signal (RTS) [4]. The Power Spectral Density (PSD) of such signal, a so-called Lorentzian spectrum, is depicted in fig. 1a. The corner frequency that can be seen in this PSD depends on the properties of the trap in question. If an MOS transistor contains a large number of such traps, and these traps do not interact, than their PSDs can be added. McWhorter showed that if the traps all generate an RTS with the same amplitude, and the corner frequencies of their PSDs are exponentially distributed, a 1/f noise spectrum will result (fig. 1b).

The McWhorter model yields an interesting prediction for small-area transistors in deep submicron processes. In such small transistors, the number of traps at the $Si\text{-}SiO_2$ interface will decrease to only a few or even only one per gate. This will have two effects. Firstly, the noise generated by traps will not exhibit a 1/f spectrum anymore, since a 1/f spectrum only results from the addition of a *large* number of traps. Therefore, it is more

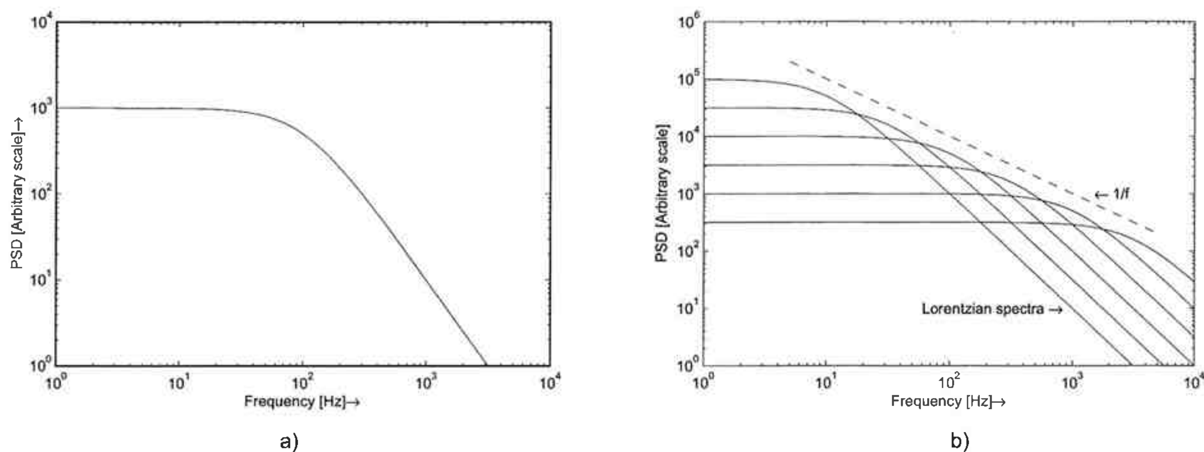

Fig. 1 a) PSD of a random telegraph signal b) A combination of large amount of RTS spectra yields a 1/f spectrum

accurate to refer to this noise source as Low Frequency (LF) noise rather than 1/f noise. Secondly, since the LF noise depends on the presence of only a few traps in a transistor, it is immediately obvious that the amount of LF noise will vary significantly from transistor to transistor.

Both predictions have recently been confirmed with measurements [5,6]. In fig. 2 measurements on a transistor with a gate area of $0.18\mu m^2$ are depicted. As can be seen in the figure, the LF noise clearly consists of an RTS signal, indicating that the noise generation inside the transistor consists of only a single trap.

III LF NOISE REDUCTION USING SWITCHED BIASING

Switched biasing is a relatively unknown circuit technique that can reduce the LF noise of a MOS transistor. The effect was first published in 1991 [7], and was studied in more detail in [6, 8].

In contrast to more conventional techniques as CDS or chopping, that mitigate the effect of LF noise on a circuit level, switched biasing reduces the noise inside the MOS transistor itself. The concept of switched biasing is relatively simple. Instead of continuously biasing a MOS transistor, the transistor is periodically turned off. This reduces the LF noise of the transistor; according to literature, this noise reduction can be as large as 8 dB [8].

Although switched biasing itself is easy to apply, the underlying physical mechanism is not fully understood. Most likely, switching the transistor 'off' empties the traps at the Si-SiO_2 interface. When the transistor is switched on, these traps remain empty for some time, thus temporarily reducing the LF noise. This effect is quite interesting for the application of switched-biasing in CMOS imagers.

As mentioned in section I, the main source of LF noise in a CMOS imager is the in-pixel source follower transistor, depicted as transistor M2 in fig. 3. As can be seen in the figure, applying switched biasing to the source of transistor M2 does not require extra in-pixel circuitry. A minimal amount of extra circuitry is needed in the column and row circuits to connect the column bus to a high voltage and closing the row select transistor some time before the actual read-out. Thus, switched biasing can be easily applied to a CMOS imager.

IV LF NOISE MEASUREMENTS

To evaluate the effects of switched-biasing in transistors under conditions equal to those in an imager pixel, a test circuit was realized in an industrial 0.35µm CMOS process. In fig. 4, a simplified schematic of the test circuit is depicted. In an imager, the signal path is single-ended, but the test circuit was made fully differential to minimize susceptibility to outside noise sources, as well as to relax the dynamic range requirements of the read-out amplifier. As can be seen in fig. 4, two test transistors M1 and M2 can be switched on and off by changing the voltage on their sources via switches S1 and S2. First the transistors are switched off by applying a high voltage V_{switch} to the source of the transistors by closing switches S1a and S1b.

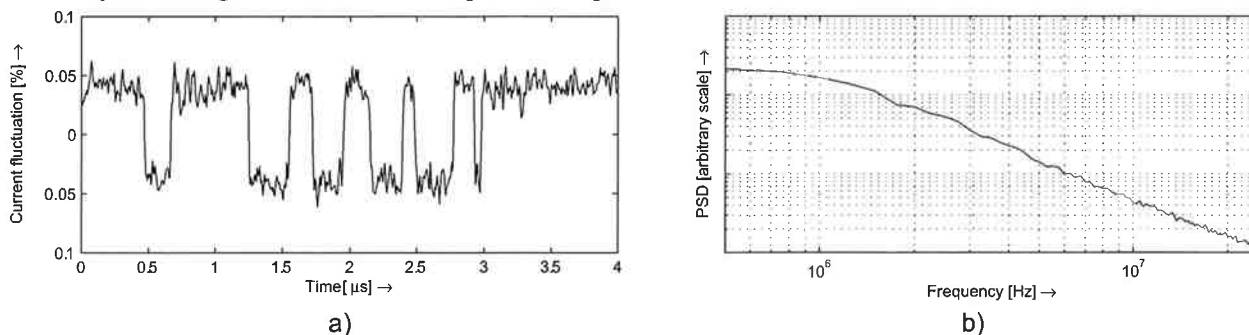

Fig. 2. a) Measurement of RTS noise in a 0.18 µm² transistor b) Corresponding Power Spectral Density (PSD)

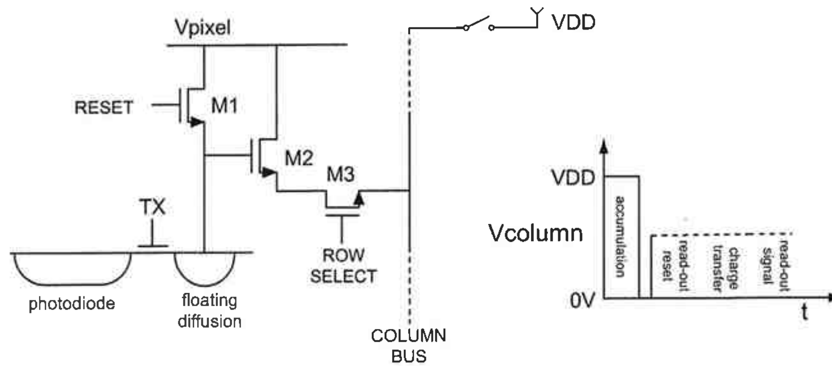

Fig. 3 Application of switched-biasing in a 4T pixel

After the transistors have been switched off for a certain time period and the traps in the channel interface are emptied, the source of the transistors is pulsed to ground by opening switches S1a and S1b, and closing switches S2a and S2b. This enables a faster read-out, as the readout amplifier's input common mode range does not extend to the positive supply. Finally, switches S3a and S3b are closed, and the 1/f noise of the transistors is measured. Since we can assume that the noise of the transistors is uncorrelated, the measured differential noise voltage is equal to the square-root of 2 times the noise voltage of one transistor All biasing voltages are supplied externally for maximum flexibility in the measurements.

Since the application of CDS is essential in CMOS imagers, a CDS operation can be performed in the digital domain (off-chip) to see the combined effect of CDS and switched-biasing, as both are expected to reduce the LF noise.

In fig. 5, scatter plots with measurement results are depicted. In both figures, the LF noise in steady-state condition is compared to the noise when applying switched-biasing. In fig 5a, the LF noise in steady state is compared to LF noise under switched-biasing conditions without applying CDS. In this plot, every dot corresponds to a transistor. On the x-axis, the noise in steady state is plotted, while the y-axis depicts the noise when switched-biasing is applied. Therefore, if the noise would be the same in both conditions, all dots would be on the line y=x that is plotted in the figures as a dotted line. However, this is not the case: most dots are below the line y=x as their LF noise is lower when applying switched biasing. Another observation that can be made from this plot is the large spread of over two orders of magnitude on LF noise between transistors, both in steady state and when applying switched biasing, as was predicted in section II. Although the LF noise of most transistors decreases, for some transistors it actually increases. The average noise decrease from 41 transistors is 1.4dB. In fig. 5B, a similar plot is depicted for the case where switched biasing is applied together with CDS. Surprisingly, although both techniques should reduce LF noise, their combined application actually leads to a noise increase, as can be seen in the figure. This is disappointing, since the application of CDS is essential to CMOS imagers and therefore cannot be omitted.

Detailed analysis [6] reveals that the noise increase observed when CDS is applied in conjunction with switched biasing is caused by the fact that the bias history of both sample instants is not identical. Whereas a simple, steady-state noise model cannot explain this effect, the correct transient noise description explains that when

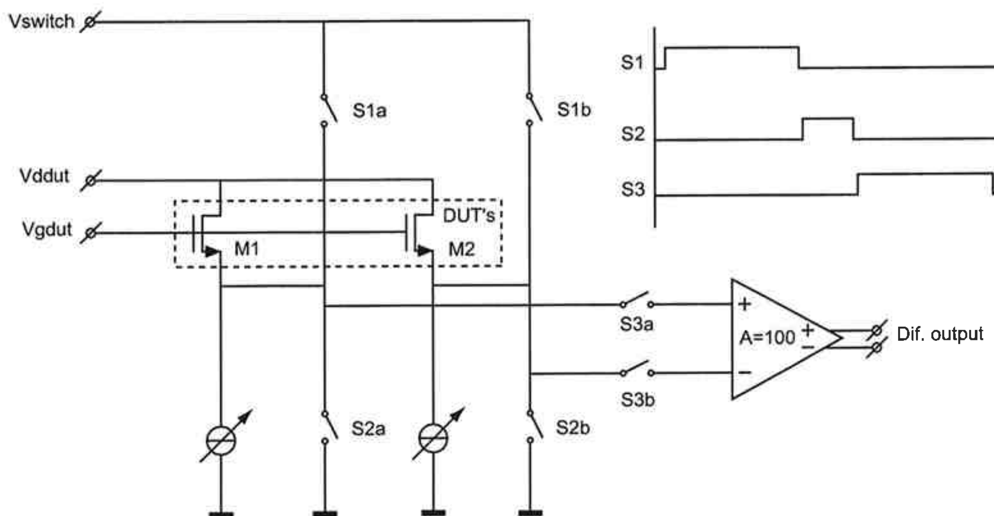

Fig. 4 Test circuit measuring the effects of switched-biasing on minimum-size transistors with biasing as in a CMOS imager

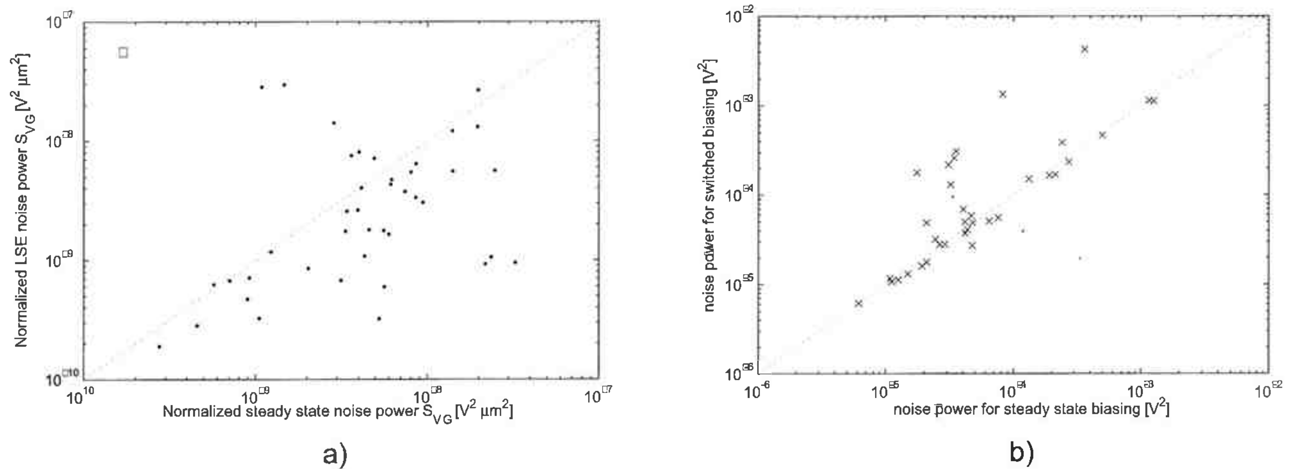

Fig. 5 Measurement results comparing 1/f noise under steady state and switched-biasing conditions: a) Without CDS b) With CDS

these two noise reduction techniques (CDS and switched biasing), which each work in isolation are combined, a noise increase results.

V CONCLUSION AND FUTURE WORK

In this paper, a study of the effects of 1/f noise in deep submicron CMOS processes is presented. It is shown that in such processes the 1/f noise of minimum-size transistors depends on only a few traps, and therefore does not exhibit a 1/f spectrum any more. The application in CMOS imagers of an alternative 1/f noise reduction technique, switched biasing, is proposed. However, measurements show that this technique is not effective in conjunction with CDS if measures are not taken to ensure that the bias history of both samples is identical. Therefore, a different approach to applying switched-biasing in CMOS imagers has to be researched. If the biasing history for both CDS samples is kept exactly identical while applying switched-biasing, a more positive result may be obtained.

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