A Low-Power Column-Parallel 12-bit ADC for CMOS Imagers

M.F. Snoeij, A.J.P. Theuwissen, and J.H. Huijsing
Delft University of Technology
The Netherlands
E-mail: M.F.Snoeij@ewi.tudelft.nl

Abstract - **This paper describes the design of a low-power column-parallel single-slope ADC for CMOS imagers. The design exploits the characteristics of photon shot noise present in imaging signals to reduce power consumption. A prototype imager with a 12-bit column-level ADC was designed in a 0.18µm CMOS process. Each analog column circuit consumes only 3.2µW, enabling a column-parallel ADC for a VGA imaging array with a power consumption of less than 5mW.**

I INTRODUCTION

The application of CMOS image sensors in mobile devices, particularly cell phones, continues to drive the development of low-cost cameras-on-a-chip. There are two key imager requirements in this application. Firstly, there is a strong demand for ever-higher resolutions. Secondly, power consumption is obviously a key issue in battery-powered device.

Both requirements have implications not only on the design of CMOS pixels, but also on the design of the analog readout circuitry: these circuits need to be faster to readout a higher-resolution imaging array, but their power consumption should not increase. Obviously, these are conflicting demands. In our view, this challenge cannot be met with the current readout architecture, and therefore, breakthroughs on the architectural level are necessary to increase the power efficiency, i.e. the amount of power required to readout an imaging array at a certain signal/noise performance. Within the analog readout chain, the ADC has the highest power consumption. In order to increase the power efficiency of the total system, attention should therefore be focused on improving the ADC.

Most low-cost CMOS imagers on the market today use a high-speed chip-level ADC. In contrast, recent publications [1-3] have shown that column-parallel ADCs can offer several advantages over more conventional chip-level ADCs. In particular, column-parallel ADCs can achieve a lower read-out noise and are better suited for high-resolution imagers. The main disadvantage of column-parallel ADCs is a relatively high power consumption.

This work presents a 12-bit column-parallel ADC for a CMOS imager. It uses the well-known single-slope architecture and exploits the properties of photon shot noise present in imaging signals to reduce power consumption. Compared to a conventional 12-bit single-slope ADC, this leads to a reduction in power consumption by about a factor of 5. A prototype of the ADC has been implemented in a standard 0.18µm process and operates at 1.8V.

This paper is organized as follows. In section II, we will discuss the technique of exploiting photon shot noise to reduce the power consumption of an imager ADC. Based on this technique, a system level overview of our ADC is presented in section III. In section IV, we will present the analog column-level circuitry used in our ADC and present the results of simulations with these circuits. Finally, conclusions will be drawn in section V.

II EXPLOITING PHOTON SHOT NOISE IN IMAGER ADCS

Photon shot noise is present in all image sensors, as it is caused by the random manner in which photons strike the imaging array. As is well known, the amount of photon shot noise equals the square root of the amount of electrons in a pixel:

$$e_{phs} = \sqrt{N} \qquad (1)$$

Where e_{phs} is the photon shot noise expressed in rms noise electrons and N is the amount of electrons in the pixel. This is graphically illustrated in fig. 1a . As can be seen, throughout most of the input signal range, photon shot noise is the dominant noise source. The other noise sources in an imager do not depend on the input signal and are depicted in the figure as the noise floor. One of these constant noise sources in conventional designs is the quantization noise of the ADC:

$$e_{qns} = \frac{1}{\sqrt{12}} q_s \qquad (2)$$

Where e_{qns} is the rms quantization noise and q_s is the quantization step of the ADC (both expressed in electrons). In conventional designs, q_s and thus the ADC resolution is chosen such that the noise is low enough for low signal inputs, where the ADC performance is most critical. However, this means that in the large input signal region where the photon shot noise is dominant, the ADC performance is actually higher than needed, i.e. the quantization step of the ADC can be increased without decreasing the overall signal-to-noise performance.

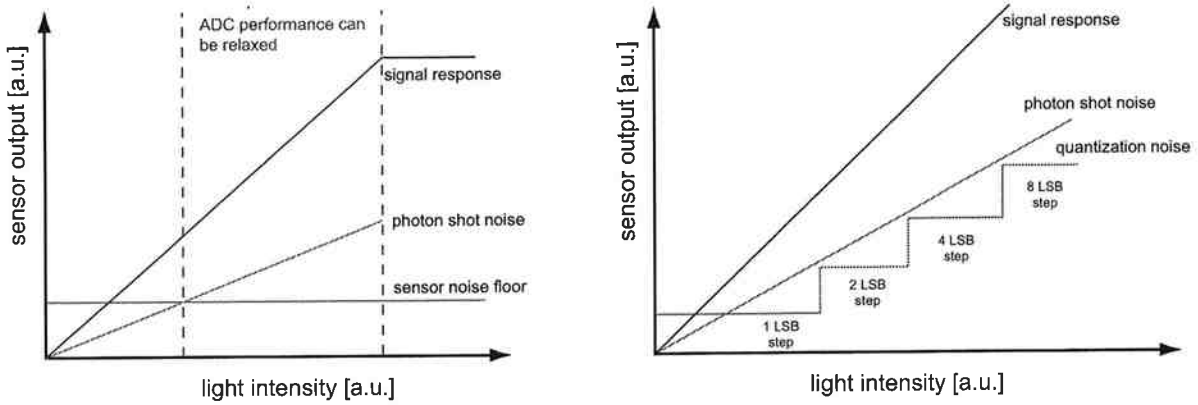

Fig. 1 a) Photon shot noise dominates in most of the imager input range b) An increase in ADC quantization noise does not worsen overall noise performance of the imager

There are several ways to change the quantization step of the ADC for different inputs. In this work, a binary-increasing quantization step was chosen, i.e. the quantization step increases from q_s to $2q_s$, then to $4q_s$, etc. This leads to a very simple system level design, as will be shown in the next section. Based on this approach, we can calculate the amount of quantization levels necessary in our ADC. If we consider only photon shot noise and quantization noise, the total amount of noise in an imager is given by:

$$e_{total}=\sqrt{e_{qns}^2+e_{phs}^2}$$

Now, when we double the quantization step this doubles the quantization noise and increases the total noise e_{total}. We can determine the input signal levels at which the quantization noise can increase by choosing a maximum allowable noise increase:

$$\sqrt{(2e_{qns})^2+e_{phs}^2}=a\sqrt{e_{qns}^2+e_{phs}^2}$$

Where a is the maximum tolerated noise increase factor. Re-arranging the above equation for e_{phs}:

$$e_{phs}=\sqrt{\frac{4-a^2}{a^2-1}}e_{qns}$$

This equation shows how much photon shot noise is required to be able to double the ADC quantization noise while not exceeding the maximum noise increase a.

Using this equation, we can now determine the total amount of quantization steps required in our ADC. For an effective resolution of 12 bits, a pixel saturation charge of 25000 electrons, and 1% excess noise (a=1.01), this leads to 848 quantization steps. If a larger amount of 3% excess noise (a=1.03) is allowed at the input levels where the quantization noise is doubled, the amount of quantization steps is only 504.

Both figures are much lower than normal linear quantization in a 12-bit ADC, which requires 4096 quantization steps. As a result, if we have an ADC architecture where the power consumption depends on the amount of quantization steps, we can potentially reduce the power consumption by a factor of 5. In the next section, we will show that this is indeed possible.

III ADC ARCHITECTURE

Although several ADC architectures could be applied in column-level ADCs, we consider the single-slope architecture, as depicted in fig. 2a, to be most suitable for

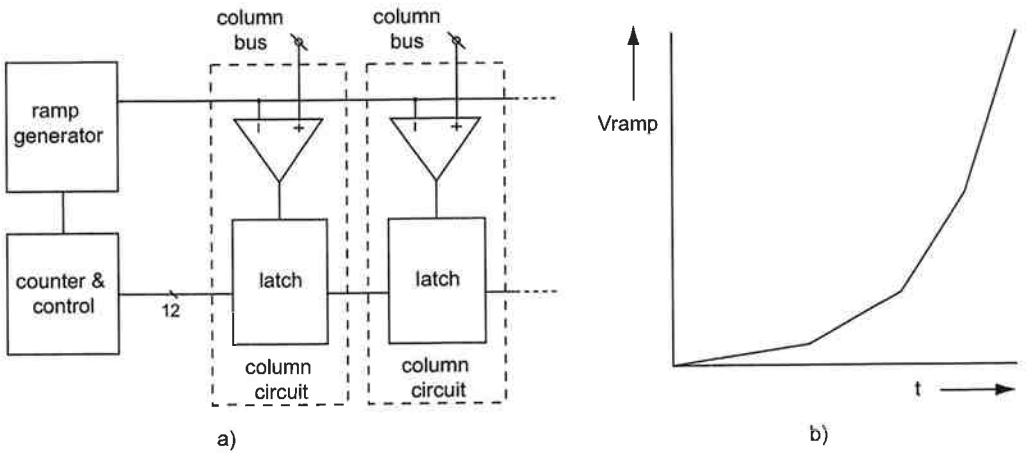

Fig. 2 a) Block diagram of the proposed column-level single-slope ADC b) Proposed piece-wise linear ramp voltage to exploit photon shot noise

our design. The advantage of a single-slope architecture is the simplicity of the column circuit: a comparator is the only analog circuit required. This is not only attractive to minimize the required chip-area, but also makes it relatively simple to ensure uniformity between the columns, which in first order only depends on the offset of the comparator.

The technique of exploiting photon shot noise to reduce power consumption described in section II, can be applied very well in a single slope ADC, by changing the ramp signal. This signal is related to the ADC input signals: the part of the ramp with the highest voltage corresponds to the highest input signal, where the quality of the ADC is not critical due to high photon shot noise. Therefore, instead of a linear ramp, we can use a piece-wise-linear ramp. As depicted in fig. 2b, the segments of this piece-wise-linear ramp have a binary increasing slope, i.e. in every segment the slope is doubled compared to the previous one. Therefore, if the amount of quantization levels can be decreased by a factor of 5, the conversion time of the ADC can be reduced by a factor of 5. Alternatively, the column-level comparators, which will most likely consume most of the power due to their large number, can be made 5 times slower and thus consume much less power.

A key requirement to the analog signal processing chain of an imager is that the input-output relation should be linear to enable easy color processing in the digital domain. Although the proposed ADC has non-linear quantization intervals, the binary increase of the quantization intervals makes it very easy to correct for the non-linear quantization. To this end, the digital counter is synchronized with the ramp generator such that it will increment the count by 1 integers per clock cycle at the first slope segment, 2 integers per clock cycle at the second slope segment, etc. This effectively creates a digital code with a linear dependence on the input voltage, in which many of the 12-bit code words are skipped.

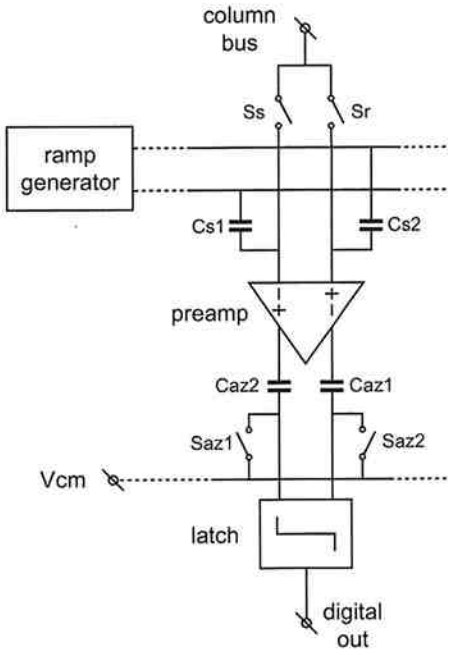

Fig. 3 Block diagram of the analog column circuit

IV ANALOG CIRCUIT IMPLEMENTATION

To test the concept described in the last two sections, a prototype VGA imager has been designed in a 0.18µm CMOS process. To obtain flexibility in the design, the ramp-generator is implemented off-chip, which leaves the column level circuit as the only analog component on the chip. The target frame rate of the imager is 30 frames/sec, which means that the conversion time of the column-level ADC should be approximately 65µs.

In fig. 3, an overview of the analog column-level circuit is given, which is similar to the circuit used in [2]. The signal and reset voltages of the pixel are sampled onto capacitors Cs1 and Cs2 by consecutively closing switches Sr and Ss while the ramp generator outputs a common-mode voltage. After the sampling, a ramp voltage is applied to capacitors Cs1 and Cs2. By applying a ramp voltage with an opposite magnitude to the differential voltage on the capacitors, the comparator output will

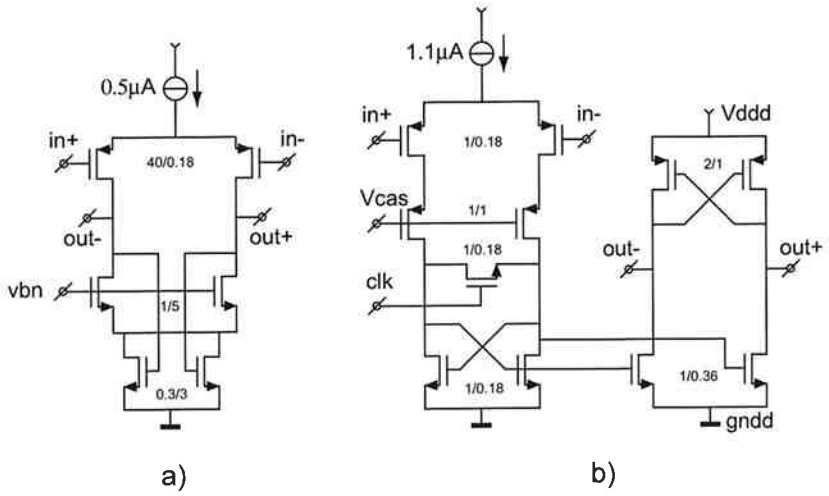

Fig. 4 Schematics of the comparator: a) Preamp b) Regenerative latch

trigger when the ramp voltage equals the difference of the signal and reset voltage. Although the circuit described in [2] uses a fully differential ramp voltage, we intend to use a pseudo-differential ramp voltage. Although the ramp-generator will be made symmetrical, one of its outputs will output a constant voltage. The advantage of this approach is that the common-mode input voltage of the comparator remains constant, which relaxes its required common mode rejection ratio.

The comparator itself is designed as simple as possible to minimize power consumption. It consists of 2 stages: a preamp and a regenerative latch. The schematic of the preamp is depicted in fig. 4a. It is basic gain stage with a gain of typically 30. It is followed by a regenerative latch (fig 4b) that provides a digital output signal.

Two key specifications for the comparator are its delay and its offset. In a conventional single-slope architecture, the comparator delay should be less than one clock period of the digital counter, which is 50ns in our design. However, a comparator with a delay less than 50ns, would consume a lot of power and have a relatively high noise due to its high bandwidth. Therefore, the comparator is allowed to have a higher delay and which is compensated on system level. A delay measurement is performed after every A/D conversion and the measured delay is subtracted from the signal in the digital domain. As a result, the preamp consumes only 0.9μW and has an integrated voltage noise of only 30μV rms, which is well below the readout noise of the pixel.

The offset of the comparator is compensated using a two step approach. First of all, auto-zero capacitors Caz1 and Caz2 (fig. 3) sample the offset of the preamp. What remains is the regenerative latch offset, which can be as large as 40mV (4σ) at the latch input, which is 1.3mV at the preamp input. This residual offset is removed by measuring it with a second A/D conversion and subtracting the result from the signal in digital domain. The advantage of this two-step approach is that the circuit-level auto-zero performed with capacitors Caz1 and Caz2 significantly reduces the conversion time required to measure the remaining offset with a second A/D conversion. At the same time, compensating the offset using only a circuit-level auto-zero would require the preamp to have a much higher gain, which is problematic to achieve with the basic circuit used here to minimize power consumption.

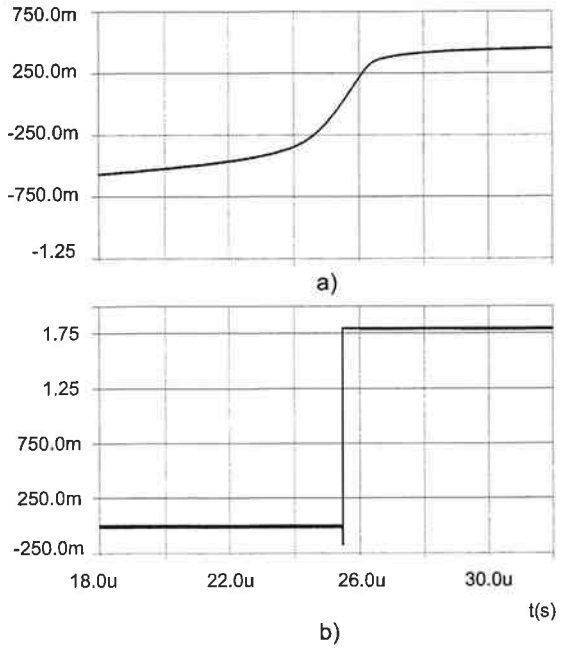

Fig. 5 Comparator simulation: a) differential preamp output b) latch output

In fig 5a, a circuit simulation of the preamp output is depicted, which shows the preamp delay of about 450ns. In fig 5b, a simulation of the regenerative latch output is displayed. The power consumption of the latch is 2.3μW, and the total power consumption is 3.2μW. Since 680 column circuits are needed for a VGA imager, and the ramp generator is expected to consume less than 2mW, the proposed ADC is expected to consume less than 5mW. A more detailed description of the comparator design can be found in [4].

V CONCLUSION

A low-power column-level imager ADC design is presented. It exploits the photon shot noise present in the imaging signal to reduce power consumption. To this end, it features a single-slope ADC architecture with a piece-wise linear ramp voltage which increases the quantization noise at high input voltage, without compromising the performance. Its column comparator is compensated for delay and offset in the digital domain, allowing a simple, low-power analog circuit that consumes only 3.2μW. The resulting CMOS imager was designed in a 0.18μm CMOS process.

ACKNOWLEDGEMENTS

The authors thank K. Makinwa, A. Mierop and M. Pertijs for the useful discussions that contributed to this work. Fabrication of the prototypes at Philips Semiconductors is appreciated.

REFERENCES

[1] T. Sugiki et al. , "A 60 mW 10b CMOS image sensor with column-to-column FPN reduction", *IEEE International Solid-State Circuits Conference*, vol. XLIII, pp. 108-109, February 2000

[2] K. Findlater et al. , "SXGA pinned photodiode CMOS image sensor in 0.35μm technology", *IEEE International Solid-State Circuits Conference*, vol. XLVI, pp. 218-219, February 2003

[3] A. Krymski, N. Khaliullin and H. Rhodes, "A 2e noise 1.3 megapixel CMOS sensor", *IEEE workshop on CCDs and advanced imager sensors*, May 2003

[4] M.F. Snoeij, A.J.P. Theuwissen and J.H. Huijsing, "A 1.8V 3.2μW Comparator for Use in a CMOS Imager Column-Level Single-Slope ADC", accepted for publication at *ISCAS 2005*, Kobe, Japan, May 2005