A 1.8V 3.2µW Comparator for Use in a CMOS Imager Column-Level Single-Slope ADC

M.F. Snoeij, A.J.P. Theuwissen and J.H. Huijsing
Electronic Instrumentation Laboratory
Delft University of Technology
Delft, The Netherlands
e-mail: M.F.Snoeij@ewi.tudelft.nl

***Abstract*—In this paper, a 1.8V 3.2µW comparator is presented. It features a hybrid offset compensation scheme and achieves over 60dB gain with an input offset below 150µV. The comparator is designed in a 0.18µm CMOS process and is specifically designed to be used as the key component of a column-level single-slope ADC of a CMOS imager. This ADC architecture is attractive because of its low noise, but so far this has come at the price of a relatively high power consumption. Using this comparator design, the power consumption of column-level single-slope ADCs can be reduced significantly.**

I. INTRODUCTION

CMOS imagers have evolved in the last decade into the imaging technology of choice for many applications. Compared to conventional CCD imagers, they offer lower power consumption at lower supply voltages. Their most important advantage is the possibility to realize both sensor and readout electronics on a single substrate, thus creating a camera-on-a-chip. However, in spite of the advantages, some challenges still remain. Firstly, the imaging quality of a CMOS imager is still lower than that of most CCDs due to higher noise levels. Secondly, there is a continuing demand for higher resolution imagers. Thirdly, a further decrease in power consumption is highly desirable in some applications, particularly in cell phones. These three design challenges have an important impact on the imager's readout circuit.

First of all, the readout circuitry significantly contributes to the total noise of the imager. Therefore, to increase the imaging quality, the noise in the readout circuitry needs to be decreased. Furthermore, the speed of the readout circuitry has to be increased in order to be able to increase the resolution of the imager. Finally, since the readout circuitry consumes most of the power in a CMOS imager, its power consumption must be reduced in order to decrease the overall power consumption of the imager. For a given readout architecture, these demands conflict with each other, as increasing the readout speed means either a higher power consumption or higher noise, and decreasing the noise means either increasing power consumption or decreasing bandwidth. Therefore, a change on the architectural level is necessary to create a readout circuit that has less noise and a lower power consumption but a higher speed.

The most important part of the readout circuit of a CMOS imager is the ADC. Most of today's image sensors use a chip-level ADC, i.e. all pixel outputs are input to a single ADC. In a typical VGA imager for mobile applications, this ADC would consume in the order of 15mW at 30frames/second. Although a chip-level ADC has several advantages, it has an important drawback: the bandwidth of the ADC has to be high (>10MSPS). This has a negative impact on the noise performance. In contrast, it has been shown [1-3] that a column-parallel ADC can offer a significantly lower noise, as each ADC channel has a much lower bandwidth. Moreover, as the ADC is in the column, the analog signal path can be shorter, which also decreases noise.

In Fig. 1, a possible approach for a column-level ADC is depicted [2]. Here, the well-known single-slope ADC architecture is used. One central ramp generator is used for all the column circuits, and therefore only a comparator and a latch have to be implemented in every column. The advantage of this approach is that, compared to other ADC architectures, it is relatively easy to compensate for circuit non-uniformities, since these non-uniformities only consist of comparator offset. However, so far imagers with such ADCs have a higher power consumption than imagers with a chip-level ADC, e.g. 60mW in [1] and 20mW in [2] (the latter number is recalculated to VGA resolution at 30 frames/second). Most of this power is probably consumed by

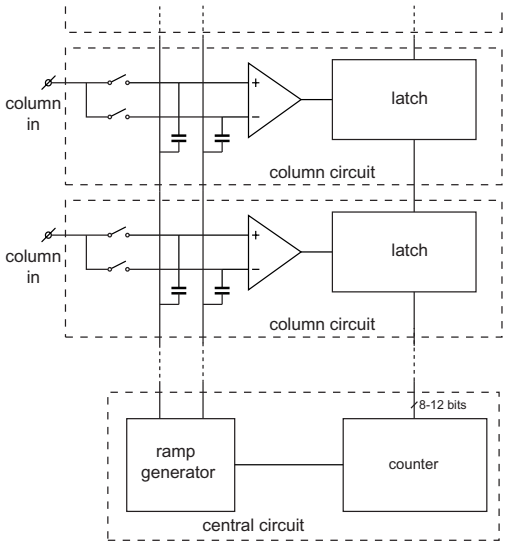

Fig. 1. Column-level single-slope ADC architecture

the column circuitry, in particular by the comparator. Therefore, to decrease the ADC power consumption, a low power comparator design is needed.

In this paper, a compact low-power comparator is presented that can be used in a column-level single-slope ADC. It is designed for a 0.18µm CMOS process and features a hybrid offset compensation scheme. It achieves over 60dB gain at a power consumption of only 3.2µW. Therefore, this design will enable a 10 bits ADC for a VGA resolution imager that has a power consumption below 5mW.

This paper is organized as follows. In section II, the system design of the comparator is presented, as well as its operation inside the single-slope ADC. In section III, the circuit design of the comparator is presented. In section IV, simulation results of the circuitry are presented. Finally, conclusions are drawn in section V.

II. SYSTEM DESIGN AND OPERATION

A. ADC Target Specifications

The comparator is intended to be used in a VGA imager that can output 30 frames/second, and therefore has a line time of about 65µs, of which 50µs can be used for the A/D conversion. The target resolution is 10 bits, which means that a clock frequency of 20MHz is necessary, i.e. the ramp increases with one LSB every 50ns. The pixel design dictates that the maximum signal input of the ADC is 500mV, thus the LSB voltage is 500µV. As the comparator has to discriminate between two LSBs, the comparator gain should therefore be at least 1000.

B. Circuit Topology

There are two classes of circuits that can be used to create a comparator: gain stages and regenerative latches. At a first glance, designing a comparator using only gain stages might seem more attractive, as they do not 'pollute' the supply rails and ramp voltage with current peaks due to switching. However, creating a gain of over 1000 in every column can easily cause instability. As a gain stage is continuously switched on, there is a high-gain forward signal path constantly present. The comparator inputs have a high impedance, as they are only connected to sampling capacitors. Therefore, if a small parasitic capacitance is present from output to input, it can create a positive feedback loop that may cause instability. Therefore, a regenerative latch is preferable, as it only has a high gain at the clock edge. To reduce the kick-back effect, i.e. the charge injection into the input of the regenerative latch, a preamp has to be added in front of the latch.

C. Delay

In a classical single-slope ADC design, the delay of the comparator has to be less than one clock period, as a higher delay creates an offset in the digital output. However, a comparator with a delay less than 50ns, as required in our case, would consume a lot of power and have a relatively high noise due to its high bandwidth. Therefore, the comparator is allowed to have a higher delay and compensate for it on system level. A delay measurement is performed after every A/D conversion and the measured delay is subtracted from the signal in the digital domain. A typical delay of 600ns is accepted, to enable the design of a low-power low-noise circuit, as will be shown in section III and IV.

D. Offset

Comparator offset can create column non-uniformities in the image, to which the human vision system is very sensitive. Therefore, the comparator offset should be well below ½ LSB; our target is 125µV. A preliminary analysis of the intended circuit blocks shows that the preamp can have a minimum input offset of 9mV (4σ). The optimal input offset specification for the regenerative latch is at least 30mV (4σ); although lower offsets are possible, this would increase power consumption quite significantly. Therefore, a dynamic offset cancellation technique will be necessary. Since the input signal is already sampled, it is most advantageous to apply auto-zeroing.

There are two methods of implementing the auto-zero. On one hand, a separate A/D conversion for offset could be performed, which could be conveniently combined with the delay measurement mentioned in the previous section. The main disadvantage is the relatively long conversion time this takes; measuring an offset of ±9mV in 125µV increments takes 144 clock cycles.

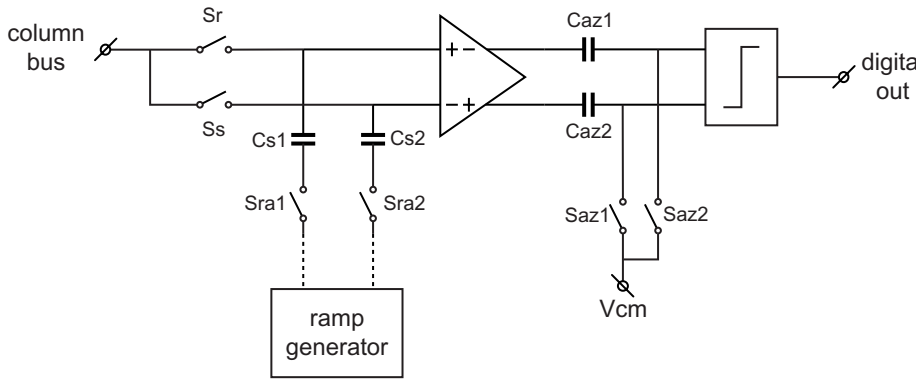

Fig. 2. Column circuit topology

On the other hand, it is also possible to implement an auto-zero at circuit level. The offset of the preamp can be corrected by storing the offset on capacitors, either at the input or the output of the preamp. We have chosen to consider only output storage, as input storage can interfere with the sampling capacitors at the preamp input. This limits the gain of the preamp to about 50, as a higher gain would cause the comparator outputs to saturate during offset sampling.

The input referred offset of the latch is at minimum 30mV/50=600μV, which is too high for our application. We therefore use a *hybrid* offset compensation scheme: first, we reduce the offset by auto-zeroing the preamp; second, we perform a combined delay/offset measurement at the system level. This approach reduces the required conversion time needed for the system auto-zero, while it does not require a low-offset regenerative latch that consumes a lot of power.

The resulting system topology is depicted in Fig. 2.

III. CIRCUIT DESIGN

In Fig. 3, the preamp circuit is depicted. Only transistors M1-M7 have to be implemented in every column; the biasing circuitry can be implemented centrally. Differential pair M2-M3 is loaded with current sources M4 and M5. The gain is determined by the combined output resistance of M2-M5 and the gm of M2-M3. The output resistance of the current sources is negligibly high; the voltage gain of the preamp is therefore determined by the length of the input transistors. As a result, the gain will vary considerably over temperature and process variations; however, as the preamp is part of a comparator, an accurately defined gain is not necessary. The output common-mode voltage is regulated to voltage V_{cm} by transistors M6-M7 that operate in triode region.

In Fig. 4, the regenerative latch circuit is depicted. This latch is based on the circuit presented in [4] and consists of two stages. The first stage, consisting of transistors M1-M7 provides most of the dynamic gain and is reset every clock cycle in order to eliminate any memory effect. The second stage amplifies the output of the first stage to digital levels. When the clock is high, transistor M5 resets the first latch. During this phase, transistors M8-M9 will be switched on, but transistors M8-M11 are dimensioned in such a way that the output of the latch does not change in this phase. When the clock goes low, a positive feedback loop will be created around M6-M7. Although this loop will not deliver a rail-to-rail output, it will be enough to drive transistors M8-M9. These will change the state of the second stage latch if the input value has changed sign since the last clock period; therefore, a digital output value will be continuously available at the output of the circuit.

The advantage of this latch circuit is that, unlike many other regenerative latch circuits, the first stage draws a constant current. Although the second stage does have a current peak at the moment of switching, this only happens when the latch output changes; moreover, as the operation of the second stage is not very critical, it can be connected to the digital supply (vddd). This greatly reduces the chance that one comparator can trigger the next in our parallel ADC structure.

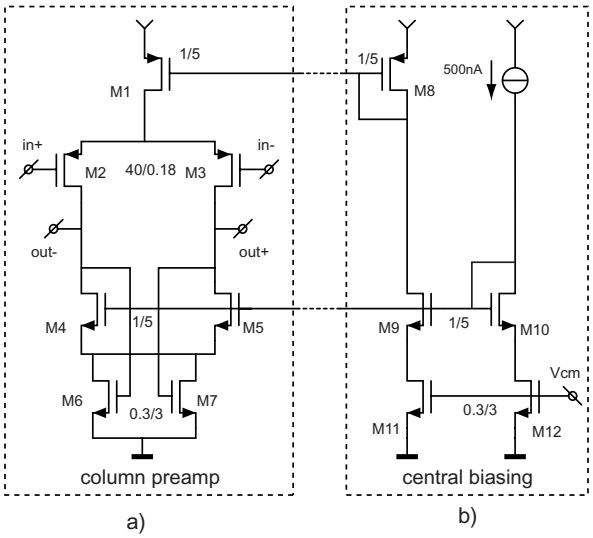

Fig. 3. a) Column preamp circuit b) Central biasing circuit

IV. SIMULATION RESULTS

In Fig. 5, simulation results of the comparator are given. In this simulation, we apply a 500mV ramp voltage to the comparator. The comparator input crosses 0V at t=25μs. As can be seen in Fig. 5a, the preamp output has a delay of about 600ns. As can be seen in Fig. 5b, the latch has a negligible delay. As described earlier, one of the design goals for the comparator was to have an analog supply current that is as constant as possible. In Fig. 5c, the simulated analog and digital supply current are depicted. As can be clearly seen in the figure, there is a high peak current in the digital supply current (shown in black). This is caused by the switching of the second stage of the regenerative latch, which only occurs when the output of the comparator

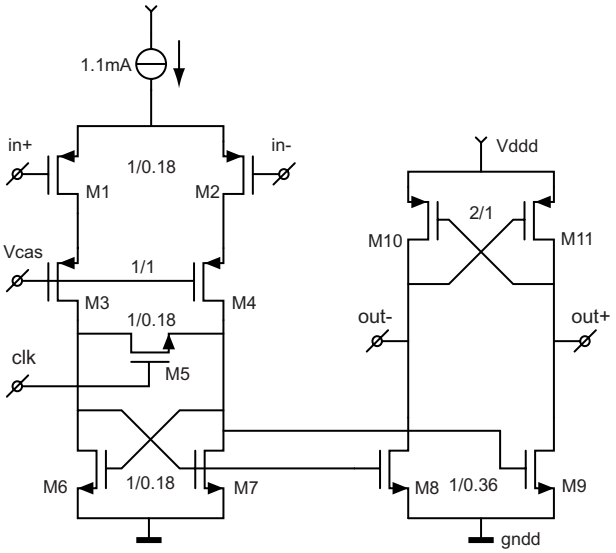

Fig. 4. Regenerative latch circuit

changes value. However, the analog supply current (shown in gray), is nearly constant. The total average supply current for the comparator is about 1.8µA, which equals 3.2µW. Finally, in Fig. 5d, the settling of the output of the preamp is shown during the auto-zero phase.

Ensuring correct operation over process corners is obviously very important. We have therefore checked the spread by doing corner simulations with the following parameters:

- Transistor spread (slow/fast corners)
- Temperature (-15 to +100ºC)
- Bias current (±20%)

By exhaustively testing for all combinations of these parameters, the worst-case spread can be found. Results of these simulations for the preamp are given in table I.

TABLE I. SIMULATED WORST-CASE PREAMP PARAMETER SPREAD

	Min.	**Typ.**	**Max.**
GBW (MHz)	7	11,9	17,2
-3dB freq. (kHz)	174	354	653
DC voltage gain	26.3x	33.1x	40.3x
Delay (ns)	250	450	820

As can be seen in the table, there is a large spread in both AC frequency response and in DC gain. The spread in frequency response results in a varying delay. This will be corrected by delay compensation; since the worst-case delay is 820ns here, we will take a delay measurement on system level with a maximum of 1µs to have design margin. The spread on DC gain should stay within limits posed by the offset compensation scheme: the gain should stay below 50 to prevent clipping of the preamp output, and above 20 to limit the input-referred offset of the latch. As can be seen from the table, this is the case.

Corner simulations of the regenerative latch show that it is insensitive to changes in the described process parameters. Its main parameter of interest is its delay, which should be shorter than one clock period. This is the case for all corners.

V. CONCLUSION

A 1.8V comparator for use in a column-level single-slope ADC of a CMOS imager was presented. By using delay compensation it achieves over 60dB gain at a power consumption of only 3.2µW. The comparator features a hybrid offset compensation that decreases its offset to below 150µV. Using these techniques, the comparator can be realized in a compact circuit of only 18 transistors, which makes it very suitable for implementation in the column of a CMOS imager. Simulation results show that the comparator performs correctly over process corners. Work on a silicon implementation of the comparator is ongoing.

VI. ACKNOWLEDGEMENT

The authors would like to thank Philips Semiconductors for their financial and practical support of this project.

REFERENCES

[1] T. Sugiki et al. , "A 60 mW 10b CMOS image sensor with column-to-column FPN reduction", *IEEE International Solid-State Circuits Conference*, vol. XLIII, pp. 108-109, February 2000

[2] K. Findlater et al. , "SXGA pinned photodiode CMOS image sensor in 0.35µm technology", *IEEE International Solid-State Circuits Conference*, vol. XLVI, pp. 218-219, February 2003

[3] A. Krymski, N. Khaliullin and H. Rhodes, "A 2e noise 1.3 megapixel CMOS sensor", *IEEE workshop on CCDs and advanced imager sensors*, May 2003

[4] I. Mehr and D. Dalton, "A 500-MSample/s, 6-bit Nyquist-rate ADC for disk-drive read-channel applications", *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 7, July 1999

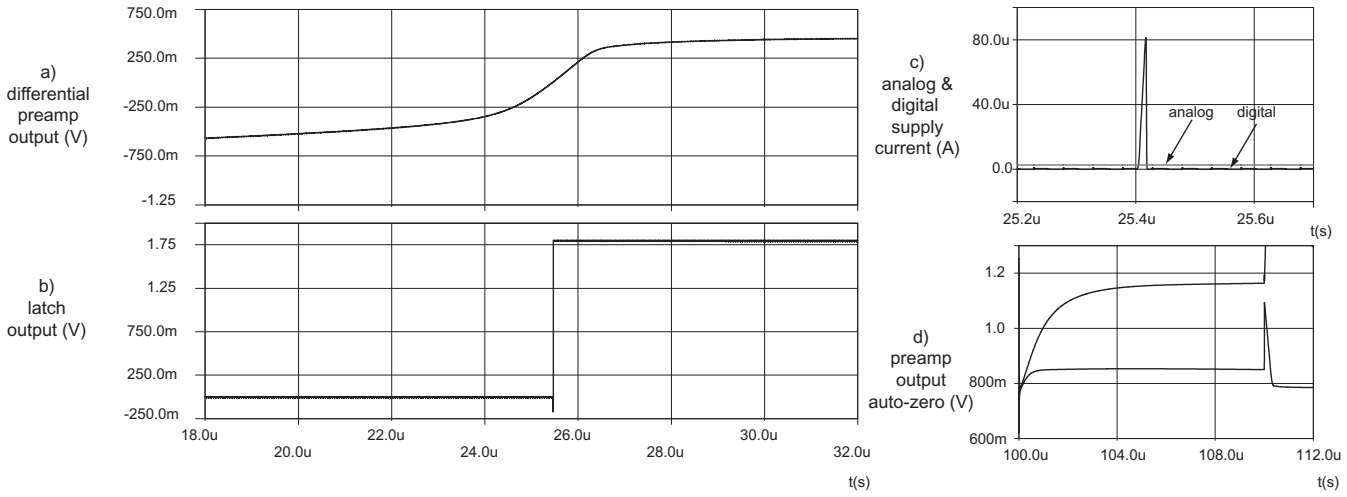

Fig. 5. Comparator simulation: a) differential preamp output b) latch output c) analog & digital supply current d) preamp output during auto-zero