Read-Out Circuits for Fixed-Pattern Noise Reduction in a CMOS Active Pixel Sensor

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Abstract— **An important limitation on the quality of an image produced by a CMOS active pixel sensor are non-uniformities in the pixel array, usually referred to as fixed-pattern noise. These are mainly caused by offset and gain mismatches between the in-pixel amplifiers. This paper describes new read-out circuits that can significantly decrease the gain errors in a pixel array. Simulation results show that gain variance due to variation in biasing and geometric variation can be reduced by 32 and 16 dB, respectively.**

Keywords— **Image sensors; CMOS APS; read-out circuitry; fixed-pattern noise; interface electronics**

I. INTRODUCTION

CMOS image sensors have evolved in the past years as a promising alternative to the conventional Charge-Coupled Device (CCD) technology. Compared to the latter, they offer lower power consumption, more functionality and, most importantly, the possibility to integrate a complete camera system on one chip, which can lead to lower cost [1]. These advantages make CMOS image sensors particularly suited for use in portable devices (cell phones, laptops etc.) where low power and small system size are essential.

In any image sensor, it is of importance that the signal transfer characteristic of every pixel is uniform, since the human eye is very sensitive to non-uniformities in an image. Two types of non-uniformities can be distinguished. Firstly, circuit offsets and dark current create non-uniformities even in complete darkness, and are therefore often called dark fixed-pattern noise. Secondly, circuit gain mismatches create non-uniformities when light is applied to the sensor, and are therefore often called light fixed-pattern noise. There is a significant difference in the amount of fixed-pattern noise between CCDs and CMOS image sensors due to the difference in their read-out circuits.

Both CCDs and CMOS image sensors usually work in integrating mode. This means that the photocurrent generated by the photosensitive device is integrated, creating an amount of charge. This charge is later converted into a voltage using a capacitive node. The resulting voltage is read-out for further processing.

The essential difference between CCDs and CMOS image sensors is the location within the sensor where the charge-to-voltage conversion takes place. In a CCD, the charge packets of every pixel are transported to the edge of the pixel array, where charge-to-voltage conversion and subsequent read-out takes place in a single read-out amplifier. The advantage of this approach is that the offset and gain errors between different pixels of the array are relatively small, since the charge transport is almost error free and errors in the read-out amplifier will affect all pixels in an equal manner. In a CMOS Active Pixel Sensor (APS) however, the charge-to-voltage conversion takes place inside the pixel. An in-pixel read-out amplifier, which usually consists of one minimum-size transistor, amplifies the resulting voltage.

As a result, CMOS image sensors suffer much more from fixed-pattern noise than CCDs. One important technique is already applied in CMOS APS to decrease fixed-pattern noise: Correlated Double Sampling (CDS). This can decrease offset, but does not decrease the gain error [2]. The research presented in this paper describes new read-out circuits that can reduce this error.

This paper is organized as follows. The problems of the existing in-pixel amplifier and proposed new circuits will be discussed in section 2. Section 3 describes the

partitioning of the readout circuits necessary to implement the circuits in an array. In section 4, simulation results will be given. Finally, conclusions will be drawn in section 5.

II. READ-OUT CIRCUITS

The read-out circuitry within a conventional APS is shown in fig. 1. Three transistors M1..M3 are included

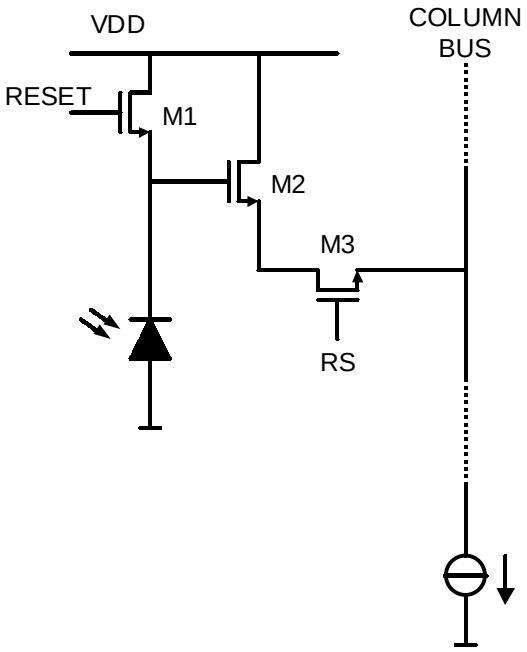

Figure 1. Conventional APS in-pixel read-out circuit

inside the pixel. A capacitive node, consisting of the capacity of the photodiode combined with the parasitic gate and overlap capacitances of the connected transistors M1 and M2, collects the photocurrent. After a certain integration period, the collected charge is read out using M2 and M3. M3 is used as a switch, operated by the RS (Row Select) signal, and connects the pixel to a bus that is shared by all pixels in one column. M2, together with a bias current source connected to the column bus, functions as a source follower. Finally, after readout, a reset signal connected to transistor M1 resets the capacitive node to a high voltage.

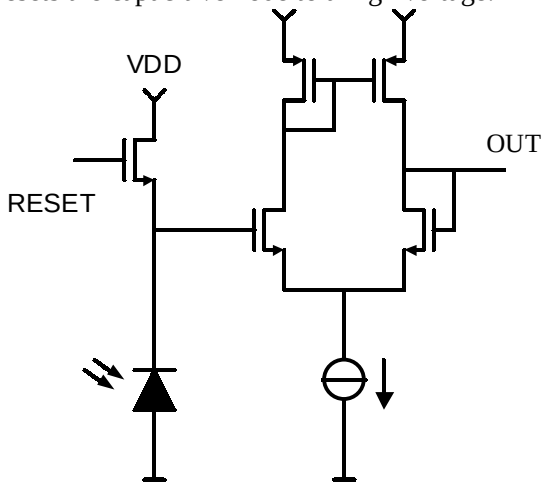

Figure 2. Read-out circuit using a pmos mirror opamp

The limitations of this read-out circuit mainly consist of the fact that only one active transistor (M2) is used. Due to the backgate effect, the gain depends of the input voltage. Any mismatch in transistor M2 between different pixels will therefore cause not only offset, but also gain errors.

The main requirement for an improved read-out circuit is gain accuracy. As widely known, the best

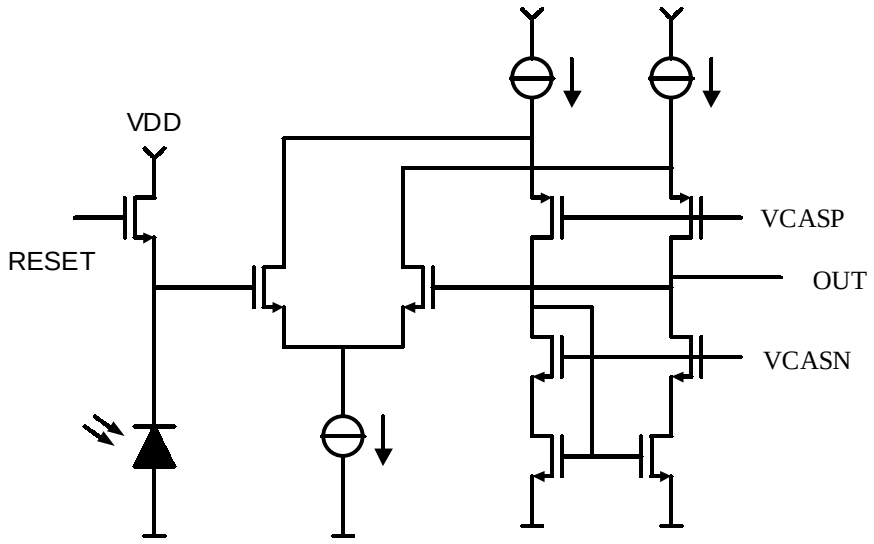

Figure 3. read-out circuit using a folded-cascode opamp

approach for this is to use a high gain amplifier combined with an accurate feedback network. We therefore consider two simple opamp structures, as depicted in figure 2 and 3. In figure 2, a very simple opamp with a pmos mirror is shown. The folded-cascode opamp of figure 3 is slightly more complicated, but can offer more gain. Both opamps are robust and easy to implement. The feedback network is in both cases a simple wire, as a gain of 1 is desired because of the large signal swing of the input (about 1 V).

III. Implementation

The limited amount of chip area is the prime constraint in implementing the proposed circuits. Current image sensors in 0.35 µm CMOS technology have a pixel whose dimensions are in the order of 7 x 7 µm [3], which leaves very little room for circuitry. Therefore, it is undesirable to put the complete opamp structure in-pixel, as the resulting increase in area would make the sensor too expensive. Therefore, a distributed approach has to be taken, where a certain part of the opamp circuit is implemented inside the pixel, while the rest is in the column circuitry, and is thus shared by all the pixels of a column. Since the inclusion of n-wells in the pixel (next to already existing p-wells) takes a lot of space, no PMOS transistors can be included inside the pixel.

A number of parasitic effects have to be considered when deciding on the partitioning between column and pixel:

- When the differential pair of the amplifier is divided between pixel and column, this can result in higher offset, and lower CMRR and PSRR.
- Care must be taken to ensure enough isolation between the highly sensitive capacitive node on which the photo charge is stored and the column line. Parasitic coupling through overlap capacitances of the input transistor could cause crosstalk.
- Since column lines will be long, they will add a lot of parasitic capacitance. Therefore, the node at which the opamp is divided has to be robust for capacitive load.

Since the aforementioned effects are hard to estimate using simulations, several different configurations will be implemented in silicon to evaluate the parasitic effects. The issue of isolation between capacitive node and column lines can be solved by adding switches that isolate the input during the integration period.

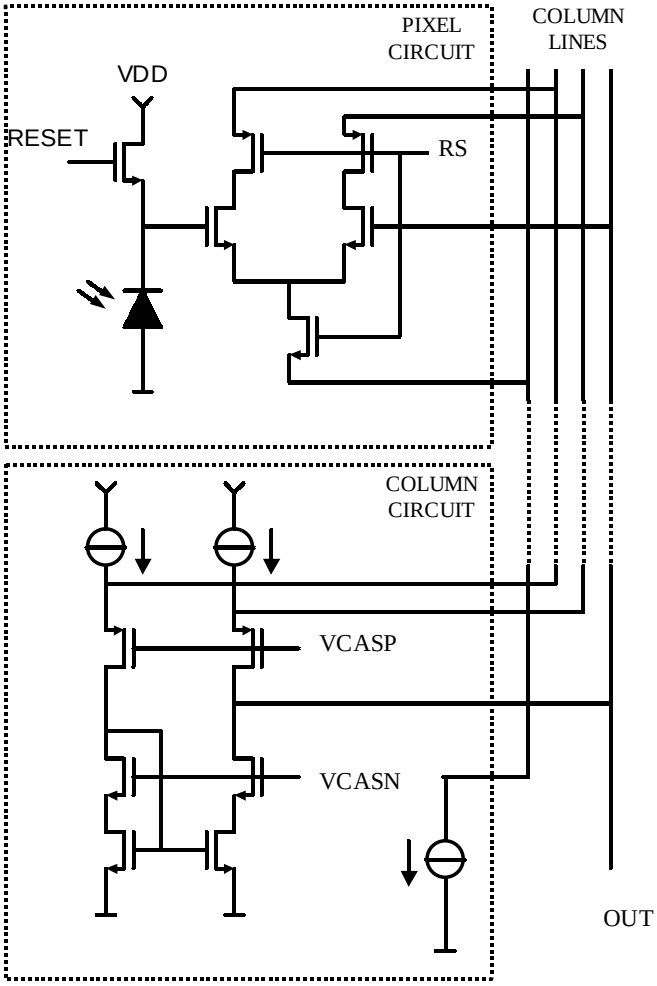

Figure 4. Example of possible implementation of the folded-cascode opamp read-out circuit

Fig. 4 gives an example of a possible implementation. Here the folded-cascode opamp of fig. 3 is divided between pixel and column circuits. Only the differential input pair is inside the pixel, while the rest of the opamp is put in the column circuit. Several switches, connected to RS (row select), are added, which isolate the pixel from the column lines when it is not read out. In this case, only 3 nmos transistors are needed inside the pixel, while 2 extra column lines are necessary. Other configurations are also possible and will be implemented as a part of this research.

IV. Simulations

Simulations have been performed to estimate the reduction in fixed-pattern noise. Since it is very hard to estimate parasitics related to the necessary partitioning of the opamp circuits as described in the previous section, this partitioning is not taken into account in the simulations.

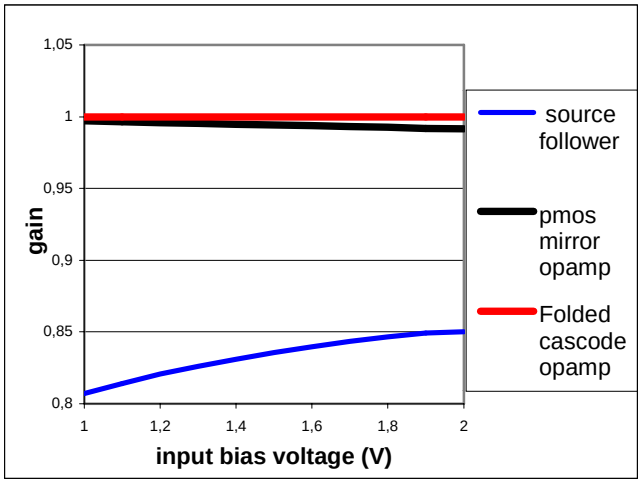

Figure 5. Plot of the amplifier gain vs. input bias voltage

For the performance of the pixel amplifier itself, the linearity is of prime importance. In figure 5, a plot is shown of the simulated gain variation vs. the input voltage. As can be expected, the open loop gain of the opamps combined with the negative feedback ensures a more accurate transfer. Therefore, both opamps are about a factor of 32 dB less sensitive to a change in input bias voltage than the source follower circuit.

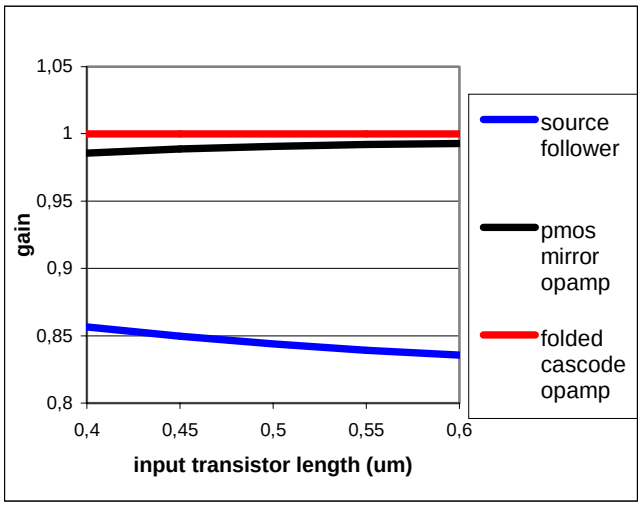

Figure 5. Plot of the amplifier gain vs. geometric variation

The most important performance parameter for the read-out circuits is the sensitivity to geometric mismatch, as this will cause fixed pattern noise. In figure 6, gain variation is plotted for a variation in the length of the input transistors. Compared to the source follower, a reduction in sensitivity by a factor of 16 dB can be obtained by using the folded-cascode opamp.

In both opamp designs the matching of the input transistors is of influence on the results. The simulation results of fig. 5 assume 100% matching of this input pair, which of course is not entirely realistic. Although some estimation can be obtained using the matching parameters of the used process, a silicon implementation is necessary to fully evaluate the opamp circuits. However, when the differential pair of the opamps is implemented inside the pixel, it will always have a better matching than that of transistors between different pixels. Thus, using the proposed read-out circuits will always have an advantage compared to the conventional read-out circuitry.

V. Conclusion

New read-out circuits for a CMOS active pixel image sensor have been presented. By using opamp structures combined with negative feedback, higher gain accuracy can be obtained than a conventional read-out circuit. Because of the use of feedback, the read-out circuits are less sensitive to process variations, which decreases the fixed-pattern noise. Simulation results show that gain variance due to variation in biasing and geometric variation can be reduced by a factor of 32 and 16 dB, respectively. Implementation in silicon will be necessary to fully evaluate the advantages of the proposed circuits, as some parasitic effects are hard to predict with simulations. Work on such an implementation is ongoing at this moment.

Acknowledgement

The authors would like to thank Philips Semiconductors for their support of this research project. In particular, the help of Adri Mierop on the implementation is appreciated.

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