

# Frame Transfer CCDs for Digital Still Cameras: Concept, Design, and Evaluation

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**Abstract**—Digital still cameras are becoming a widely used alternative for conventional silver-halide cameras. This paper presents first the concept of frame-transfer CCD imagers designed for consumer digital cameras. Next, the different modes of operation are explained in detail and compared with alternative approaches. Finally, extensive evaluation results on four different imagers using this new concept are presented. It will be demonstrated that the flexible modes of operation, the high dynamic range, and excellent optical properties of FT-CCDs make them very suited for this type of electronic imaging.

**Index Terms**—Charge coupled devices, color, image sampling, image sensors, sensitivity.

## I. INTRODUCTION

THE global market of consumer digital still cameras (DSCs) has grown from 2.5 million cameras in 1997 to 10 million in 2000. Imaging resolutions have increased from 125 k pixels in 1995 (Casio QV10 DSC) to 5M-pixels in 2001 [1].

The demand for increasing resolution and low imager cost requires a decrease of the pixel size to limit the image diagonal to about 10 mm (2/3" optical format). Pixel areas have decreased more than a factor of five, from about  $7.4 \times 7.4 \mu\text{m}^2$  in 1/3" VGA sensors in 1995 to  $3.15 \times 3.15 \mu\text{m}^2$  in 3 M-pixel sensors in 2000 [2]. Pixels as small as  $2.4 \times 2.4 \mu\text{m}^2$  have been demonstrated [3].

In a DSC, the primary function of a CCD (or CMOS) imager is to replace the silver-halide film as image capture medium. In addition, camera functions such as autofocus and exposure control, previously handled by additional sensors, can now be performed by the solid-state imager in combination with a digital signal processor (DSP). Finally, the imager, together with an LCD display, can replace the optical viewfinder.

It will be illustrated that the CCD concept presented here is well suited to fulfil all of the above requirements.

The paper focuses on the following topics: the concept of a FT-CCD imager optimized both for best quality still-imaging and for optimal camera functions (Sections II and III), detailed description of several modes of operation (Sections IV through

TABLE I  
OVERVIEW OF CCD IMAGERS FOR DSC PRESENTED IN THIS PAPER

Sensor type	FXA1012	FXA1013	FXA1022	FXA1023
Size	2/3"	2/3"	1/2"	1/1.7"
Image diagonal	11.0mm	11.0mm	8.0mm	8.8mm
Resolution	1600x1280	2000x1600	1660 x 1240	2000 x 1500
Pixel size	$5.1 \mu\text{m} \times 5.1 \mu\text{m}$	$4.1 \mu\text{m} \times 4.1 \mu\text{m}$	$3.9 \mu\text{m} \times 3.9 \mu\text{m}$	$3.6 \mu\text{m} \times 3.6 \mu\text{m}$
Color filters	RGB Bayer	RGB Bayer	RGB Bayer	RGB Bayer
microlenses	no	yes	yes	yes
Storage lines	298	250	260	260
Chip size HxV	$9.49 \text{mm} \times 9.32 \text{mm}$	$9.49 \text{mm} \times 8.67 \text{mm}$	$7.75 \text{mm} \times 6.72 \text{mm}$	$8.50 \text{mm} \times 7.38 \text{mm}$

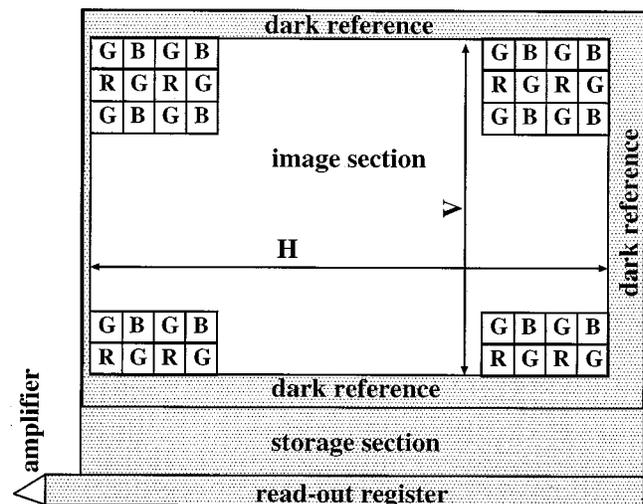


Fig. 1. Basic concept of a frame-transfer CCD imager optimized for DSC applications.

VII), an overview of the four different imagers that were manufactured (Section VIII) and full evaluation results on these CCDs (Sections IX through XII). Table I gives the major design data for the four devices.

## II. CONCEPT OF FT-CCD IMAGER FOR DSC

The basic architecture of a FT-CCD imager for DSC is presented in Fig. 1 [4]. It contains an image section, a storage section with a reduced number of lines, a readout register, and an output amplifier. The primary function of the CCD is to generate the best quality, full-resolution, single-shot image which is then stored in the camera memory. This image, typically with a resolution of 2 to 3 million pixels, is obtained by first exposing the CCD to the scene through the camera lens, then closing the camera mechanical shutter and finally reading out the image, through the storage section and the readout register. The storage

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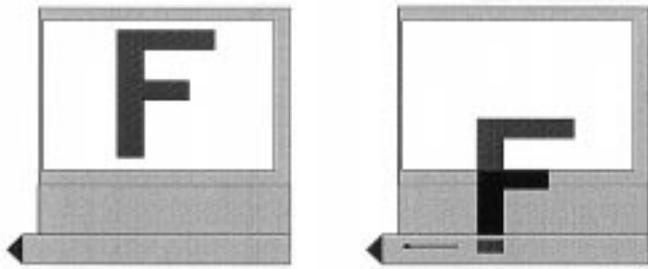


Fig. 2. Concept of full-resolution readout.

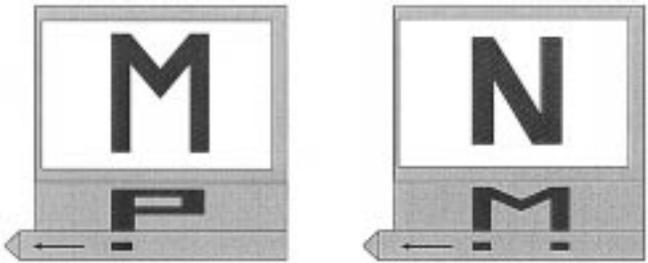


Fig. 3. Concept of subsampled continuous video readout.

section is not required in this mode of operation, as the generated image is shielded from light during readout by the camera mechanical shutter, Fig. 2. Typical pixel rates are 18 to 25 MHz; allowing frame rates of five to ten images/s.

The secondary function of the CCD is to generate scene information which can be used, prior to the capture of the full-resolution image, for camera functions such as autofocus, autoexposure, and electronic viewfinder. For most of these auxiliary functions, the maximum full-resolution image capture rate of five to ten images/s is not sufficient and the use of a mechanical shutter is not obvious. A significantly higher image capture rate of 20 to 40 images/s can be obtained by performing on-chip data reduction by decreasing the vertical resolution. In this new mode of operation, first a full-resolution image is integrated. Then, during the frame shift, the vertical resolution is reduced by subsampling at the image-to-storage transition. The image with reduced vertical resolution is then stored in the storage section and read out through the camera DSP to e.g., a LCD monitor or used for autofocus and autoexposure information. Fig. 3 summarizes this new functionality. The presence of a storage section allows continuous video output: one image is read out of the storage section, while the next image is being integrated in the image part of the device. The camera mechanical shutter remains open, the captured image is shielded from light once it is transported into the storage section. This paper will show how the flexibility of this vertical subsampling action that can be selectively turned on at the image-to-storage transition, is an important feature in CCDs for DSC.

### III. BASIC CELLS OF A FT-CCD FOR DSC

Fig. 4 shows a top view and a cross section of the image pixel of the CCD imager. For the devices discussed here, the square pixel has a dimension between  $5.1 \times 5.1 \mu\text{m}^2$  and  $3.6 \times 3.6 \mu\text{m}^2$ . A four-phase electrode (A1..A4) structure is

adopted, using two layers of thin transparent membrane polysilicon with vertical shunt wiring [3]. The vertical npn-structure ensures good highlight handling: blooming is prevented by using the n-substrate as a vertical overflow drain (VOD) [5]. A profiled n-channel CCD doping structure results in a high charge capacity [6]. Fig. 5 shows the resulting potential profile versus depth in silicon, both under the center of the two “high” gates and under the center of the two blocking gates, during integration, for an “empty” pixel. Electronic shuttering is performed to define the start of the exposure time by giving a positive pulse on the n-substrate (VNS), while all four image gates are at the low level. This completely removes the local potential maximum, as shown in curve (3) of Fig. 5, ensuring that all electrons previously collected in the image pixels will be drained to the n-substrate. The storage cell is identical to the image pixel, except for the light shield and a higher dose of the p-well, to prevent charge loss to the n-substrate. The storage electrodes are labeled B1–B4. The readout register also uses a four-phase structure, using the same two layers of thin polysilicon. The output amplifier is a three-stage source-follower.

### IV. OPERATION IN FULL-RESOLUTION MODE

The pulse diagrams for full-resolution image capture and readout are shown in Fig. 6. At the start of the exposure cycle, an electronic shutter action is performed: all image gates are turned to the low level and a positive pulse is given to the n-substrate (Vns). During image capture, two image gates are at the high voltage level, the two other gates are at the low level. At the end of the exposure time, the mechanical shutter closes and the charge packets are transferred from the image section, through the storage section, to the readout register. The image and storage electrodes are fully synchronised. The next integration cycle can start with a new electronic shuttering as soon as the last image line has been moved into the storage section. The storage cells are not reset: two storage gates are high and the higher p-well dose maintains a sufficient barrier to the n-substrate. At 25 MHz pixel clock, five to ten full-resolution images/s can be generated.

Note that one single progressive-scan image is readout, contrary to most high-resolution IL-CCDs, where two consecutive interlaced fields need to be read out to overcome the limited charge capacity of the interline CCD registers (“frame interline mode”).

### V. BASIC OPERATION IN MONITOR MODE

In monitor mode, after the image exposure, the collected charge from selected lines of the image section is rapidly transported to the storage section, while the charge from the other image lines is removed to the n-substrate. This on-chip reduction of the vertical resolution is referred to as “subsampling.” Typical subsample ratios for the devices considered here are 2:10, 2:12 or 2:14; i.e., the charge of two out of every ten, twelve or fourteen lines is transferred to the storage section, the charge of the remaining eight, ten, or 12 lines is dumped to the n-substrate at the image-to-storage transition during the frame shift. A typical vertical clock frequency is 1.5 MHz. About 20..40 images per second with 250 lines resolution can

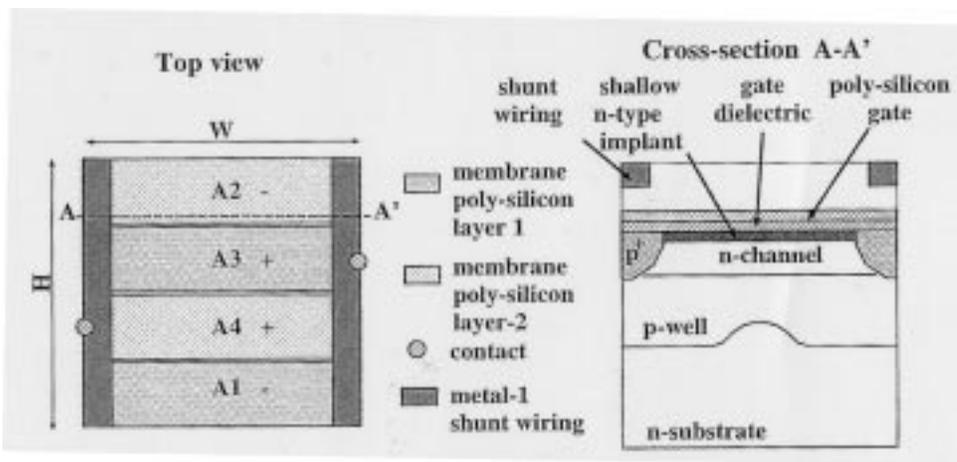


Fig. 4. Basic image pixel structure.

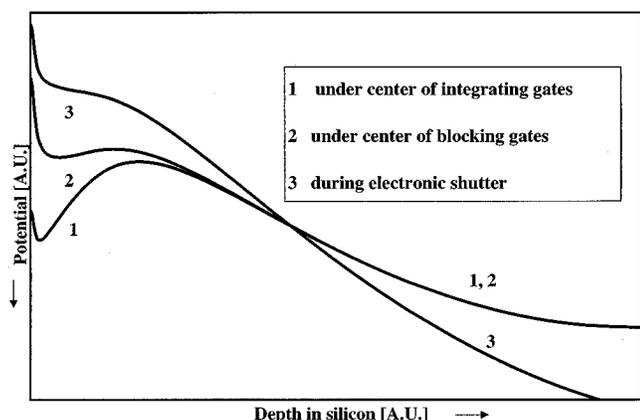


Fig. 5. Potential profile in FT-CCD imager: 1) under center of integrating gates; 2) under center of blocking gates; and 3) in electronic shutter condition.

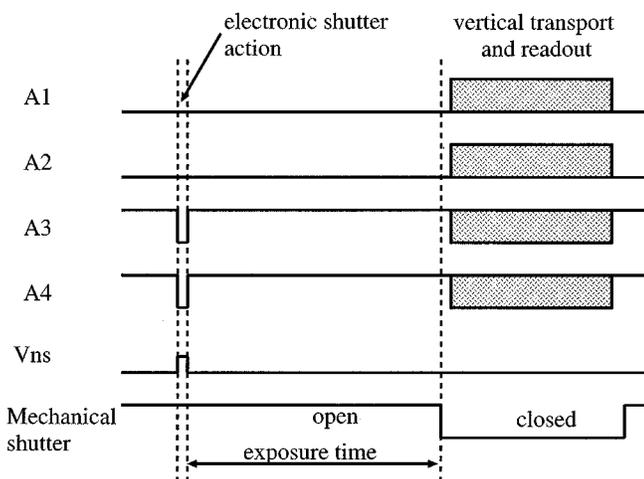


Fig. 6. Pulse diagrams for full-resolution imaging.

be generated at 25 MHz readout frequency. Fig. 7 presents a top view of one column of the imager, near the image-to-storage transition, as a function of time. Fig. 8 shows the corresponding pulse waveforms for the image and storage clocks. For illustration, a 1:2 subsample ratio is shown. Charge packet Q1 is transported to the storage section and stored under gates B3 and B4. Then the storage clocks are halted, with gates B1 and

B2 low. Charge packet Q2 eventually arrives under the last A4 image gate. When the A4 gates are pulsed low, charge packet Q2 will be drained to the n-substrate, using the VOD structure. This is essentially the same action as electronic shuttering, except that it is performed only locally, at the image-storage transition. Several precautions were taken in the design to avoid mixing of Q2 with either Q1 or Q3 at this stage, as can be seen from Fig. 9 where a top view of one column of the imager at the image-to-storage transition is shown. The length of the “blocking gates” [A3 and (B1 + B2)] was increased to ensure good and equal separation forward (to Q1) and backward (to Q3) and the length of the last A4 gate was increased so that it can hold the maximum charge packet Q2 even with A3, B1 and B2 ‘low’. In addition, the n-channel and p-well layout under A4 were modified to ensure a local potential maximum and a smaller barrier to the substrate. When Q2 has been dumped, the following charge packet Q3 is transferred to the storage section by synchronising again the B clocks with the A clocks, etc. Fig. 10 shows the corresponding pulse waveforms. The RGB Bayer color filter pattern is maintained. During the combined frame shift and subsampling, the ‘electronic shutter pulse’ is applied to the n-substrate, as it is required to dump the charge packets at the image to storage transition. Because of this pulse, the maximum charge capacity in monitor mode is about 25–40% smaller than in full resolution mode: the overflow barrier (Fig. 5) for charge packets that are not dumped is reduced. However, the dynamic range still exceeds the requirements for this mode of operation.

## VI. ALTERNATIVE SUBSAMPLE SCHEMES

In literature, other vertical subsampling schemes have been proposed. Only the approach most used in IL-CCDs for DSC will be shown for comparison Fig. 11, [7], [8]. Most of these high-resolution CCDs for DSC have four-phase interline registers. One four-phase cell of the interline register is designed per two photodiodes, which implies that interlaced readout is required in full resolution mode. After the mechanical shutter has closed, first the photodiodes of all odd lines are read into the interline register by a high pulse on the V1 clocks and readout in the conventional method. To obtain the second field, the V3

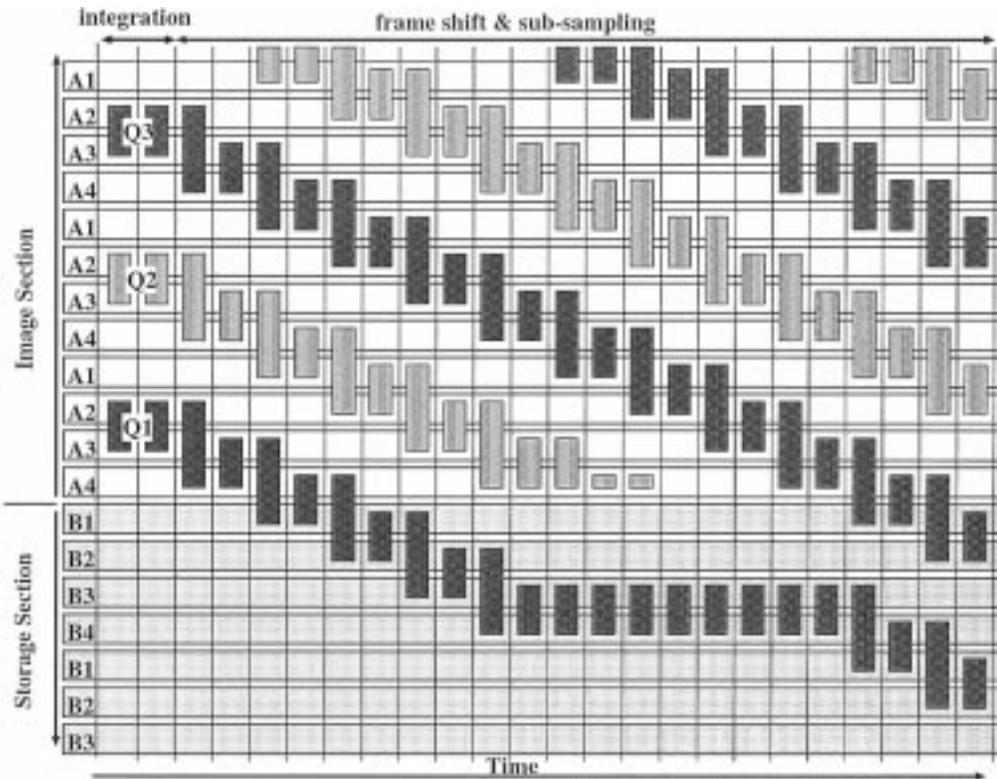


Fig. 7. Top view of one column of the CCD imager during subsampling. The horizontal axis is a time scale.

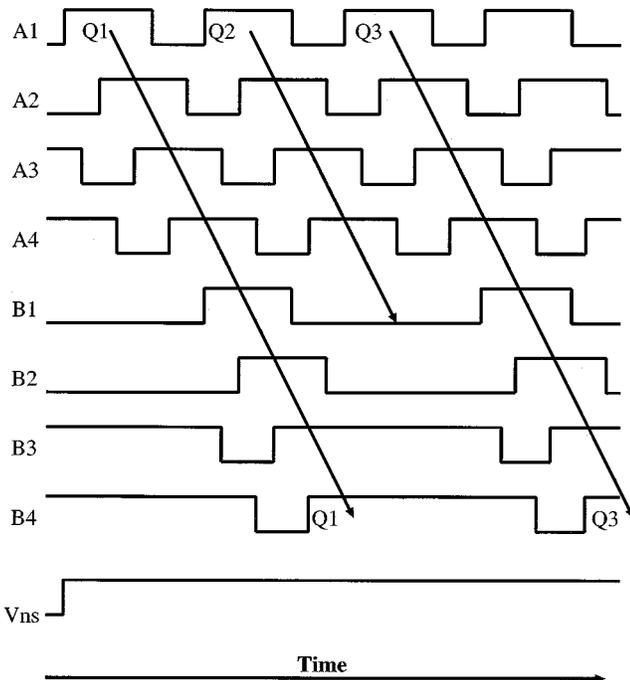


Fig. 8. Pulse pattern for image and storage electrodes during subsampling.

clocks are pulsed high to read out the even lines. This four-phase interlaced approach is chosen for optimal charge capacity. To obtain subsampled images, the V1 and V3 electrodes of the interline register are split into several parts (e.g., V1A, V1B; V3A, V3B). This allows the readout of a reduced number of lines only, in progressive-scan readout mode. The major disadvantage of

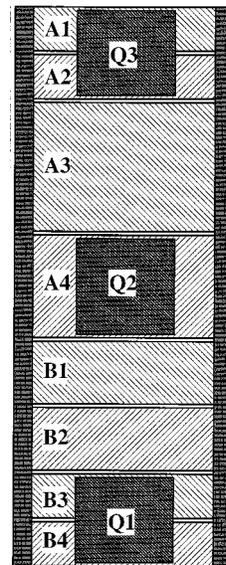


Fig. 9. (Top view) Schematic design of image-to-storage transition, optimized for subsampling.

the concept of Fig. 11 is the lack of flexibility: the subsample scheme is completely determined by the design.

## VII. ADVANCED MODES OF OPERATION

In the concept presented here, the subsampling is defined by the pulse patterns applied to the image and storage electrodes, not by the design. As a consequence, a wide range of possibilities exist to reduce the vertical resolution at the image-to-storage transition. This can generate interesting features for the DSC

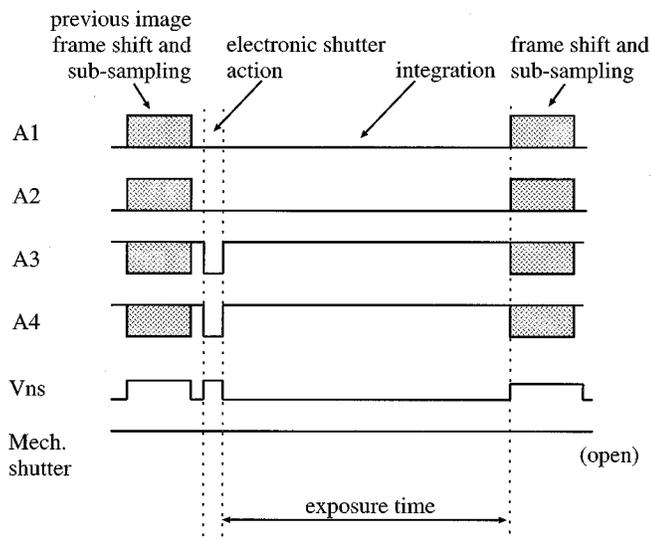


Fig. 10. Pulse patterns for total imaging cycle in subsampling mode.

cameras in which the CCD is used. A few examples are presented here.

#### A. Fast Autofocus on the Center of the Image

Fig. 12 shows an example of fast autofocus on the center part of the image. Only the middle 60 image lines are transferred to the storage section. The preceding lines are dumped at the image-to-storage transition by subsampling. When the charge from the selected lines has been stored in the storage section, the contents of the subsequent lines are cleared by the electronic shutter action. This mode allows a very high frame rate, e.g., at 25 MHz pixel clock and 2000 pixels/line, 120 frames/s of 60 lines can be obtained. Selecting different, multiple areas to obtain autofocus information is of course also possible. The same principle can be used for autoexposure measurements on predefined lines of the imager.

#### B. Vertical Binning

At low light levels in full resolution mode, the exposure time can be increased to match the illumination of the scene, without any other constraint than the maximal level of dark current that is acceptable. However, in monitor mode, an image capture rate between 15 to 30 images/s is required for comfortable viewing on an LCD monitor. This of course limits the exposure time to 1/15 or 1/30 s. To increase the sensitivity in monitor mode for low exposure scenes, vertical charge binning is possible [9]. Fig. 13 shows the principle of sensitivity increase by subsampling with a 2:6 subsample ratio combined with charge binning: charge from “blue” and “red” lines is added selectively. Only one column of the imager is shown. First the charge from two odd lines is added (1+3), while the charge from line 2 is dumped, then the two next even lines are added (4 + 6) while the odd line five is dumped. The RGB Bayer color filter pattern is maintained in the resulting image, which contains 2/6ths of the original number of image lines but is composed from the information from four out of six image lines. Table II shows the possible binning factors as a function of subsample ratio.

## VIII. OVERVIEW OF CCD IMAGERS

Table I already showed the overview of four different CCD imagers for digital still cameras that are presented here. Table III shows the typical operating conditions for these sensors.

## IX. EVALUATION RESULTS

In this section, the evaluation results of the imagers described above will be presented. All aspects of sensor performance relevant to the use in DSC camera systems will be presented.

### A. Pixel Evaluation

**Charge Capacity:** The charge capacity of CCDs with small pixels is an important competitive issue, as it determines (together with the noise floor) the dynamic range of the image. For “movie applications” (camcorders, security cameras), eight-bit dynamic range is often sufficient. However, for high-quality photo prints, a dynamic range in excess of ten bits is desirable. Contrary to movie applications where photon shot noise is not relevant because of temporal averaging, it becomes a significant issue for CCDs with small pixels. As an example, a CCD with a maximum charge capacity of 15 000 electrons will be set to operate at a working point (average exposure level) of 10 000 electrons or less. The photon shot noise will be the square root of this, i.e., 100 electrons, or already at least 1% of the signal level.

Table IV shows the maximum charge capacity in still picture and in monitor mode for the four CCDs presented here, using the typical operating conditions mentioned in Table III.

**Highlight Handling:** Efficient highlight handling through vertical anti-blooming is an essential requirement for imagers for DSC cameras. The vertical npn structure shown in Fig. 4 can handle 1000× overexposure without blooming.

**Electronic Shutter:** In a FT-CCD sensor with a vertical n-p-n structure, all charge can be drained instantaneously to the n-substrate by setting all the image electrodes to the low level and applying a pulse to the n-substrate. For the imagers presented here, a 5 V positive pulse on the n-substrate during 20 μs is sufficient to completely empty all pixels.

**Dark Current:** In CCDs used in continuous video applications, such as camcorders, the exposure time can never exceed the field time of the PAL or NTSC display, thus 1/50 s or 1/60 s is the maximum integration time. However, for still imaging applications, like for conventional silver-halide cameras, exposure times up to 1 s or longer should be possible. This requires a very low dark current level in the CCD pixels. The dark signal from the FT-CCD imager is very low: typically 0.02 nA/cm<sup>2</sup> at 30 °C. An overview of the dark signal charge at 25 °C and 60 °C at 1/15s exposure time is given in Table V. Since the dark current generation is significantly influenced by the electrical fields in the pixel and since the doping profiles in the different pixels are not entirely identical, no clear relation between pixel area and dark current generation can be observed.

Note that in a FT-CCD, the dark current generation is very low and equal during exposure and readout: both operations use the same basic CCD cell. In an IL-CCD, the pinned photodiodes can have an extremely low dark current [10], but the narrow interline registers have a high doping concentration to obtain

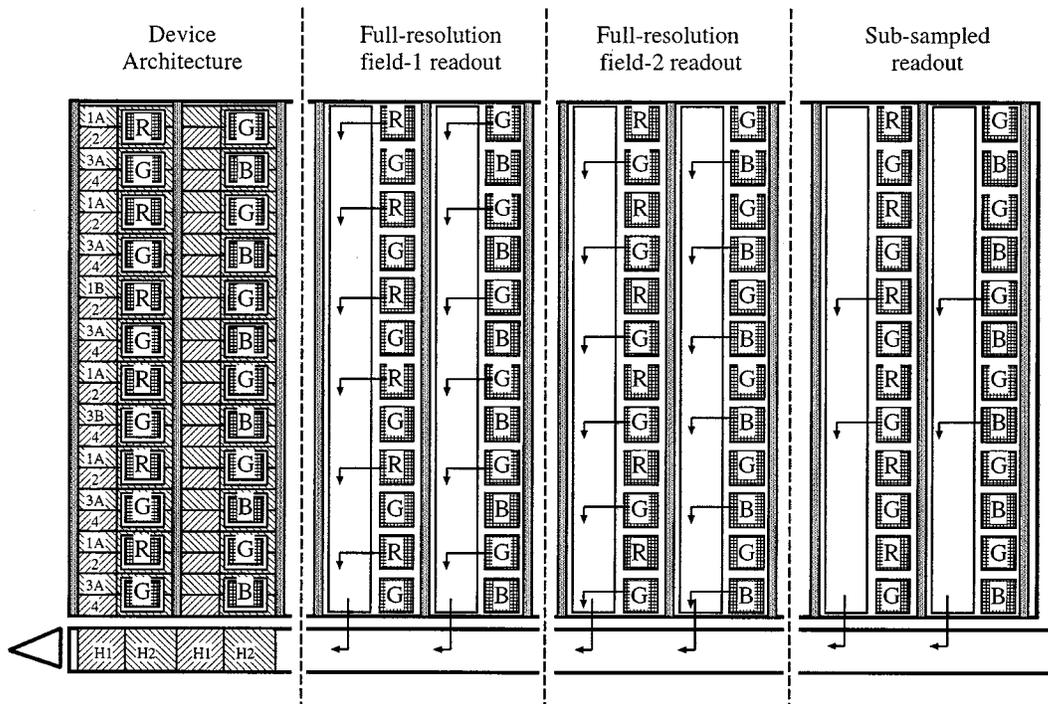


Fig. 11. Widely used subsample scheme for interline-transfer CCD imagers for DSC.

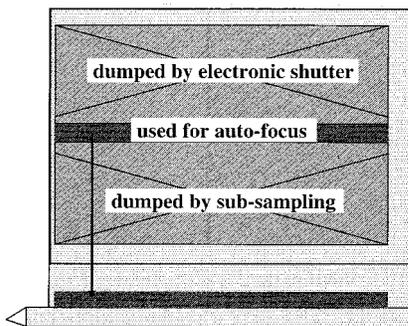


Fig. 12. Readout scheme for autofocus with FT-CCD for DSC.

a sufficiently large charge capacity. The resulting higher electrical fields and the absence of an inversion layer at the interface cause a much higher dark current generation. Table VI compares, for FT- and IL-CCD, the relative values of the dark current generation for integration (pinned photodiode for IL-CCD) and for readout (interline register for IL-CCD), as found in [11]. Though IL-CCDs have a lower dark current during exposure, clearly, for high-resolution IL-CCDs the interline-register dark current will be a serious problem with increasing resolution, as the readout time will also increase: at 18 MHz readout frequency, it takes about 1/7 s to read out one field (2.5M-pixels) of a 5M-pixel IL-CCD (frame interline mode).

**B. Evaluation of Optical Response**

*Introduction:* The optical response of the CCD image pixels was extensively evaluated. Spectral response characteristics (RGB curves), angular response and the gain obtained by the use of on-chip microlenses are presented in detail.

*Application of On-Chip Microlenses:* A schematic representation of the sensitivity of the FT-CCD pixel in horizontal and

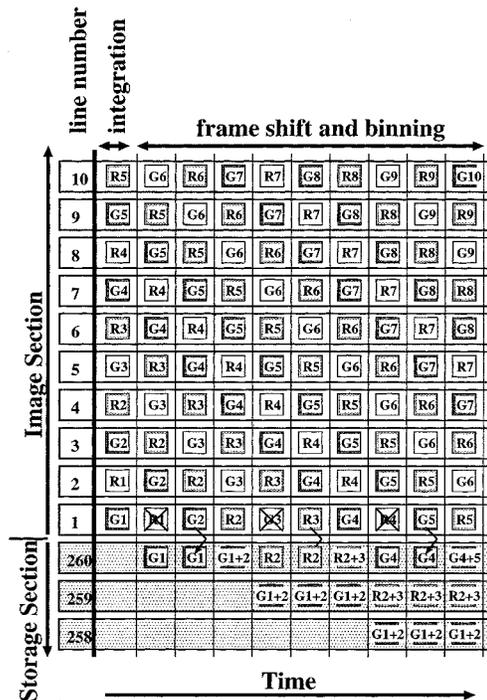


Fig. 13. Readout scheme for binning in monitor mode.

vertical direction is shown in Fig. 14. Shown is the response for a photon at each position in the pixel: The collection depth for electrons is at a maximum in the center of the pixel. In the direction of charge transport, the sensitivity decreases under the blocking gates, as can be understood from the potential diagrams of Fig. 5. In the other direction, the sensitivity is reduced to zero under the metal-1 wiring, in the p-channel stops.

TABLE II  
POSSIBLE VERTICAL BINNING FACTORS IN MONITOR MODE

Sensor type	Subsampling ratio	Achievable vertical binning
FXA1012	1:5 or 2:10	x1, x2, x3
FXA1013	1:7 or 2:14	x1, x2, x3, x4
FXA1022	1:6 or 2:12	x1, x2, x3
FXA1023	1:7 or 2:14	x1, x2, x3, x4

TABLE III  
OPERATING CONDITIONS FOR CCD IMAGERS PRESENTED HERE

Image and storage clock swing	12V
Read-out register clock swing	5V
Image and storage clock frequency	1.2MHz
Read-out register clock frequency	25MHz

TABLE IV  
MAXIMUM CHARGE CAPACITY (IN NUMBER OF ELECTRONS) FOR DIFFERENT PIXEL SIZES

Sensor Type	FXA1012	FXA1013	FXA1022	FXA1023
Pixel size	5.1 $\mu\text{m}$ $\times$ 5.1 $\mu\text{m}$	4.1 $\mu\text{m}$ $\times$ 4.1 $\mu\text{m}$	3.9 $\mu\text{m}$ $\times$ 3.9 $\mu\text{m}$	3.6 $\mu\text{m}$ $\times$ 3.6 $\mu\text{m}$
Full-resolution mode	35 000	30 000	30 000	28 000
Monitor Mode	20 000	18 000	18 000	17 000

TABLE V  
DARK SIGNAL OF CCD IMAGERS FOR DSC AFTER 1/15 s EXPOSURE TIME

Code	FXA1012	FXA1013	FXA1022	FXA1023
Dark current electrons per pixel, 25°C	4	3	3	4
Dark current electrons per pixel, 60°C	30	20	20	30

TABLE VI  
COMPARISON BETWEEN FT-CCD AND IL-CCD FOR THE RELATIVE DARK CURRENT CONTRIBUTIONS FROM INTEGRATION AND FROM READOUT (FROM [11])

Relative Dark Current	FT-CCD	IL-CCD
Integration (Pixel)	1	0.2
Readout	1	50

To maintain a sufficiently high sensitivity, microlenses were applied on pixels smaller than  $5 \times 5 \mu\text{m}^2$ . Their primary purpose is to focus the light onto the center, most sensitive part, of the CCD image pixel, [9]. Fig. 15 shows a cross section of a  $4.1 \times 4.1 \mu\text{m}^2$  pixel with color filters and microlens. Table VII shows the increase in sensitivity (for white light, 3200K, IR filtered) and the decrease of cross talk (expressed here as Gr-Gr difference at 600 nm illumination, see further) for both a  $3.9 \times 3.9 \mu\text{m}^2$  pixel and a  $3.6 \times 3.6 \mu\text{m}^2$  pixel obtained by the use of on-chip microlenses. The measurements were performed with a parallel light beam perpendicular to the CCD surface. Fig. 16 shows the improved RGB response by the application of microlenses on a  $3.9 \times 3.9 \mu\text{m}^2$  pixel.

*Angular Response:* The angular response of a CCD image pixel is very important since it determines the design of the camera lens, typically the most expensive part of the complete

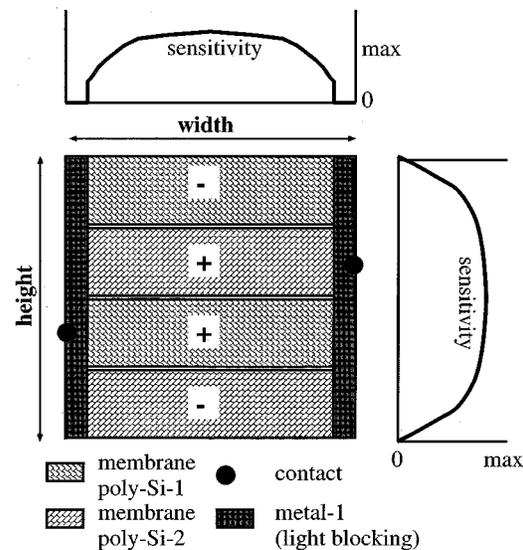


Fig. 14. Sensitivity as a function of position within a  $4.1 \times 4.1 \mu\text{m}^2$  pixel.

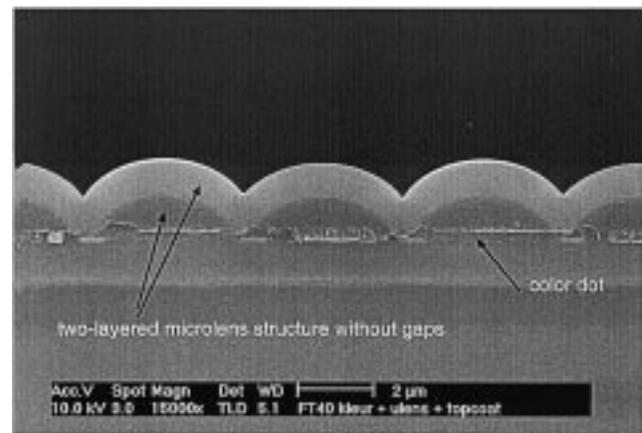
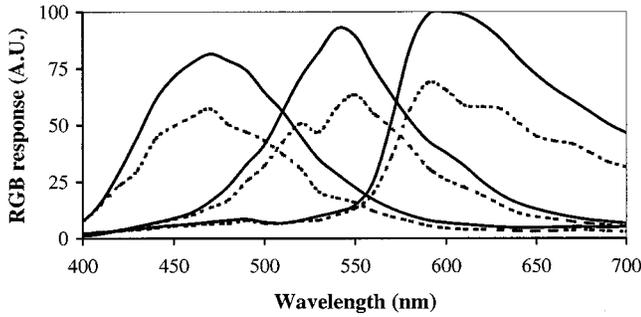
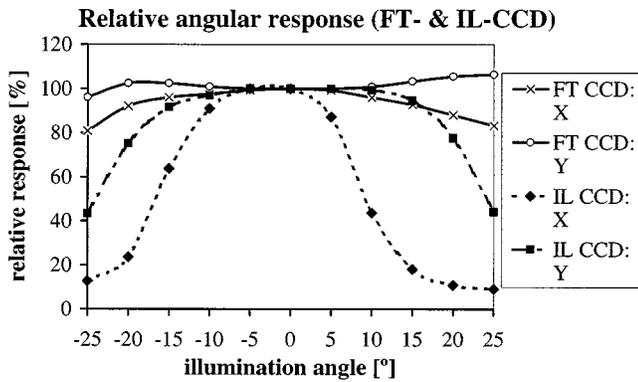


Fig. 15. Cross section of  $4.1 \times 4.1 \mu\text{m}^2$  pixel with color filter and microlens.

TABLE VII  
INCREASE OF SENSITIVITY AND REDUCTION OF CROSS-COLOR BY USE OF MICROLENSSES ON  $3.9 \times 3.9 \mu\text{m}^2$  AND  $3.6 \times 3.6 \mu\text{m}^2$  PIXELS

	3.9 $\times$ 3.9 $\mu\text{m}^2$ pixel	3.6 $\times$ 3.6 $\mu\text{m}^2$ pixel
Sensitivity Increase		
Blue	20%	35%
Green	35%	45%
Red	35%	40%
Cross-Color		
without microlens	10%	11%
with microlens	1.5%	2%

DSC camera. A wide angular response of the image pixels allows the use of a less expensive, more compact lens [11]. Fig. 17 shows the measured angular response for a  $3.9 \times 3.9 \mu\text{m}^2$  pixel FT-CCD with microlenses and results obtained on a similar, commercially available, IL-CCD. *X* means a rotation around the vertical axis, such that the light is directed to neighboring pixels across the channel stops. *Y* means a rotation around

3.9x3.9  $\mu\text{m}^2$  pixel with and without microlensesFig. 16. Increase in sensitivity by application of microlenses on  $3.9 \times 3.9 \mu\text{m}^2$  pixel.Fig. 17. Angular response plot for  $3.9 \times 3.9 \mu\text{m}^2$  FT-CCD and IL-CCD pixels, both with microlenses.

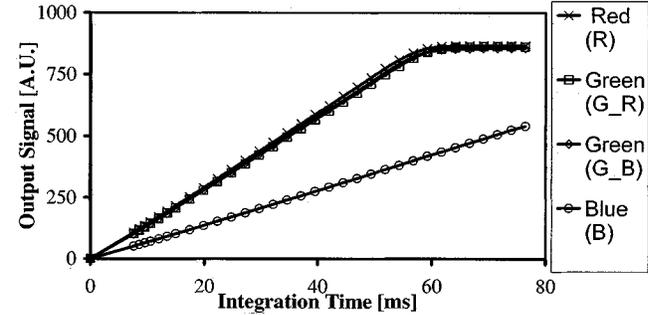
the horizontal axis, directing light to the neighboring pixels at the other sides of the blocking gates. Without microlenses, the IL-CCD typically would have a light-sensitive area of about  $2 \mu\text{m}^2$ . This explains the stronger degradation of response as a function of the angle of the incident light. Due to the presence of the interline register between the photo diodes, the angular response in  $X$  direction drops even faster and is asymmetrical. The small initial increase of response for the FT-CCD in  $X$  direction is thought to be caused by a small change in reflection and absorption in the pixel stack for nonperpendicular incident light. The wide angular response of the FT-CCD allows the use of compact, less expensive, telecentric camera lenses.

### C. Evaluation of Subsampling Efficiency

The most efficient method to measure the subsampling performance consists in comparing the RGB response in full resolution mode and in monitor mode. The sensor was illuminated with blue-green light. With “perfect” subsampling, charge dump at the image to storage transition should empty the pixels for 100%, and no charge mixing between the “dumped” and the “conserved” lines should occur. Thus, the sensitivity ratios Green/Blue and Red/Blue should be identical in subsampled mode and in full-resolution mode. As can be concluded from Table VIII, this is the case for the imagers discussed here.

TABLE VIII  
EVALUATION OF SUBSAMPLING EFFICIENCY BY COMPARISON OF COLOR RATIOS

Color ratios	$G_R/B$	$G_B/B$	R/B
Full-resolution mode	0.92	0.91	0.17
Sub-sampled mode	0.92	0.91	0.18

Linearity per color plane  
(CCD with  $3.6 \times 3.6 \mu\text{m}^2$  pixels)Fig. 18. Linearity measurement. The signals from the four color planes R,  $G_R$ ,  $G_B$ , and B are shown as a function of the exposure time.TABLE IX  
POWER CONSUMPTION OF DIFFERENT CCDS

Code	FXA1012	1/2" 2M IL-CCD
V clock swing	12V	8V
H clock swing	5V	5V
Monitor mode, 15 im/s	170mW	165mW
Full resolution, 5 im/s	170mW	190mW
H clock swing	3.3V	3.3V
Monitor mode, 15 im/s	130mW	140mW
Full resolution, 5 im/s	140mW	150mW

### X. OUTPUT AMPLIFIER

The output amplifier is a three-stage source follower [9], [12]. The capacitance of the floating diffusion detection node was minimized and the gain was maximized to achieve the highest possible conversion from charge to voltage. A conversion factor at the output node of  $35 \mu\text{V}/\text{electron}$  was realized, with a bandwidth of 85 MHz.

### XI. SYSTEM LINEARITY

Excellent system linearity is essential for reconstructing a color image from a CCD imager over a 12 bit dynamic range. The overall system to be considered for a CCD imager is the linearity from “photons in” to “mV out.” The linearity was characterized by measuring the output voltage of the different color planes (R,  $G_B$ ,  $G_R$ , B) as a function of exposure time under constant uniform white illumination. Fig. 18 shows the result: the linearity is very good.

### XII. POWER CONSUMPTION

For portable applications, power consumption should be as low as possible. For a CCD, power is consumed for driving



Fig. 19. Image obtained with 3M-pixel 1/1.7" FT-CCD.

the electrodes (image, storage, and readout register) and in the output amplifier. The use of nonoverlapping membrane polysilicon gates [3] assures low overlap capacitances, thus significantly reducing the  $C \times V^2$  power consumption [8]. When scaling the pixel to below  $5.1 \times 5.1 \mu\text{m}^2$ , special care was taken to limit the capacitances. Table IX compares the power consumption for the 1/2" 2M-pixel FT-CCD with a 1/2" 2M-pixel IL-CCD (with a four-phase vertical IL-register and two-phase horizontal clocks). For the calculation, the image rate was kept constant (implying different exposure times when changing the image resolution). The capacitance values were measured for the FT-CCD, for the IL-CCD, the "typical" data sheet values were used. Shown are the power consumption in monitor mode at 15 images/s and in full-resolution mode at 5 im/s. The power consumption is the sum of the power dissipated to drive the clocks ( $C \times V^2$ ) and the total power required for the output amplifier, including the power dissipated in the off-chip load resistor ( $V \times I$ ). Values are given for 3.3 V and 5 V amplitude of the horizontal clocks (and reset gate) pulses. Note that the high maximum charge of FT-CCD pixels combined with the small detection node capacity generates a large voltage swing on the detection node. This implies that with current process tolerances, when using 3.3 V reset-gate (RG) pulse height, the DC offset of the RG pulse may require adjustments. No other adjustments are required.

### XIII. CONCLUSIONS

The concept of a frame-transfer CCD with a reduced storage section combined with subsampling at the image-to-storage

transition is very well suited for digital still camera applications. The large charge capacity ensures a high dynamic range, even at pixel sizes of  $3.6 \times 3.6 \mu\text{m}^2$ . The flexibility of the vertical subsampling allows extra features for the DSC camera. Fig. 19 gives an image obtained with the 1/1.7" 3M-pixel CCD.

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