2.7 A CCD Image Sensor of 1Mframes/s for Continuous Image Capturing of 103 Frames

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This solid-state image sensor can capture moving images at 1Mframes/s and reproduce them for >10s at 10frames/s, which is sufficient to activate dynamic recognition of scientists and engineers. The pixel count is 312x260. The sensor is fabricated and tested to prove image quality with low noise for ultra-high-speed image capturing.

The sensor is an in-situ storage image sensor (ISIS). Each pixel of the sensor has its own in-situ image-signal storage area. During the image capturing phase, image signals generated in the photo-sensitive areas of all pixels are simultaneously recorded in the in-situ storage areas without being readout from the sensor, realizing parallel recording at all pixels and, thus, image capturing at the ultimate high frame rate. During read out after image capture, the stored image signals are read out.

Reference [1] describes a CCD image sensor of 1Mframes/s with 30 in-situ storage elements within each pixel (Figure 2.7.1). The structure of the storage area is serial-parallel-serial (SPS). The design seemed ultimately refined as an ISIS. However, it has one disadvantage, later pointed out by the authors: two-directional transfer of image signals within each small in-situ storage. First, an image signal generated in the photodiode is horizontally, then, vertically, and again, horizontally transferred.

The ISIS presented here is explained in Figure 2.7.2. Image signals generated in the photo-gate are transferred to the linear in-situ CCD storage, which is placed slightly slanted to the grid axes of the photo-gates. The one-directional transfer significantly simplifies the structure of the gates and metal wiring within the in-situ storage, compared to the SPS structure. Thus, the area of the in-situ storage is minimized and the number of stored consecutive images is maximized. The simplicity of the structure also contributes to increased yield and decreased noise. The frame rate is exactly equal to the transfer rate of the storage CCD.

The linear in-situ CCD storage is realized by the slightly slanted alignment, with angle adjusted to place the lower linear CCD storage under the upper one without wasting space. Since there is no simpler structure than the one-directional transfer, this sensor seems the ultimate design of an ISIS with CCD storage.

In the readout VCCD, a vertical drainage is installed for overwriting. During image capture, old image signals are continuously drained to the substrate, and the latest ones are successively stored in the linear in-situ storage. The operation continues in parallel at all the pixels until a trigger signal is released to stop image capture, immediately after occurrence of a target event. The overwriting function works efficiently for synchronization of image capture to occurrence of a target event.

In readout, one vertical CCD channel at the left end of each storage area works as the readout CCD. The readout is as follows:

(1) Charge transfer stops in the linear CCD storage areas. The operation transfers only image signals stored in the readout VCCD to HCCD placed below the photo receptive area. The readout VCCD becomes empty.
(2) Image signals in the storage are transferred to the readout VCCD until it is filled with signals. The cyclic operation of (1) and (2) continues until the storage and the readout VCCD become empty.

For cyclic readout operation, a storage CCD and a neighboring readout VCCD are operated independently. A CCD element at the end of a linear in-situ storage, which is the top of a readout VCCD segment of each pixel, works as a switch, which controls to transfer charge packets from either the linear CCD storage or from the upper readout VCCD segment to the lower readout VCCD segment.

To simplify the structure of the switching CCD element, a structure and an associated operation are introduced. The test sensor employs the 4-phase transfer to keep sufficient charge-handling capacity. It requires a set of 4 metal wires to increase transfer rate. To independently operate the readout VCCD, 4 metal wires should be placed on the one VCCD channel, resulting in closely spaced adjacent metal wires. Small distance between metal elements significantly reduces yield rate.

This scheme requires only two additional metal wires on the readout VCCD of the four-phase transfer, as is explained in Figure 2.7.3. The linear CCD storage is operated with a set of four electrodes, A1, A2, A3 and A4, while the readout VCCD with A1, B2, A3 and B4. Two of four electrodes A1 and A3 work in common, and two additional electrodes, B2 and B4, are placed on the readout VCCD, instead of A2 and A4.

Transfer voltage patterns for A1 and A3 are the same as the standard four-phase transfer. When voltage patterns for A2 and A4 (or B2 and B4) are the same as the standard ones, charge packets are simply transferred (Figure 2.7.3a).

If the voltage of A2 (or B2) is fixed at the higher level and that of A4 (or B4) at the lower level, A4 (B4) works as a blocking gate and A2 (B2) as a reserving gate, and a charge packet is kept beneath [A1 and A2] or [A2 and A3] (or [B1 and B2] or [B2 and B3]) alternately (Figure 2.7.3b). Consequently, without B1 and B3, the linear CCD storage and the readout VCCD are independently operated either as transfer CCD or as storage CCD.

Curving design is introduced to as many elements as possible of the test sensor, instead of rectangular design, which results in more natural potential profiles, milder corners on the masks, etc. The non-rectangular design is largely supported by a 3D device simulation software “SPECTRA”. Figure 2.7.4 is a micrograph of the sensor.

Design specifications of the test sensor are shown in Figure 2.7.5. Example images are shown in Figure 2.7.6. The image is a breaking balloon taken at 100kframes/s.

A triple-ISIS camera under development provides either a color version with 243,360 pixels, or a monochrome version which captures consecutive 309 images, reproducing a moving image of more than ten seconds at 30frames/s.

Reference:

[1] F. W. Kosonocky et al., “360x360-Element Very High Frame-Rate Burst Image Sensor”, ISSCC Digest of Technical Papers, pp.182-183, 1996.

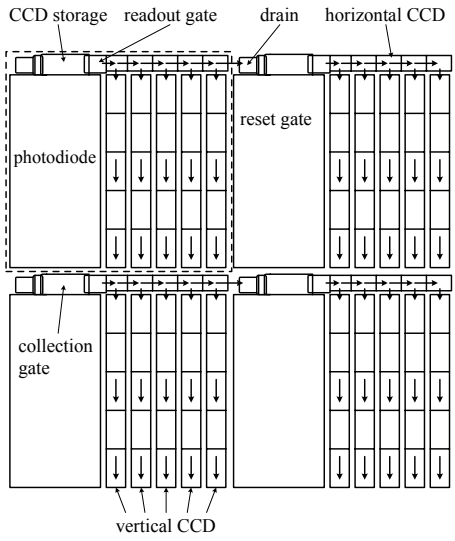


Figure 2.7.1: A burst image sensor: ISIS with the SPS CCD Storage (Kosonocky et al. 1996).

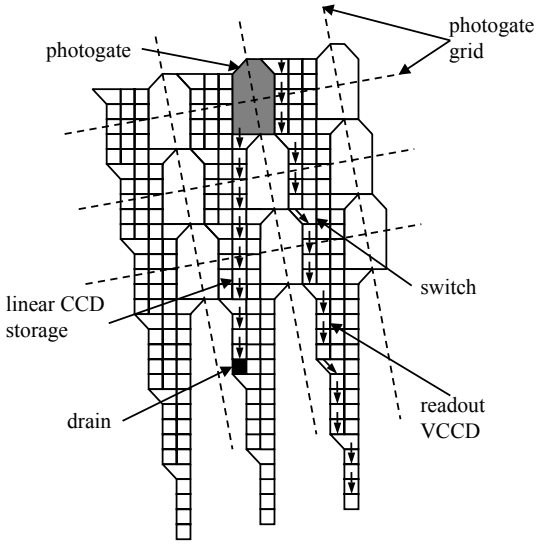
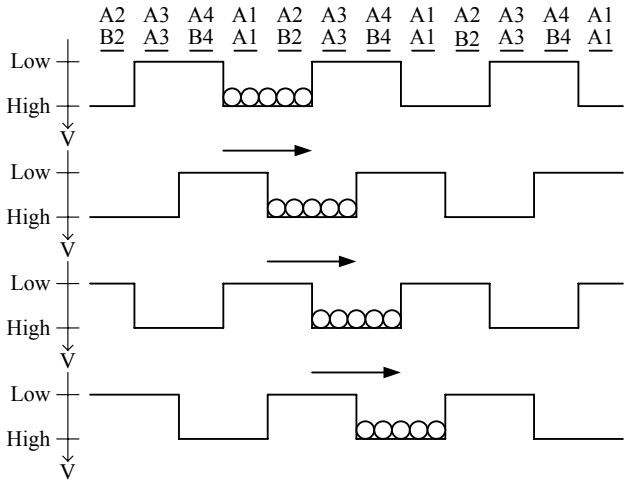
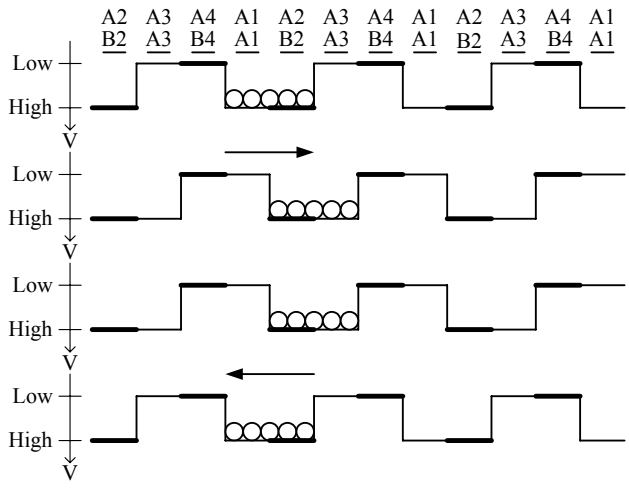


Figure 2.7.2: Elements of an ISIS with slanted linear CCD storage.



(a) Transfer phase



(b) Reservation phase

Figure 2.7.3: Operations of two adjacent CCD channels of 4-phase transfer.

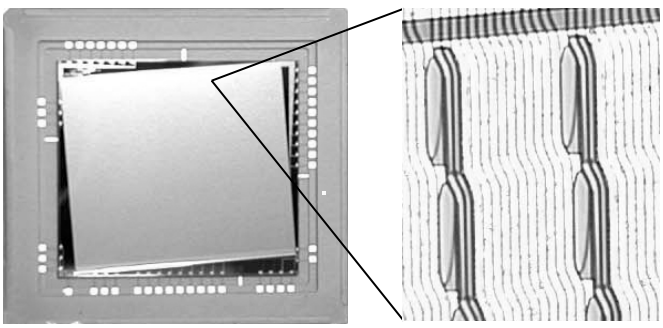


Figure 2.7.4: Micrograph of the fabricated sensor (upper part).

Frame Rate	1,000,000 frames/s (max)
Pixel Count	312x260 (=81,120) pixels
Pixel Size	66.3x66.3μm^2
Size of CCD Element	5.1x5.1μm^2
Fill Factor	13 %
Number of Stored Image	103 frames
Charge Handling Capacity	40,000 electrons
Grey Level	10b
On-chip Color Filter Array	None
Overwriting Drain	Installed
Transfer Scheme	4-phase transfer (Quasi 2-phase transfer for HCCD)

Figure 2.7.5: Design specification of the test ISIS.

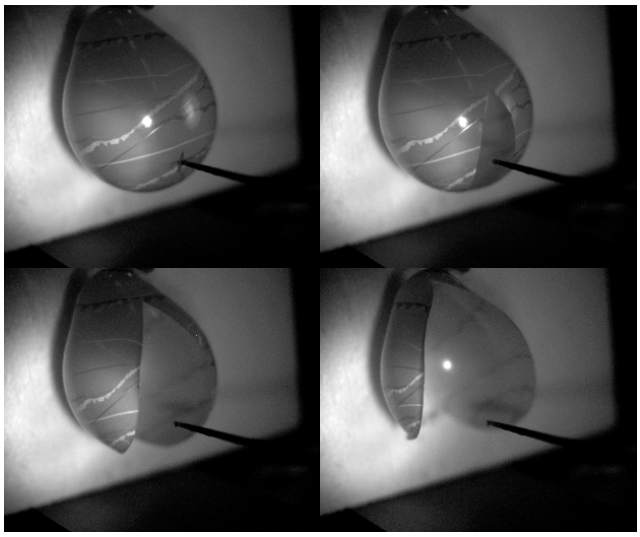


Figure 2.7.6: Images of a breaking balloon captured at 100k frames/s.

