2.1 A 1/1.8" 3M Pixel FT-CCD with On-Chip Horizontal Sub-Sampling for DSC Applications

Laurent Le Cam, Jan T. Bosiers, Agnes C. Kleimann, Harry C. van Kuijk, Joris P. Maas, Monique J. Beenhakkers, Herman L. Peek, Peter C. van de Rijt, Albert J. Theuwissen[1]

Philips Semiconductors Image Sensors, Eindhoven, The Netherlands
[1]also with Delft University of Technology, Delft, The Netherlands

Charge-coupled device (CCD) imagers used in mega-pixel digital still cameras (DSC) usually have two different modes of operation. In snapshot mode a full-resolution image is captured and stored. In preview mode vertically sub-sampled images are generated for other camera functions that do not need full resolution, such as liquid crystal display preview (viewfinder), auto-focus or video clip [1]. With sensor resolutions now above 2M pixels, readout time in this second mode easily exceeds 1/30s. This drastically limits the functionality for viewfinder or video clip imaging. This on-chip horizontal sub-sampling allows more camera flexibility by doubling the readout rate of the device without changing the readout frequency and can be turned 'on' or 'off' simply by the timing generator.

Horizontal sub-sampling with binning is introduced in a 3M pixel 1/1.8" 2000 (H)x1500(V) frame-transfer CCD imager for DSC with 3.6x3.6μm² pixels. The image, storage and the readout sections all use four-phase clocks. The storage section contains only about 1/6 of the number of lines of the image section. In snapshot mode, a mechanical shutter shields the image pixels from light during readout (Figure 2.1.1). In preview mode, vertical sub-sampling is performed at the image-storage transition during frame-shift by transporting only the charge of selected lines into the storage section, and by dumping the charge packets of the other lines to the substrate. The resulting continuous video images can be used e.g. for the electronic viewfinder or for auto-focus information, and more recently also for the 'video clip' function of DSC cameras.

Imagers with 4M and 5M pixel resolution are now available. With more than 2000 pixels per line and 20MHz pixel clock, only 30 images/s can be generated when vertically sub-sampled to about 250 lines. A higher capture and display rate of 60 images/s is desirable, especially for video clips. This can be achieved by introducing horizontal sub-sampling.

The 3M pixel CCD shown in Figure 2.1.1 is chosen as test vehicle for developing this feature. Figure 2.1.2 shows a detail of the original design of the transition area from the storage section to the readout register. For the line-per-line horizontal readout, the gates H1 and H2 are set 'on', H3 and H4 are set 'off'. The charge packet is clocked from storage clocks B1 and B2 to B3 and B4. When first B3 and then B4 are switched off, the charge is transferred into the readout register, under gates H1 and H2. Now the horizontal readout can start at the 25MHz standard frequency, while B3 and B4 are 'off' to ensure a good separation between the next charge packet in the storage section and the charge in the readout register.

Figure 2.1.3 shows the redesign for horizontal sub-sampling. Two design modifications are needed to allow horizontal sub-sampling. First, each set of horizontal gates (H1…H4) is split into two new sets (H1…H4 and H1'…H4'). Next, the last row of storage cells is modified: for two columns the cells end, as before, on a B4 gate; for the next two columns, the cells now end on a B3 gate. When no horizontal sub-sampling is required, the operation is as before, except that in two columns the charge is clocked into the register already when B3 is switched off. The split in horizontal clocks in not used, i.e. H1=H1', H2=H2', H3=H3', H4=H4'.

When horizontal sub-sampling with binning is turned on, first the charge from the columns ending on B3 (here columns 3 and 4) is transferred into the horizontal register when B3 is turned low, while in columns 1 and 2 the charge is kept under B4 which is still high, Figure 2.1.3. Then the charge packets originating from columns 3 and 4 are clocked forward over two columns. Finally, the charge from columns 1 and 2 is added when B4 is clocked low, Figure 2.1.4. At this stage, the 2:4 horizontal sub-sampling is achieved.

No color mixing occurs since the periodicity of the R-G-G-B Bayer pattern is respected. The charge is then redistributed, and the horizontal register can be read out, as before with a 4-phase transport clock but now with H2=H3, H4=H1', H2'=H3', H4'=H1. The effective number of stages is halved, so the display rate can be doubled while keeping the standard readout frequency. Only four additional bonding pads are required, no technology change is needed, and the chip size does not increase.

The horizontal sub-sampling at the storage-to-horizontal register transition and the vertical sub-sampling at the image-to-storage (also with binning possibility, [2]) are completely independent, and thus can be combined freely: e.g. to generate high-sensitivity 'movie' images at NTSC standards (60Hz, interlaced) the original 2000(H)x1500(V) image can be reduced to 1000(H)x250(V) by 1:6 vertical sub-sampling combined with 3x vertical and 2x horizontal binning.

To implement horizontal sub-sampling without binning, a drain can be added to the present design. In this case, depending on the exposure conditions, the 2x sensitivity gain achieved by horizontal binning can then be switched 'on' or 'off'.

The design is optimized by 3-D electrostatic simulations to ensure that the last storage gate is both sufficiently long to avoid charge mixing during the initial horizontal transport step, and at the same time not too long to avoid charge transfer problems to the horizontal register when switched off, which could arise due to a reduction of the fringing field.

Performance is evaluated by comparing color images taken with the horizontal sub-sampling with binning 'off' and 'on'. With monochromatic illumination, the color ratios of the overall images does not change, proving that no charge mixing occurs. Using a resolution test chart with white illumination, no vertical or horizontal color shading is observed after color matrixing and white balance, showing that both the vertical and horizontal transfer efficiency are not influenced by the design change. These results are presented in Figure 2.1.5 with the CCD characteristics. Figure 2.1.6 shows an image obtained in preview mode (1:6 vertical sub-sampling) with horizontal sub-sampling 'on'. Figure 2.1.7 shows a die micrograph.

Switchable horizontal sub-sampling is introduced in a CCD by a simple design adaptation. Combined with vertical sub-sampling, on-chip data reduction in both directions is possible. Thus faster auto-focus and auto-exposure, and high-sensitivity video clip mode with up to 60 images/s are now possible in high-resolution DSC cameras without changing the readout frequency of the CCD. The full-resolution performance is not compromised, no technology changes are required, and the chip size is not increased.

References:

[1] J. Bosiers et al., "A 1/3" 1280(H)x960(V) FT-CCD for digital still camera applications", IEDM Tech. Dig., 1997.
[2] H. van Kuijk et al., "Sensitivity improvement in progressive scan FT-CCDs for digital still camera applications", IEDM Tech. Dig., 2000.

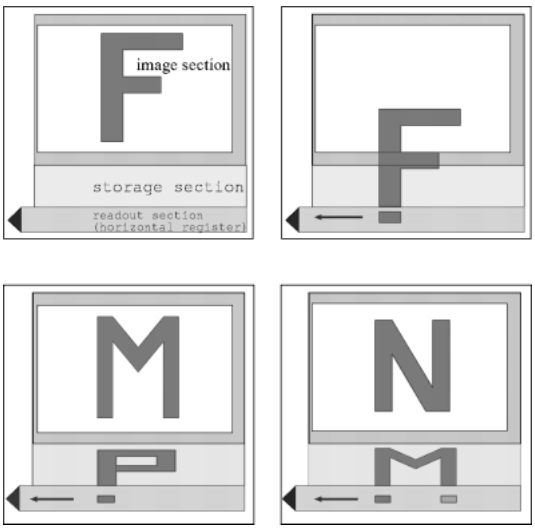

Figure 2.1.1: Top, snapshot/full-resolution readout; bottom, preview mode/vertically sub-sampled readout.

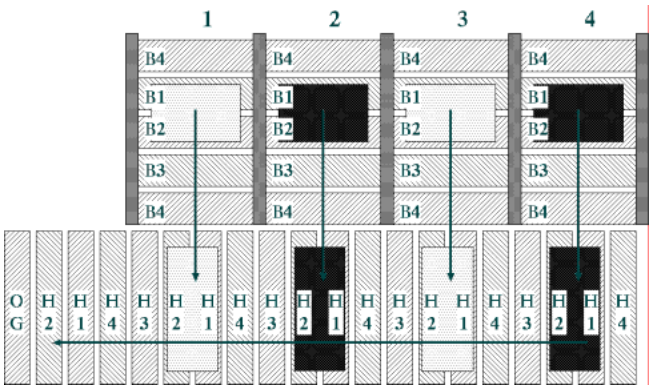

Figure 2.1.2: Original design of transition of storage section to horizontal register without horizontal sub-sampling option.

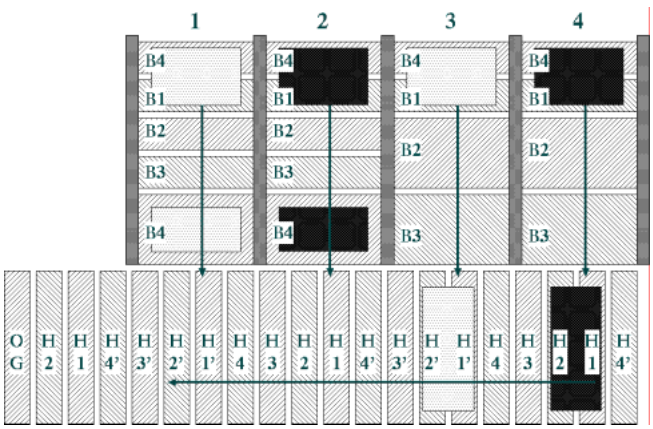

Figure 2.1.3: Redesign with horizontal sub-sampling option.

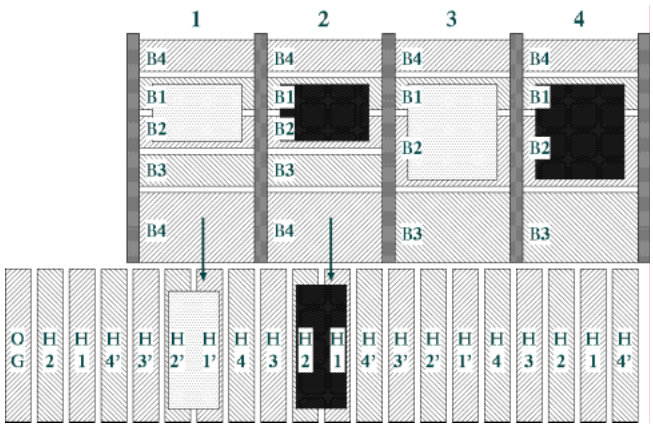

Figure 2.1.4: Horizontal charge binning achieving the 2:4 horizontal sub-sampling.

CCD type	Frame-Transfer with reduced storage	
Optical Format	1/1.8"	
Number of active lines	1500	
Number of active pixels per line	2000	
Pixel size	3.6x 3.6µm^2	
Chip size	68.4mm ^{2}	
Operation modes	Full resolution: = 5im/s at 1500 lines monitor preview: = 40im/s at 250 lines monitor preview with hor. sub-sampling: =80im/s at 250 lines	
V clock frequency & swing H clock frequency & swing Maximum charge capacity Sensitivity (green, IR filter) Color filters	1.56MHz at 12V 25MHz at 3.3V 28 000 electrons 240mV/lux.s Bayer RGB	
Outamp type Outamp responsivity at output node	Triple source-follower 35µV/electron	
Package	24-pin LCC	
	Ratio G/B	Ratio G/R
Full resolution V. sub-samp. (V 1:6) H. & V. sub-samp. (H. 1:2; V. 1:6)	11.7 11.7 11.4	6.4 6.4 6.3

Figure 2.1.5: Summary of 3M pixel 1/1.8" FT-CCD with horizontal sub-sampling option.

Figure 2.1.6: Vertical sub-sampling (1:6) and horizontal sub-sampling with binning (1:2) turned 'on' (1000(H)x250(V) pixels), before re-scaling (top) and after re-scaling to 4:3 aspect ratio (bottom).

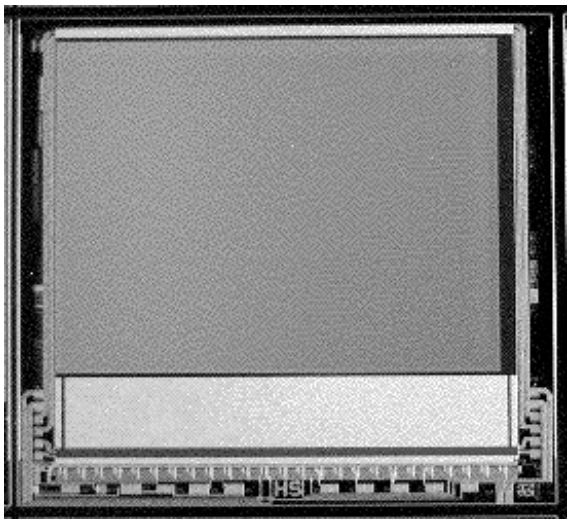

Figure 2.1.7: Die micrograph.