A Color Image Sensor with 9µm Pixels for High-End Digital Still Photography

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Abstract

In this paper a CCD for use in high-end Digital Still Cameras is presented. It has a 9µm x 9µm pixel. Despite the smaller pixel size, the device has a performance which reaches the same level as the *bouwblok* family, with its 12µm x 12µm pixel.

Introduction

In the evolution of the digital still camera market, the goal of manufacturers is to reach the performance of professional cameras in systems that are priced for the consumer market. For the imaging chips, this means that the important characteristics of the sensors, such as sensitivity and dynamic range, should be maintained to the 'professional' values while the pixel size shrinks. We present a new CCD with a 9 µm pixel, made in the process technology of the 12µm *bouwblok* pixel, and whose performance is not compromised by the smaller pixel. Specifically, this new imager offers nearly 13 bits of dynamic range and is made in a low-cost process for large area devices. This process has been optimized for charge handling and sensitivity by tuning the doping profile and adding a new polysilicon etch step to partly thin the CCD gates above the channel. This sensor is a color device, with RGB filters in a Bayer pattern.

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Architecture

Figure 1 shows a floor plan of the sensor. The architecture is similar to the *bouwblok* imagers like the 6 Mpixel (FTF3020) sensor [1]. It uses four vertical(A1-A4) and three horizontal (C1-C3) clocks; the horizontal register is split in two sections to allow the use of either one or two outputs. Like the *bouwblok* sensors, the register contains a separately clocked summing gate (SG) before the output gate (OG). This allows horizontal binning, the summing of packets before read-out, to reduce the sensor's resolution and increase the read-out speed. Unlike the *bouwblok* sensors, a separate transfer gate (TG) has been added for vertical sub-sampling. During sub-sampling a line of charge is dumped to the substrate. Like binning, this increases the frame rate by decreasing the vertical resolution, but now without changing the packet size [2] and consequently without increasing the light sensitivity. The sensor is clock-compatible with the *bouwblok* family and can be used with the same chip set (clock, driver, front-end processing, and DSP chips) for those devices.

Process & process options

These sensors are fabricated in a simple (low-cost) frame transfer CCD process with vertical anti-blooming (Figure 2), using three polysilicon layers and only one metal layer The anti-blooming barrier forms along a shallow out-diffusion of the p-well. The sensor uses standard polysilicon with a thickness of 250 nm, so that the time constant of the vertical clocks is reasonable and no metal strapping is necessary. However, thick polysilicon obstructs the light path to the collection volume, especially for blue light. Unlike the 12µm pixel, the new 9µm can not use light windows. Instead, the new design has thinned areas in the thick polysilicon on top of the pixel. By etching back the thick polysilicon, a membrane of approximately 50nm is left behind [3]. The thick edge of the gates provides a low resistance path for the clock signals and maintains the maximum vertical clock frequency. With three-level clocking, charge packets become so large with the *bouwblok* doping profiles in this smaller pixel that the charge reaches the $Si\text{-}SiO_2$ interface. A 40% higher channel doping moves the charge deeper in the channel, improving charge handling, linearity, and transport [4].

Performance

Figure 3 shows the result of a simulation of the quantum efficiency, done with an in-house optical simulator. The quantum efficiency of the pixel with the thinned polysilicon areas is considerably higher in blue region compared to the pixel without thinned areas. Thinning does improve the relative blue sensitivity at 400 nm with about 100%. The relative sensitivity in green (500nm) is increased by 25%. The measured response of the pixel is excellent. The 3% linear point Q_{lin} lies above 95% of the maximum charge Q_{max} (Figure 4) which exceeds 200 ke-. The adapted doping profile also gives a good transport efficiency by the increasing driving electrical fields during transport. This can be seen in green-green difference, the difference in the response of the green pixels in the blue and red lines under red light. This value is constant over the sensor, showing that transport losses are minimal. The good linearity of the pixel translates into a high value for the linear dynamic range (LDR) as defined by [5]. With a dark current of $30pA/cm^2$ at 30°C and 25 e- read noise over 9MHz, we measure a LDR of 77.5 dB. An overview of the measured characteristics is given in Table 1.

Conclusion

We realised a full frame CCD image sensor with 9µm pixels. The technology is based on a 12µm design with some additions to maintain charge handling. An additional etch step that thins the gates above the channel improves the light sensitivity. A higher phosphorus channel implant gives excellent linearity and transport efficiency. The sensor achieves a linear dynamic range of 77.5 dB.

References

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[2] J.Bosiers et al., "A 1/3" 1280(H) x 960(V) FT-CCD for digital still camera applications", Proc. IEDM'97, Washington DC, 1997

[3] H.Peek et al., "An FT-CCD imager with true 2.4 x 2.4 μm^2 pixels in double membrane poly-Si technology", Proc. IEDM'96, San Francisco, CA, 1996.

[4] H.O. Folkerts et al., "Influence of Sensor Settings an Doping Profile on Dark Current in FT-CCD's", 1999 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, June 1999, Nagano, Japan. pp. 9-12.

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Q_{lin} (1%)	200 k e-
Dark Current (at 30°C)	30 pA/cm^2
Read Noise	24 e-
Linear Dynamic Range	77.5 dB
Relative Sensitivity (3200 K, to green) blue/green/red	0.73/1.0/1.07

Table 1: Measured characteristics of the 9µm pixel

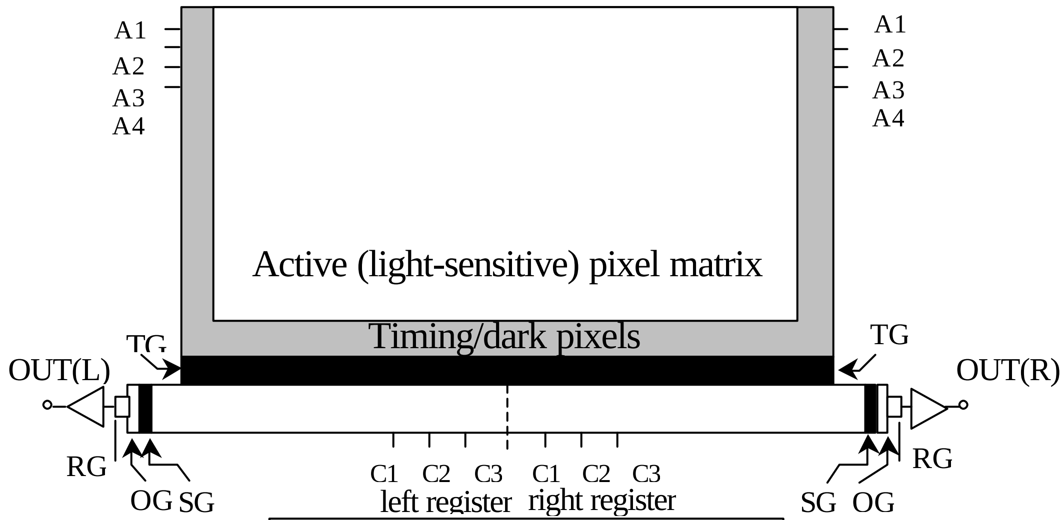

Figure 1: The Sensor Architecture

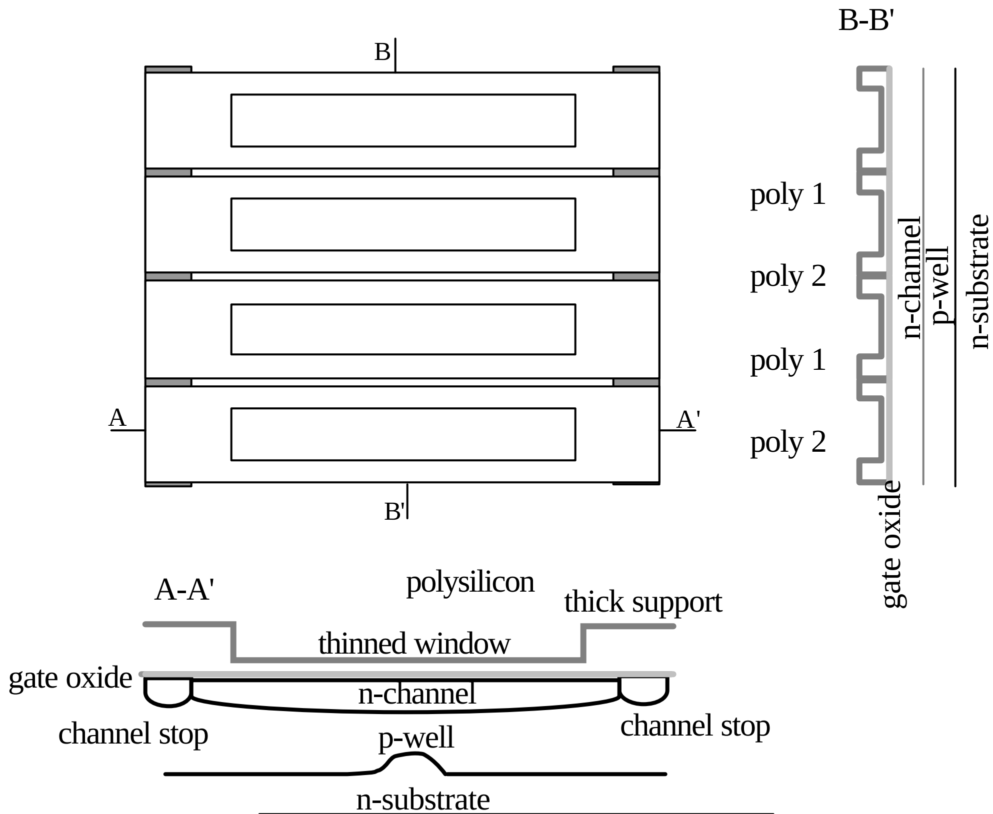

Figure 2: The Pixel Structure

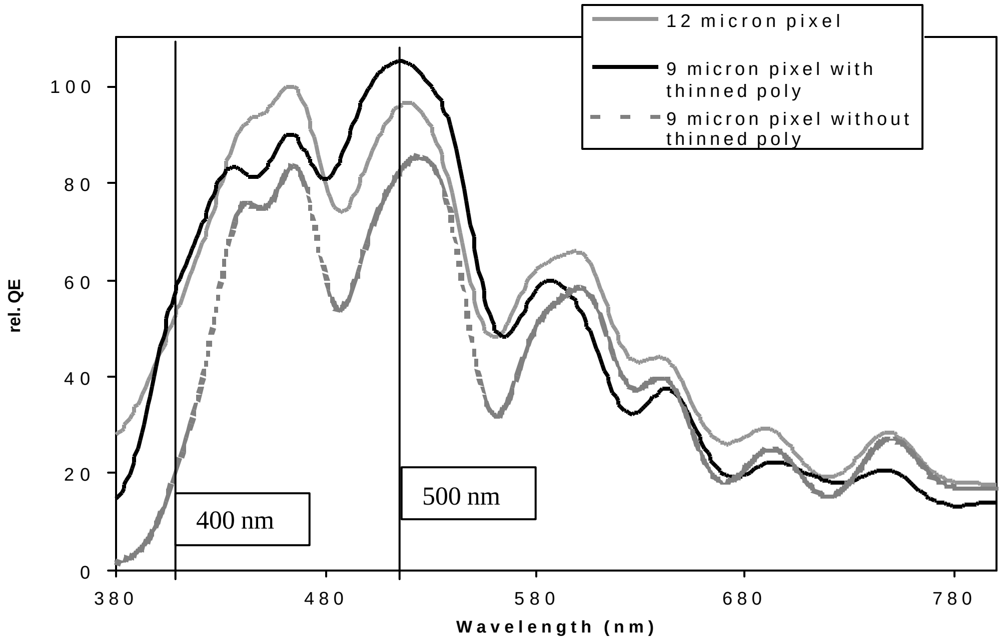

Figure 3: The Simulated Quantum Efficiency of the 9 µm pixel with and without thinned polysilicon, relative to the 12 µm pixel

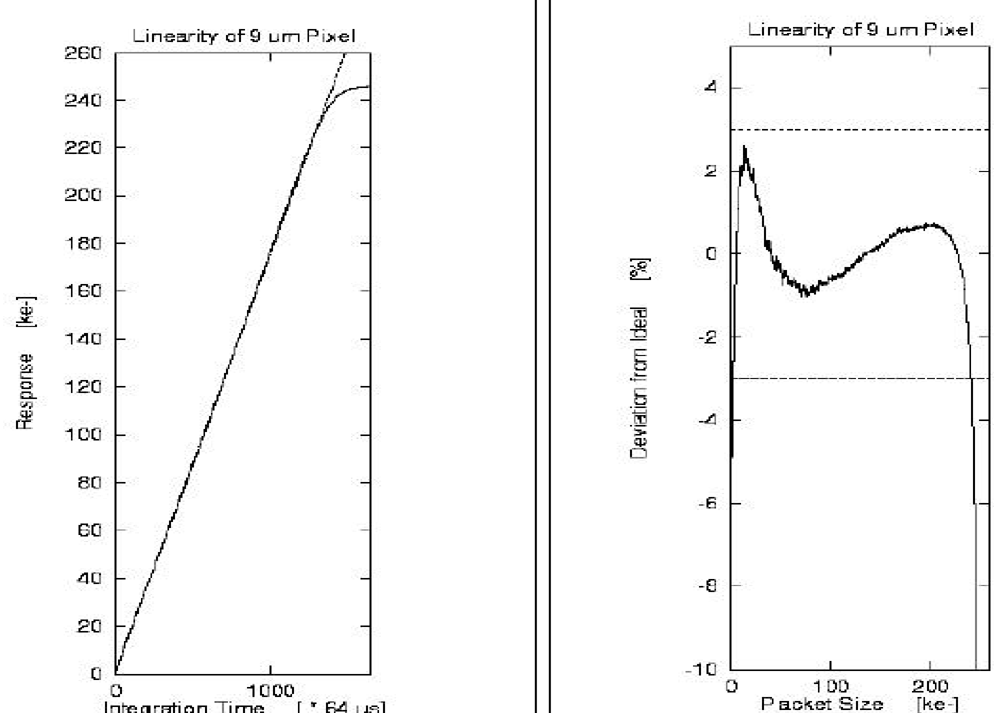

Figure 4: Linearity in response (left) and plotted as deviation from ideal (right).