CCD or CMOS Image Sensors for Consumer Digital still Photography ?

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Abstract

Compared to CCD imagers, CMOS image sensors have some clear advantages : lower power, lower driving voltages, on-chip functionality, selective read-out and cost. Despite of these advantages, CCDs still deliver a better image quality, especially for digital still applications. This paper tries to give an answer to the questions : "Why is the imaging performance of a CCD better ? Will it remain that way ? Can CMOS imagers also challenge CCDs in this application field ?"

Introduction

There are two interesting new developments in the imaging field :

- the classical solid-state imager sensor technology, charge-coupled devices (CCDs), is being challenged by CMOS image sensors, and
- the digital imaging market is emerging, mainly in the direction of digital still applications.

A simple conclusion from these two statements might be : every digital still camera has a CMOS image sensor. In fact, the cameras for the consumer digital still applications which are currently on the market, contain almost exclusively CCD image sensors as the imaging device. This paper attempts to explain this contradiction.

Charge-Coupled Devices

This section briefly describes the working principle of the CCDs. There are many architectures possible as far as CCDs are concerned, but in this paper, we will limit the description to the so-called 'full-frame CCDs'.

A CCD is composed of a series connection of capacitors. All of the capacitors have one plate in common : the silicon substrate. The second plate of each capacitor is biased by means of digital pulses. Figure 1 shows a cross section of a single pixel of a CCD : the cell contains 4 capacitors, all of which are biased at 0 V, except the second one, which is biased at 10 V (top of Figure 1). An isolated potential well is generated in the silicon substrate by applying a large potential to the gate of this capacitor. The potential well can hold a charge packet composed of electrons, and can be thought of as a bucket holding water.

If the bias voltage of the third gate is switched to 10 V, the potential well in the silicon is enlarged and the electrons are distributed along the entire length of the well (center of Figure 1). The opposite takes place when the gate bias of the second gate is switched back to 0V : the potential well shrinks (see bottom of Figure 1). When the action is completed, the potential well with the isolated charge packet is shifted from the second towards the third gate. This process is typical for a charge-coupled device : charge packets can be transported from one site to another.

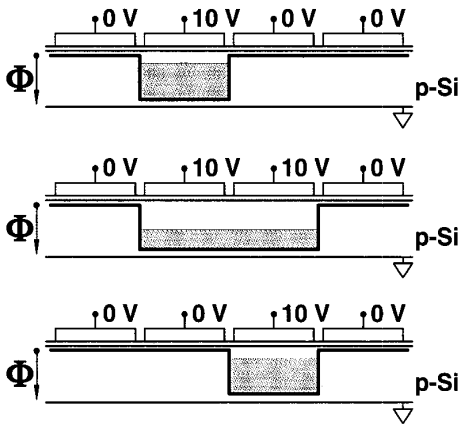

Figure 1. Basic charge transport by means of four phases through a CCD. The potential wells in the silicon substrate are indicated by the solid lines.

A two-dimensional CCD imaging array can be built using a serial connection of the aforementioned CCD cells. This is shown in Figure 2. Six (vertical) columns, each of 6 pixels, compose the focal plane. The columns are all connected to a serial horizontal output register and an output amplifier. The complete operation of a full-frame device can be described as follows : All CCD cells in the light-sensitive top part of the device or image section are biased in the integrating mode. Part of the CCD gates are connected to a high DC level, and part of them to a low DC level, creating individual potential wells in the silicon substrate.

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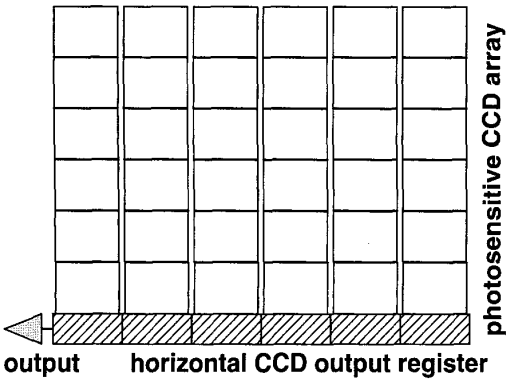

Figure 2. Device architecture of a full-frame CCD image sensor.

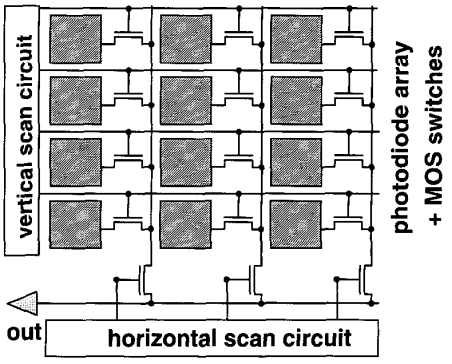

Figure 3. Basic device architecture of a CMOS passive pixel image sensor.

The generation of the potential 'buckets' is similar to the process described in Figure 1. In this situation, charges generated by impinging photons are collected in the induced potential wells. At the end of a defined integration time, the CCD shift registers transfer their charge packets to the corresponding CCD line in the light-insensitive horizontal output register. During this action, the charge packets located on a horizontal line (and therefore belonging to different vertical CCD shift registers) are transferred to a single output structure. Once the charge packets have been shifted into the horizontal output register, the final transfer to the output stage can take place, charge packets can be converted to an electrical voltage, and the video signal can be processed further. During the transfer of the video information from the light-sensitive area to the memory area, photons can still continuously impinge on the sensor. A shutter is used to avoid this effect.

It is important to notice that :

- the CCDs transport their charge packets towards the outside world through a single output stage,
- in the case of a high pixel count and a high frame rate, the output stage operates at high frequencies,
- the integration of charges starts and ends at the same point in time for all pixels,
- CCDs are fabricated in a dedicated process, fully optimized for imaging.

CMOS Image Sensors

A CMOS XY-addressable imager is constructed as a matrix of photodiodes, each of which is provided with a MOS transistor acting as a switch. This setup is shown schematically in Figure 3.

To convert the two-dimensional spatial information into the serial stream of electrical signals, electronic scan circuits are added to the device to address all pixels in a sequential mode, and to readout their information. This addressing feature forms the basic operation of the device.

At the beginning of a new field, the vertical scan circuit is activated. Suppose that the first row of pixels is selected. This is done by setting a high DC voltage on all gates of the MOS switches of this first row. Next, the horizontal scan circuit selects the pixels on one particular column by scanning its own outputs using a single high DC output, while all others are at a low level. This combination of one output of the vertical scanner and one output of the horizontal scanner at a high level and all the others low, selects one single pixel from the two-dimensional matrix. This pixel can be emptied and can dump its information into the output stage. Immediately after this action, the pixel can be reset and restart an integration. The neighboring pixel will then be addressed and readout.

The CMOS imager with passive pixels (the simple photodiode) is limited in its performance due to the relatively high levels of noise and fixed-pattern noise. These are partly caused by the small capacitance of the photodiode which is connected to the large readout capacitance of the sense line. A small amplifier can be added to every pixel to overcome this noise and fixed-pattern noise. A source-follower stage (amplification in the charge domain) is constructed within every single pixel, and both the noise and the fixed-pattern noise can be limited.

The new architecture of the Active Pixel Sensor (APS) is very similar to the Passive Pixel Sensor (PPS), except for the pixel design. Figure 4 shows two potential pixel concepts : the left one is based on a photogate conversion and the right one is based on a photodiode conversion.

After selection of the appropriate pixel by the scan circuitry, the information in the photogate pixel is read in exactly the same way as it is done in a CCD : the charge is transported from the photosensitive area towards a floating diffusion amplifier by means of the transfer gate. The driver of the source follower stage (the amplifier in the pixel) is implemented in the pixel itself; the load of the source follower is common for all pixels on a column. The photodiode pixel looks very similar to the photogate pixel,

except for the additional transport from the converting site towards the output diffusion.

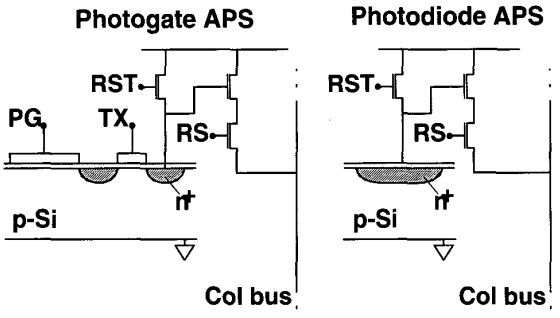

Figure 4. Pixel configuration, used in active pixel CMOS imagers, based on a photogate and a photodiode.

When compared to the PPS, the overall noise and fixed-pattern noise performance of the APS sensors is at least one order of magnitude better.

It is important to notice that :

- the CMOS imagers transport their information towards the outside world through many different output stages,
- in the case of a high pixel count and a high frame rate, the output stage present in each pixel operates at low frequencies,
- the integration of charges starts and ends at a different point in time for all pixels,
- CMOS imagers are fabricated in more or less standard processes, which are not optimized for imaging.

Imager Parameters versus Camera Specification

The quality of the picture made by the digital photographic equipment is largely determined by the various parameters and characteristics of the image sensor. The resolution is probably the most common imager characteristic. It is clear that more pixels on the focal plane will result in a higher degree of sharpness in the digital print. Other important imager characteristics are listed in Table 1, together with their corresponding translation into camera specifications.

Although the relationship between the imager parameter, on the one hand, and the corresponding camera specification, on the other hand, might be clear and straight forward, it is not always easy to improve a particular characteristic. Consider the resolution, for example : adding more pixels on a chip will increase the area of the device, the price of the chip, the size of the lens and the volume of the camera. We have to consider the pros and cons of each of these side-effects when deciding whether or not to increase the resolution of the chip. A second important boundary condition, as far as chip size is concerned, is the optical format. The imager is part of an optical system for which standards exist which cannot be circumvented.

Imager Parameter	Camera Specification
Resolution	Sharpness
Signal-to-noise ratio	ISO speed
Angular response	Minimum F-stop
Dark current	Maximum exposure time
Dynamic range	Latitude
Linearity	Color fidelity
Pixel uniformity	Granularity
Imager architecture	Features

Table 1. Translation of imager parameters into camera specifications.

During the oral presentation of the paper, we will discuss the various parameters and their impact on camera specifications. Existing CCD and CMOS imagers will be benchmarked for each characteristic. The most important characteristic in this paper, the noise of the imager, will be described in more detail.

Signal-to-Noise Ratio and Dynamic Range

The imager's noise performance plays a crucial role in the quality of the digital print. This is in contradiction to classical video. The reason for this difference can be explained using Figure 5.

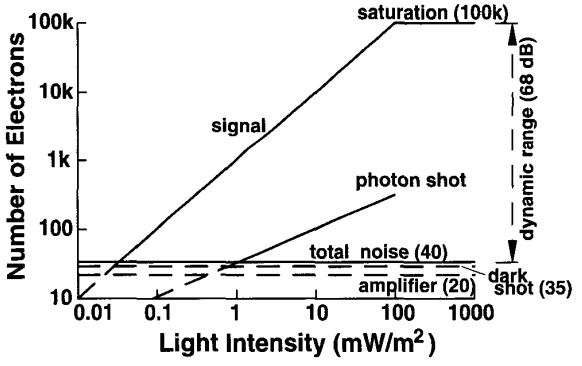

Figure 5. Various sensor signals as a function of the amount of light input.

This illustration shows the output of a sensor (in number of electrons) as a function of the light input. The video signal of the sensor is fully linear with respect to the sensor's input, up to saturation level. One of the different noise sources also varies as a function of the light input : the photon shot noise. As the number of impinging photons obeys the Poisson statistics, the photon shot noise is proportional to the square root of the number of photon-generated electrons. The other noise sources are independent of the light input : the temporal noise of the output amplifier (read noise) and the dark shot

noise (stochastical noise of the dark current). Two noise sources are not shown on this graph :

- the reset noise, due to the reset action of the floating diffusion,
- the fixed-pattern noise, which is not a temporal noise, but which is the difference in response for all the pixels.

For any given light input, the signal-to-noise ratio to be delivered by the imager can be calculated as the "distance" between the signal and the highest noise level. For input levels lower than 0.1 □W/cm^2, the S/N ratio is determined by the total noise of the sensor; for input levels higher than 0.1 □W/cm^2, the noise is determined by the photon shot noise. The difference when compared to standard video applications, is that both the TV-monitor and the human eye filter out part of the noise, including the photon shot noise. In other words, digital still applications do not have these filters, and suffer more from signal-to-noise problems than does a standard video.

For the sake of completeness, the definition of dynamic range is also shown in Figure 5. Note that the dark current shot noise is also included in the noise figure.

Benchmarking CCD and CMOS imagers for their noise performance yields the following conclusions :

- photon shot noise : this noise component is given and determined by mother nature. Both CCD and CMOS suffer equally from this phenomenon.
- dark current shot noise : dark current shot noise finds its origin in the uncertainty of the amount of dark current generated in the sensor. A uniformly generated dark current can be compensated for, and even a non-uniformly generated dark current can be corrected, but there is no compensation means for the dark current shot noise. In other words, the dark current should be kept as low as possible. These days, CCDs still outperform CMOS imagers by at least a factor of 10 as far as dark current is concerned.
- read noise : the temporal noise of the output amplifier is a strong function of the bandwidth of the output amplifier. CMOS imagers are much more favored than the CCD when considering this characteristic : a CCD outputs all the information through a single output stage, whereas a CMOS has as many output stages as the sensor has pixels. The bandwidth of a CMOS output stage is consequently much lower than that of a CCD.
- reset noise : if this component is not completely suppressed, it dominates the overall noise performance. If the output node of the sensor has a separate floating diffusion (as is the case for all CCDs and for the photogate APS imagers), the reset noise can be completely cancelled using off-chip or on-chip Correlated Double-Sampling (CDS) circuitry. The absence of the rest-noise cancellation option in photodiode APS sensors, forces the designers of this pixel type to look for alternatives which can also have CDS on-chip.
- Fixed-Pattern Noise : FPN is the result of offset and gain variations between the various output amplifiers on the same chip. Fortunately, a CCD only has one amplifier, therefore keeping the FPN very low. Unfortunately, an active pixel CMOS imager has as many output stages as it has pixels. A CMOS sensor therefore suffers much more from FPN. These days, researchers pay a lot of attention to on-chip FPN compensation circuits, to minimize the visible effect of the FPN.

Conclusions

The nature of the DSC application requires an image sensor with an excellent noise performance, much better than for video applications. CCDs are still superior to CMOS image sensors, as far as signal-to-noise and dynamic range are concerned. This characteristic means that CCDs are still the first choice for high quality digital still photography. A great deal of effort is still put into further optimization of the noise performance of CMOS imagers, however. Examples of these efforts are the development of new pixel designs (a photodiode-based pixel with the possibility of reset-noise cancellation), and further fine tuning of the semiconductor processes to produce devices with a lower dark current.

If the noise issues (mainly reset noise and dark current shot noise) can be solved in CMOS imagers, then CMOS might be able to challenge CCDs in digital still applications. Only then can we benefit from the many advantages of the CMOS image sensor compared to the CCD:

- low power of CMOS,
- low driving voltages of CMOS,
- on-chip functionality,
- selective read-out mechanism,
- cost advantages.

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