Building a Better Mousetrap

Modified CMOS processes improve image sensor performance.

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When charge-coupled device (CCD) detectors entered the consumer camcorder market two decades ago, they faced a challenge from metal-oxide semiconductor (MOS) image sensors, which were based on the same principle as today's complementary-metal-oxide-semiconductor (CMOS) imagers. Excessive image nonuniformity, or fixed-pattern noise (FPN), blocked MOS detectors from commercial success, however.

By leveraging improved architecture and fabrication technology, CMOS image sensors have returned to challenge CCD detectors. Enhanced technology has provided new options to the designer, and today's low-end CMOS products can compete with the more traditional technology.

design and operation

CMOS imagers transport their information toward the outside world through many different output stages, more or less in parallel. A CMOS *xy*-addressable imager consists of a matrix of photodiodes, each of which is provided with a MOS transistor that acts as a switch.

Passive-pixel CMOS imagers—simple photodiodes with addressing transistors in every pixel—suffer from high levels of noise and FPN. By integrating amplifier circuitry with each pixel to create an active pixel sensor (APS), designers can boost the signal-to-noise ratio (SNR) of the device, achieving FPN and overall noise performance that is an order of magnitude better than passive designs. The pixel itself only includes the driver transistor; the load of the source-follower is common for all pixels belonging to the same column.

To convert two-dimensional spatial information into the serial stream of electrical signals, electronic scan circuits read out each pixel sequentially. At the beginning of a new field, the vertical scan circuit selects a row of pixels by setting a high DC voltage on all gates of the MOS switches of the row. Next, the horizontal scan circuit selects the pixels in one particular column using the same technique. As a result, only one pixel in the two-dimensional matrix has a high DC voltage on both the row and the column switch, which electronically selects it for readout. After the pixel dumps its information into the output stage, it is reset to begin a new integration, and the readout process progresses to the next pixel in the row.

The most common pixel architectures for APSs are photogate conversion and photodiode conversion (see figure 2). In the photogate design, once the scan circuitry has selected a pixel, a pulse on the transfer gate triggers the transport of data from the photosensitive area toward a floating-diffusion amplifier. The photodiode pixel looks very similar to the photogate pixel, except for the additional transport of data from the converting site toward the output diffusion.

enhancing performance

Manufacturers initially fabricated CMOS image sensors using DRAM processes, which are characterized by 0.6-μm minimum feature sizes, a single level of polysilicon, and triple layers of metal. Though economical, DRAM processes yield devices with sensitivity and noise problems.

The first step in overcoming these performance drawbacks is to switch from a DRAM process to an analog CMOS process. Although it is more complex, the approach offers enhanced fabrication capabilities for capacitors, accurate resistors, and well-matched transistors, yielding devices with improved FPN and imaging performance. The resultant image sensors are still not up to the level of CCD detectors, however.

To improve the imaging quality of a device, manufacturers must alter an existing CMOS process to optimize the spectral response and/or noise performance. SeeMOS (Philips Semiconductors Image Sensors; Eindhoven, Netherlands), for example, is an optimized 0.35-μm CMOS process designed to manufacture high-quality CMOS image sensors.

Improving sensitivity

In theory, a photodiode-based APS pixel can show great light sensitivity, but devices fabricated via standard CMOS processes are hampered by shallow photodiode junctions and limited fill factors. Process adjustments can compensate for these drawbacks, however.

Standard CMOS processes yield photodiode junctions that are only about 0.25 μm deep, providing sensitivity to blue and green light, but almost no response to red wavelengths. Red photons penetrate up to 3 μm into the silicon before absorption and are lost if the depletion layer around the metallurgical junction does

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not reach these depths. Designers can compensate for this effect by introducing extra boron or phosphorus implantations into the standard CMOS process, providing a deeper depletion layer to capture the generated electrons.

Low fill factor (the ratio of active region to total pixel area) also reduces device sensitivity. Each pixel in the detector array incorporates at least three transistors, which occupy the same area as the photosensitive active region. Because the transistors are not light sensitive, their presence drops the per-pixel fill factor to as low as 25%.

Microlenses can counteract this effect by focusing the photons that would normally impinge on the transistors onto the active area, improving sensitivity by a factor of 2.5. Unfortunately, microlensed image sensors show a strong dependency of sensitivity as a function of the incident angle of the incoming rays. This effect can limit the benefits of the microlenses to larger *f*-numbers.

reducing noise

The noise in the video signal delivered by a CMOS image sensor consists of photon shot noise, dark-current shot noise, reset noise, and thermal noise. Photon shot noise is the uncertainty of the amount of photons falling on a pixel. In video applications, the human eye filters out this noise component, but in digital still images, the presence of photon shot noise can seriously hamper sensor performance.

Dark-current shot noise is the noise component generated by pixels in the absence of illumination. Dark current itself can be canceled out and dark-current nonuniformities can be corrected by means of an additional frame store, which is extra memory that can contain a complete frame or picture. Most of today's CMOS imagers focus on low-end applications, however, so an additional frame store is not always affordable.

Although dark-current shot noise is impossible to eliminate, designers can reduce the effect of the shot noise, as well as that of FPN, by minimizing overall dark-current generation. One technique involves the use of pinned photodiodes, in which a shallow p^+ layer on top of the photodiode fills the interface states by means of holes, preventing them from generating dark current.

Another noise source, pixel-reset noise, can be the limiting factor on the SNR of the imager. After every reset action, the capacitance of the floating diffusion is recharged through the reset resistor, which generates noise. Reset noise can be canceled out by means of correlated-double sampling (CDS), in which reset noise is measured alone, then subtracted from the measurement of video signal plus the reset noise.

CDS also cancels the major part of the 1/*f* noise. To perform CDS, the device must include an electron collection site and a separate measuring site on each pixel. Pixels with a single photodiode architecture are not compatible with CDS, but photogate architecture is well-suited to the technique. As always, there are tradeoffs. Although the photogate design is compatible with CDS, it requires an extra transistor within every pixel, further reducing fill factor.

The final noise source is the thermal noise generated by the electronic circuitry present in every pixel. The CMOS pixel readout sequence minimizes thermal noise. The readout speed of every pixel is relatively low (one read cycle for every frame), so the bandwidth of the amplifier within every pixel is very small.

optimizing architecture

CMOS imager performance depends on the architecture of the individual pixel as well as that of the overall image sensor. Unlike CCD detectors, basic CMOS imagers use a rolling integration cycle in which the beginning and end of the integration period differs for each pixel. This approach can yield poor results when integration times are short, or when the device is operated with flash lamp, strobe, or fluorescent light.

To achieve simultaneous pixel integration—freeze-frame shutter—the device requires in-pixel storage capability, which can be realized at the cost of an extra transistor and extra capacitor within every pixel. In some cases this architecture can provide both extra storage and CDS capability, though not simultaneously. Such devices operate in one of two modes: synchronous integration or CDS.

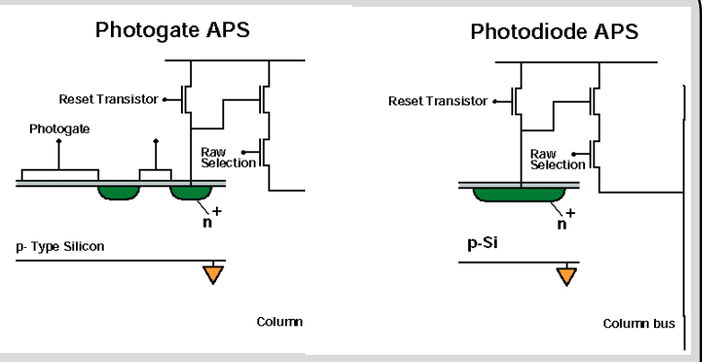

Figure 2 Photogate design (left) provides low noise operation for low-light imaging. Photodiode architecture (right), an economical design for consumer applications, offers additional transport toward output diffusion.

CMOS designers have the option of performing on-chip analog-to-digital (A/D) conversion. Conversion can be implemented with a single A/D converter (ADC), but the converter must operate at the speed dictated by the application. A VGA imager (640 × 480) operating at 60 frames/s, for example, forces a 20 MHz conversion rate. To implement a low-power ADC with these characteristics on-chip is a challenge.

The speed issue can be overcome by introducing an ADC on every column, which, in this example, would lower the operating rate required of each circuit by a factor of 640. The main drawback of the per-column approach is the reduction in fill factor. For a VGA image sensor with 5-µm pixels that is fabricated with a 0.5-µm process, the ADC would occupy 50% of the area of the focal plane. This ultimately is a very high price for this type of architecture. Not surprisingly, most commercial products still use a single-ADC solution.

looking to the future

CMOS imagers benefit from improvements to semiconduc-

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tor fabrication technology. Although the external optics for the imager determine the focal plane area, both the on-chip electronics and the in-pixel circuitry can become much smaller as manufacturers develop more aggressive technologies.

Unfortunately, although the new technologies shrink circuitry dimensions, they also severely limit the imaging function in the following ways: Metallurgical junctions become shallower, which degrades light sensitivity and increases dark current; salicidation of the junctions minimizes resistivity but renders the junctions opaque to incoming photons; increasing numbers of metallic layers raise the physical height of the overall stack, hampering the light sensitivity, even in the case of microlenses; and shrinking power supplies limit the dynamic range of the imagers.

Clearly it will be a challenge to fabricate high-performance CMOS image sensors using standard processes designed for critical dimensions smaller than 0.18 μm. To overcome the issues mentioned above, new processes will be needed to bring CMOS image sensors up to the performance level of CCD imagers. **oe**

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