Versatile building-block architecture for large area, high performance CCD imagers

Albert Theuwissen, Monique Beenhakkers, Bart Dillen, Hein Otto Folkerts, Henk Heyns, Laurens Korthout, Greg Kreider, Peter Opmeer, Herman Peek, Edwin Roks, Helmut Rosner, Arjen van der Sijde, Frans Vledder.

Philips Imaging Technology[1]
Prof. Holstlaan, 4,
MS WAG14,
5656AA Eindhoven,
the Netherlands.

Abstract

A *bouwblok* (building-block) concept is described which allows one to fabricate several large area CCD image sensors from a single mask set. The size of the various imagers can differ both horizontally as well as vertically. The new method drastically reducesthe development time and the associated cost of a new sensor. Because all imagers use of same basic pixel structure, the characteristics of new configurations can be fairly well predicted.

Keywords : CCD, imagers, solid-state imaging, modular concept, mask stitching, high-performance imaging, digital photography.

1. Introduction

Professional imaging applications all require an image sensor which is optimally suited for the function which needs to be performed. Or vice versa : for every high-end imager, only a limited number of application fields can be addressed. This makes the development of large area, high performance devices unique for each type and, consequently relatively time consuming and expensive. For instance, medical applications require an image sensor with 1 Mpixels and 30 frames/sec, while the ultra-large area devices applied in astronomy have to deliver only one frame a night, but need to have ultra-high pixel numbers. It would be much more economical if a common solution could be found for all these professional applications. A first step could be a common flow chart to manufacture all these devices, a second step towards more commonality could be found in a common test strategy, but the ultimate solution would be a common mask set developed in a single development stage for all devices and applications.

The latter approach is described in this paper. Based on the knowledge gained in the HDTV project a stitching technique is applied to put several pieces together like a jigsaw during the diffusion cycle of the silicon wafers. In this way almost any size of image sensor can be defined. The basic architecture of the CCD imager is described in Section 2, Section 3 contains more details about the building-block architecture and Section 4 will show several examples manufactured thus far with this technique. The main characteristics of the CCD image sensors are summarized in Section 5. The paper will end with conclusions.

2. Basic architecture of CCD imagers

A CCD image sensor in general is built-up by means of several unit cells or blocks which are connected to each other during the design or lay-out phase of the development cycle of the sensor. A typical example of

[1] email : theuwiss@natlab.research.philips.com ; telephone : +31-40-274-2734 ; fax +31-40-274-3390 ; web : http://www.be.philips.com/ppi

such a unit cell or block is the matrix of pixels. The lay-out designer creates a single pixel and this structure is repeated in the x- and y-directions to complete the overall matrix of light-sensitive pixels. Another example is the output amplifier, which in turn is constructed by means of three source-follower stages. These can be seen again as a unit cell built-up by means of single transistors.

A schematic view of such a (simplified) architecture is shown in Figure 1. It shows the basic configuration of a full-frame image sensor. The central part forms the matrix of CCD pixels which convert the incoming photons into electrons. A typical example (for this study) can by a matrix of 1 K pixels both horizontally and vertically. The various CCD gates which define and drive the individual pixels need to be connected in 4 groups (in the case of a four-phase transporting system). The interconnection function is done by means of aluminum bus-bars. These bus-bars are interconnected to the bondpads which form the interface to the outside world. The interconnections from the gates to the bonding pads are indicated in Figure 1 by the shaded areas. Note that these interconnecting patterns are not the same left and right.

The electrons packets generated and collected in the pixels need to be transported to the outside world. This is done primarily by the matrix of CCD pixels itself, but also by means of horizontal output registers. These are located at the top and at the bottom of the matrix. The charge packets move from the parallel channels in the matrix to the serial read-out structure in the horizontal CCD registers. In other words, a parallel-serial transport takes place.

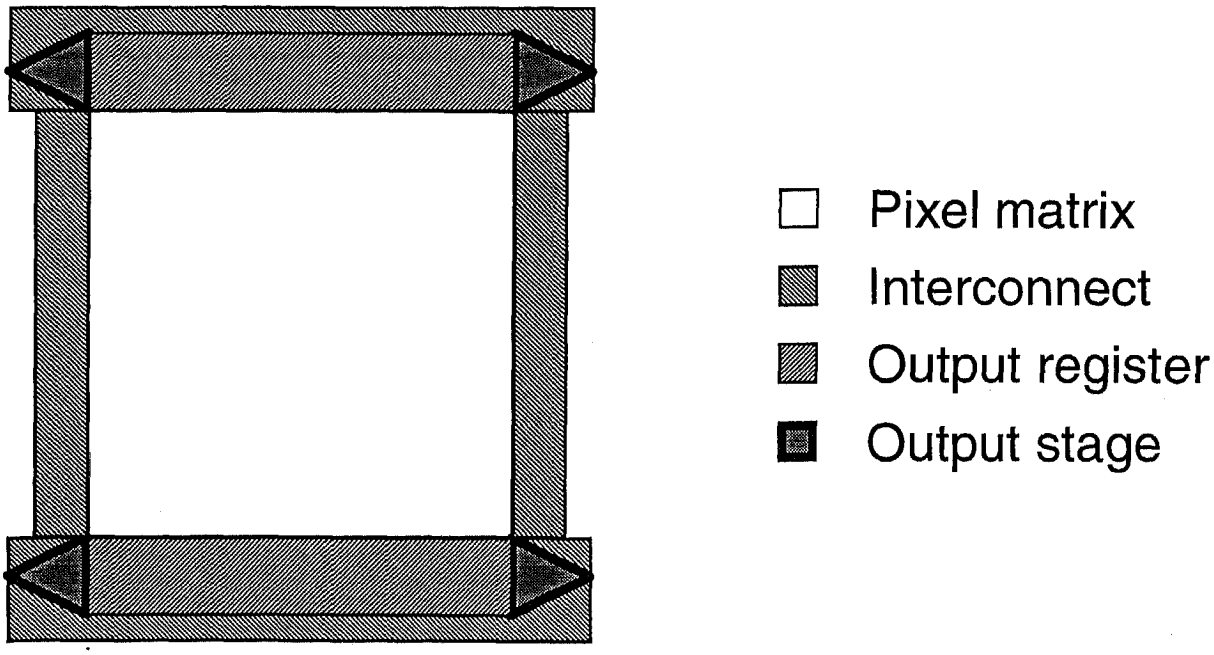


Figure 1. *Example of the device architecture applicable to a full-frame CCD image sensor, with a matrix of pixels, all metal interconnects, two horizontal read-out registers and four output amplifiers.*

The gates of these horizontal CCD registers need to be connected again in three or four groups, depending on the read-out mechanism. These interconnections, together with their bonding pads are also indicated in Figure 1. After the horizontal transport the charge packets arrive at the output node where they are converted into a measurable voltage by means of the output amplifier. Note that in the example used, four output amplifiers are used, one at each corner of the chip. By means of appropriate clocking schemes, these four output stages can be used in parallel or just one of these four can be chosen.

After the design and lay-out phase in the development stage of the image sensor, the lay-out is shipped to the mask shop and masks are fabricated which are used by the diffusion department to manufacture the image sensors.

3. Building-block architecture

As could be understood from the foregoing section, the lay-out engineer usually designs the various parts of the imager separately and puts them together on the CAD system. Another approach can be found in the following strategy : the individual blocks are not assembled on the CAD system, but are shipped to the mask shop as separate circuits. The assembling of the various parts of the integrated circuits are put together in a much later stage, namely during the diffusion process.

A possible splitting in different building blocks of the imager depicted in Figure 1 can be seen in Figure 2. Exactly the same parts as in the earlier figure can be recognized : the central matrix of individual pixels, the left and right interconnections to these gates, the two horizontal read-out registers (with their metal interconnection not separated), and the four different output amplifiers.

The design, the lay-out and the masks are fabricated in such a way that the various parts fit perfectly to each other during the production phase. To realize this, special structures are including at the lines between the various pieces of the puzzle.

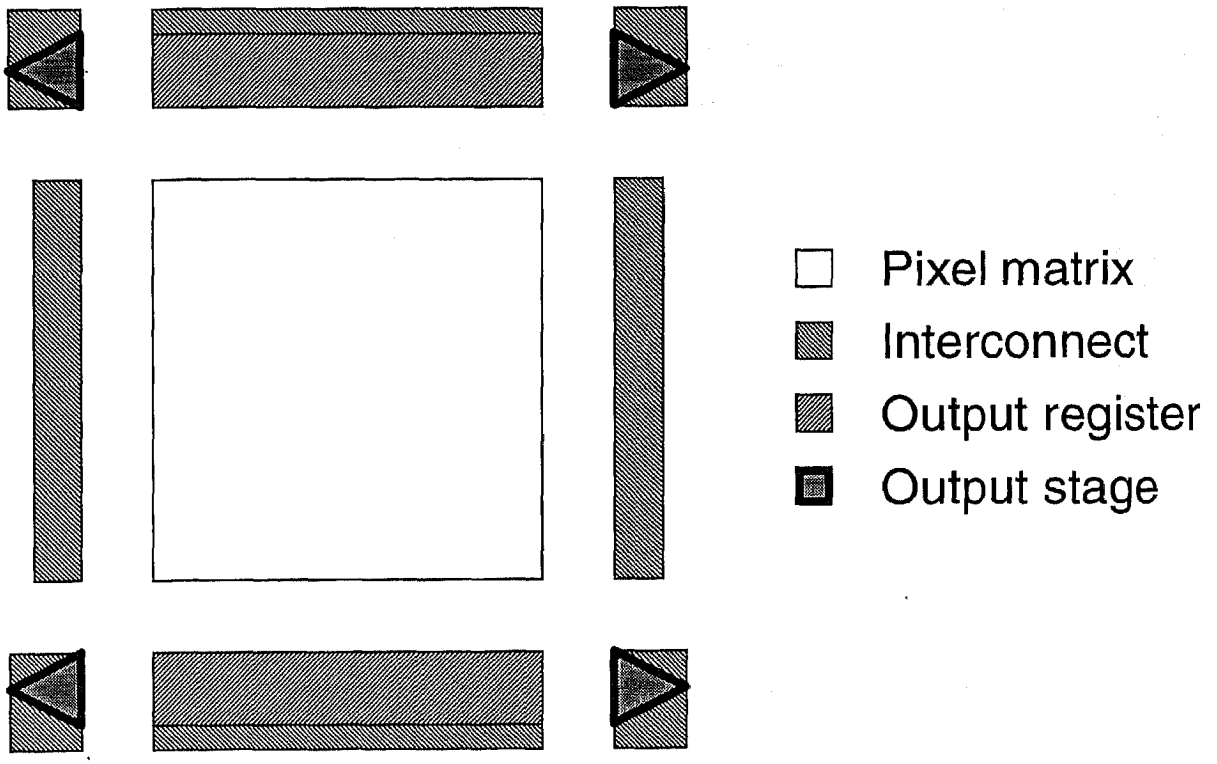


Figure 2. *Separation of the various building blocks which are used in the overall design of the image sensor depicted in Figure 1.*

This stitching technique is not entirely new. It is already described earlier in literature for stitching in one dimension [1], [2] and for stitching of pieces belonging to the circuitry of liquid-crystal displays in two dimensions [3].

But an interesting feature shows up if the mask set is designed such that the various parts can seem nicely together : instead of placing the right interconnect block directly alongside the pixel matrix, it should alsobe possible to place a second copy of the pixel matrix near the first one. In this way the original 1 K x 1K pixel array is extended towards 2 K x 1 K. Figure 3 illustrates this effect. Not only the pixel array is repeated, but the horizontal output registers with their interconnections and bonding pads are too. In other words : the jigsaw puzzle is not only put back together, some of the parts are multiplied and fed in between the original ones.

The same trick which is applied to come to Figure 3, namely, expansion in the horizontal direction, can also be used in the vertical direction to make the imagers also "taller". The combination of both results in an expandable system or imager architecture in two dimensions. Actually the only limitation for this building-block concept is the wafer size. All devices which are multiples of the central matrix of 1 K x 1K pixels can be made by means of this technique.

But if the stitching takes place in the active image area, one has to be extremely careful with the design of the stitching lines. To avoid visible effects in the images captured with these imagers, special stitching structures are placed on both sides of the structures which need to be stitched. As will be shown later, the stitching lines do not introduce any effect that limits the application of these devices.

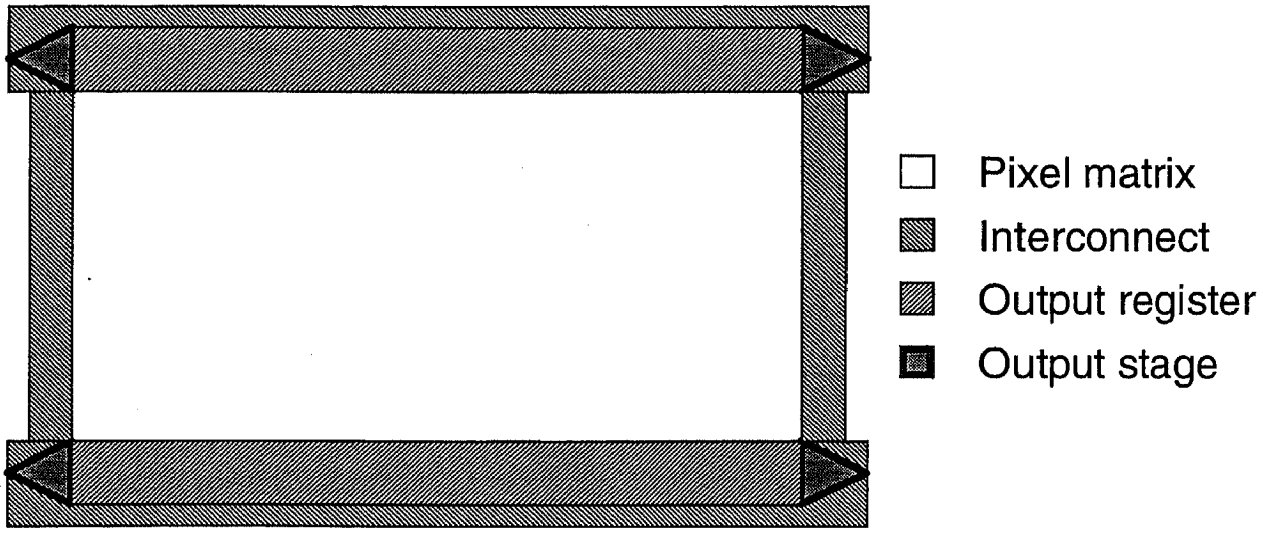


Figure 3. *Stitching the units cells back together while at the same time repeating the central parts twice enlarges the array to twice the pixel count of the original one, shown in Figure 1.*

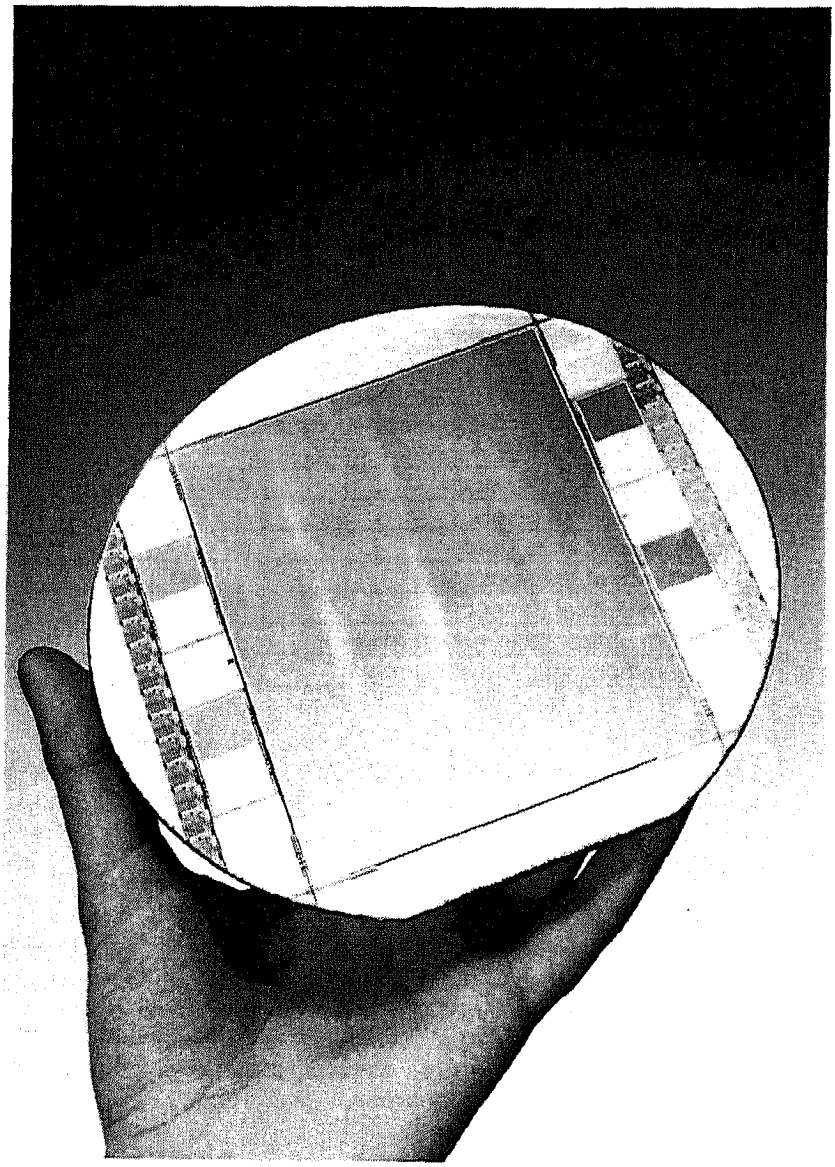
As already mentioned, in principle all devices which are multiples of the 1 K x 1 K unit block are possible with this technique. The smallest is the 1 K x 1 K itself, the biggest is a 7 K x 9K full-frame imager [4], the largest integrated circuit ever made [5].

Other options which were added to this *bouwblok* concept are a set of colour masks (RGB Bayer pattern) and a metal light shield, which has an area equivalent to the 1 K x 1 K block. In this way the *bouwblok* system contains not only full-frame and monochrome CCDs, but also its frame-transfer alternative CCD and colour image sensors. All devices are fabricated by means of a single mask set (which has only double the number of masks compared to the original 1 K x 1 K set), the same flow chart and the same initial test program. That means that the development cycles of the image sensors which fit into this concept become very short, that the development efforts are limited (no design efforts, no lay-out efforts, no mask costs), that the characteristics of the devices are very well predicted and that a mix of device types can be fabricated on a single wafer or in a single run.

4. Examples of imagers realized

Several of these large-area imagers have already been fabricated by means of this stitchable building-block concept. Examples are :

- a 1 K x 1 K frame-transfer imager, intended for medical applications,
- a 2 K x 2 K full-frame imager : monochrome for medical applications, and colour for digital still-photography,
- a 3 K x 2 K full-frame imager : monochrome and colour for still photography
- .....,
- a 7 K x 4 K full-frame imager for digital mammography,
- .....,
- a 7 K x 9 K for astronomy [5].



Photograph. *A 6" wafer is shown of a 7 K x 9 K device.*

A photograph of the 7 K x 9 K is included. Note that smaller 1 K x 1 K frame-transfer imagers are placed along the edges of the wafers. The reason for fabricated the smaller devices together with the larger arrays on the same wafer is to use them as test vehicles.

5. Characteristics of the imagers

One of the strengths of this technology can be found in the fact that the characteristics of the imagers are predictable, although the imager of a particular size might never have been processed before. Several properties of the CCD are independent of the overall array size. Examples include the light sensitivity and conversion factor. Other properties of the imagers such as the transport speed are scaleable with the width or the length of the imager.

A few characteristics which are fixed for the modular building-block architecture are summarized in the following table :

Pixel size	12 µm x 12 µm
Noise amplifier @ 5 MHz pixel rate	23 electrons
Bandwidth of the output stage	120 MHz
Conversion factor	10 µV/electron
Charge-handling capability	250,000 electrons
Quantum efficiency @ 550 nm	38 %
Dark current @ 60 ^{o}C	250 pA/cm^2
Pixel random non-uniformity	< 1 %

Examples of parameters or numbers which are depending on the array size are given in the following table, considering an mK (horizontal) by nK (vertical) device :

Number of horizontal pixels	m x 1024
Number of vertical pixels	n x 1024
Capacitance of array gates	m x n x 1 nF
Capacitance of read-out gates	m x 50 pF
Maximum vertical transport	500 kHz /(m^2)
Maximum horizontal transport m <= 3	40 MHz
Maximum horizontal transport m > 4	40 MHz/(m-2)^2

6. Conclusions

A new concept to design and fabricate CCD image sensor is described. The main advantages of this concept are :

- short development time,
- reduced development costs,
- common testing strategy for the complete family,
- predictable characteristics of new family members.

The *bouwblok* architecture is applied to a series of large devices : frame-transfer and full-frame architectures, monochrome and color devices belong to the same stitchable family. Further options offered are quadruple read-out or read-out through a single output stage, on-chip charge binning and on-chip selective sub-sampling. Applications of this family of image sensors can be found in all kind of professional imaging business ranging from medical, digital photography, military, machine vision, industrial, scientific and astronomical imaging functions.

7. References

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