An mK × nK Modular Image Sensor Design

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ABSTRACT

A 1K × 2K full frame sensor demonstrates a new modular sensor design. Each imager in the family is built from smaller, abutable blocks which are exposed in the correct position during lithography. These blocks can be stacked to form sensors of arbitrary size, all based on the same pixel structure. These pixels have a high charge handling capability, vertical anti-blooming, electronic shuttering, a high light sensitivity, and low dark current.

INTRODUCTION

As production yields have increased, CCD manufacturers have been able to offer ever-larger devices. This growth comes at a price: lithography equipment with a wider field of view has larger feature sizes, which limits performance.

The solution to this takes advantage of the repetitive structure of CCD imagers in order to split the design into smaller blocks that can be exposed by steppers with smaller critical dimensions. Building the sensor involves positioning each piece within the sensor and exposing the resist underneath [1,2]. In this manner one can make large area sensors with a pixel structure that was, until now, impossible. There are other advantages. A carefully made division is modular: sensors of arbitrary size can be built from the same blocks. The pieces may be more compactly placed on reticles, reducing mask costs. Design changes are also cheaper, requiring fewer new masks if they are confined to the smaller blocks. Finally, a sensor can be quickly put into fabrication, needing only new control programs for the lithography equipment.

The final design contains blocks based on 1024 (1K) pixels. These pixels, with narrow channel stops and non-overlapping gates, have a large charge handling capability and vertical anti-blooming. Windows between the gates improve the light sensitivity, and dark current is low. The devices can bin (combine) pixels horizontally and vertically and may be divided into horizontal and/or vertical halves during read-out. The design includes a light shield for frame transfer applications and color filters. The smallest sensor that can be built is a 1K × 1K full frame imager; the largest, for a 6" wafer, a 7K × 9K imager.

Specifically, a 1K × 2K full frame sensor demonstrates the performance of this modular design.

TECHNOLOGY

The process for these sensors uses one metal and three polysilicon layers, as used in other imagers from Philips. Each pixel, 12 × 12 μm^2, has four non-overlapping gates [3] with windows above the channel stops (Figure 1). A p well between the n channel and n substrate raises a barrier for vertical anti-blooming; proper clocking will give electronic shuttering. For read-out, each cell in the horizontal register, a three phase CCD, is large enough to hold two lines for vertical binning. The last (summing) gate is independently driven and made over-sized to store up to two vertically binned pixels. The amplifier is a three stage source follower that can operate at 40 MHz pixel rates and can handle very large charge packets.

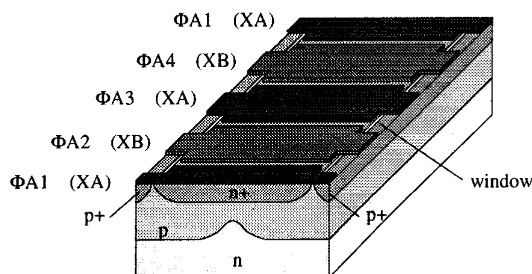

Figure 1. Pixel structure of the imager.

ARCHITECTURE

All sensors in the family have the same basic architecture, similar to others in their class (Figure 2).

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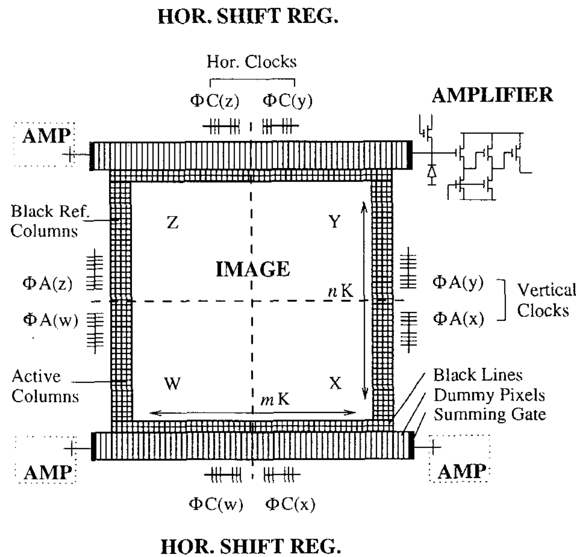


Figure 2. Architecture of the modular sensors.

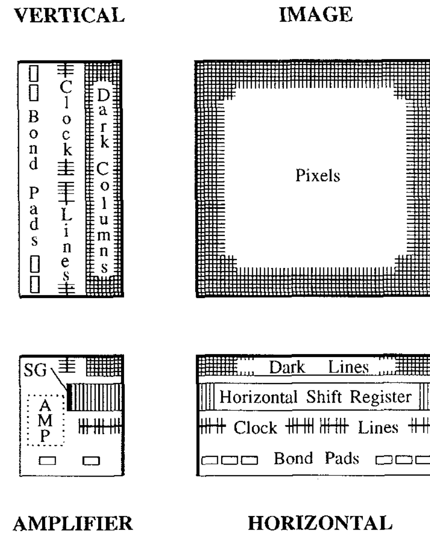


Figure 3. Basic division of the layout.

The vertical and horizontal CCD's are split in the middle of the device. Each half can clock either in the same direction, so that all packets move towards one side of the imager, or in opposite directions, dividing the sensor in two. The read-out modes include driving the whole sensor through any one amplifier, each vertical or horizontal half through two, or each quadrant through its own. This division also means that frame transfer sensors, which need two sets of vertical clocks, can be made. Binning is done by clocking multiple lines into the horizontal register during vertical transport, or multiple pixels under the summing gate (SG). Outside the mK $\times$ nK imaging array there are a number of extra columns and lines for black reference and timing (Table 1).

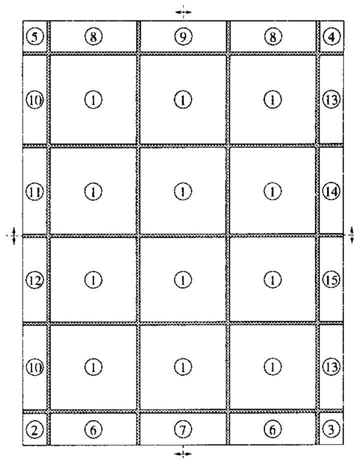
Table 1. Geometrical specification of the sensor.

<u>General</u>	
Sensor Type	1K × 2K Full Frame
Number of Pixels	1024 × 2048
Extra Pixels	
Active Columns	2 × 4
Black Reference Columns	2 × 20
Black Lines	2 × 6
Dummy Register Pixels	2 × 7
<u>Architecture</u>	
Number of Output Registers	2
Number of Amplifiers	4
Clocking	progressive
Split sensor vertically	yes
horizontally	yes
Vertical binning	in horizontal register
Horizontal binning	under summing gate

BLOCK LAYOUT

The heart of an image sensor is the pixel array and this is the basis for dividing the sensor (Figure 3). A matrix of 1024 × 1024 pixels defined along the channel stops and under one gate forms the image block. Its size is a trade-off between longer exposure times with smaller blocks (more stepping for larger sensors) and a better packing on the reticle. Outside the image section the peripheral circuits split into three pieces. The horizontal block includes the sensor's dark lines, horizontal shift register, and possibly bonding pads and a temperature reference diode. In the corner lies the amplifier, the end of the register, bonding pads, and the pixels common to the extra lines and columns. The vertical block contains the extra columns, vertical clock lines, and possibly bonding pads.

The general mK $\times$ nK solution contains many blocks. All the possibilities of clock routing in the periphery make this number large. Both the horizontal and vertical clock lines must be split in the middle of the sensor to read out each half separately, and this occurs either in the middle of a block, if m or n is uneven, or along the edge between two. In sensors with three or more pieces per side, there must also be continuous connections from the middle to the corners (Figure 4). Each of these possibilities requires separate blocks. The routing options also include bonding pads, which must lie adjacent to the amplifiers but not in the middle of the sensor.



Block Key

1	Image (1K × 1K)	10/13	Vertical Block bonding pads continuous routing
2/3	Amplifier W/X		
4/5	Amplifier Y/Z		
6/8	Horizontal Block bonding pads continuous routing	11/14	Vertical Block no bonding pads routing split on edge
7/9	Horizontal Block no bonding pads routing split middle	12/15	Vertical Block no bonding pads routing split on edge

Figure 4. Block diagram for a 3K × 4K sensor.

Only one layer needs to cover all the possibilities: the interconnect. The other layers (gates and implantations) form the structure of the sensor and if their horizontal and vertical blocks are carefully designed, they can be re-used in any position along the edge. This reduces the number of distinct pieces. An example is the bonding pads (see Figure 5 for an example). A sensor with a 1K edge has amplifiers on both ends of the block, and needs two sets of bonding pads within the edge. Larger sensors have an amplifier at only one end and need only one set of pads. Rather than designing blocks for the three cases (bonding pads on each of the two ends, or both), however, all sensors use the 1K block. The interconnect will determine which of the pads are used.

STITCHING

Piecing the blocks together during lithography is called stitching. Although this technology has been used in other types of devices with large areas, for example flat panel displays [4], image sensors are much more sensitive to changes in the pixel structure. The danger is that non-uniformities will be visible in the image along stitch lines. One cause is mis-alignments, due to the inherent imprecision of the step-and-repeat cycle. Others are variations in focus and illumination energy between steps. The sensitivity of the sensor to these effects will vary with implantation dose and driving conditions. The goal is to provide a smooth transition across the stitch line, so that discontinuities do not cause appreciable deviations. Special structures along the edges of each block fulfill this.

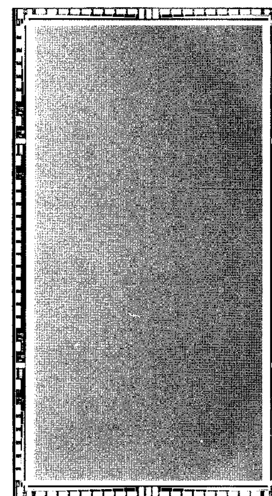


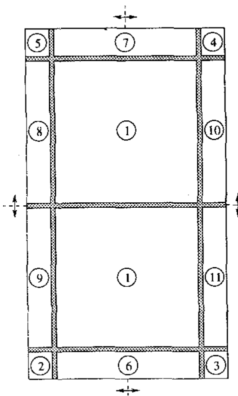
Figure 5. The 1K × 2K modular imager.

1K × 2K FULL FRAME IMAGER

The fabrication of a 1K × 2K full frame imager built from a complete modular mask set demonstrates this concept. Figure 5 shows the result, and Figure 6 the block diagram. Table 2 gives some electrical measurements from this device. The performance is as designed. No stitch lines are visible on a monitor between the image sections.

CONCLUSION

The 1K × 2K full frame imager is but one example of the mK × nK layout. This is a family of large area, high performance sensors. The pixel design can store large packets and has anti-blooming, a low dark current, and high light sensitivity. Architecturally, the sensors have four output amplifiers and may be split in half vertically and/or horizontally through any or all of the outputs. The design also supports binning. These sensors are built by exposing smaller blocks within the imager's bounds



Block Key

1	Image (1K × 1K)	8/10	Vertical Block bonding pads routing split on edge
2/3	Amplifier W/X		
4/5	Amplifier Y/Z		
6/7	Horizontal Block bonding pads routing split middle	9/11	Vertical Block bonding pads routing split on edge

Figure 6. The blocks used to build the imager.

using a wafer stepper during lithography. There are four basic types: a 1K × 1K image array, horizontal and vertical slices of the periphery, and an amplifier. The general solution also distinguishes between the structure of the CCD (gates and implantations) and the interconnect. This difference minimizes the total number of blocks needed to cover all possible combinations by placing most of the complexity in one layer. This solution includes all sensors, full frame or frame transfer, with or without color, based on one pixel design, and ranging in size from 1K × 1K to 7K × 9K (on 6" wafers).

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Table 2. Electrical specification of the sensor.

Q_{max}	> 200 000 electrons
Quantum Efficiency (530 nm)	27 %
Random Non-Uniformity	< 1.0%
I_{dark} (60°C, non-MPP)	< 0.5 nA/cm^2
Amplifier Bandwidth	> 100 MHz
Conversion Factor	4 μV/electron
Readout Frequency	40 MHz
Vertical Frequency	500 kHz
Electronic Shuttering Pulse	-5 V 2 μs to image clocks

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