

A Low-Noise, Highly-Sensitive, 1", 2.2 Mpixel FT-CCD Imager for High-Definition Applications

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Abstract

A new, highly-sensitive HDTV frame-transfer CCD imager that has a very low noise by surface pinning and by an optimized output-amplifier design is reported. FPN at 60°C has been lowered by 90% and the noise over the full bandwidth is lowered by 30% compared to our previous device presented by Theuwissen *et al.* [1]. This imager combines for the first time the dark current reduction method "All-Gates Pinning", optimized with respect to charge-handling capacity and sensitivity, with membrane polysilicon technology for use in professional broadcast cameras.

Introduction

Two sources of noise determine the performance of present CCD imagers: output-amplifier noise and fixed-pattern noise (FPN) caused by dark current non-uniformities. Strategies to reduce the output amplifier noise by reducing the total capacitance at the floating diffusion node have been presented by Centen [2] and are applied to this imager by making the amplifier layout very compact.

A well-known way to completely suppress interface-state generation in buried-channel CCDs is to invert the surface, i.e. have a layer of holes at the Si-SiO₂ interface during integration [3]. This has been realized in the photodiodes of Interline Transfer CCDs by means of a shallow surface *p*-type layer [4] and in Frame Transfer CCDs by an inversion layer of holes at the surface generated by setting all gates at a sufficiently low level [5]. In FT-CCDs this mode of operation is called "All-Gates Pinning" (AGP). The introduction of AGP in an FT image cell is not simple because the functions of integration and transport are combined into the same cell and the other properties of the pixel (charge-handling capacity, anti-blooming capability, electronic shutter, etc.) cannot be compromised. So, until now the AGP approach was used only in consumer applications, while high-end applications used the charge-pumping technique [6]. In this work, the AGP method is optimized with respect to charge-handling capacity and sensitivity for use in professional broadcast cameras.

Dark current reduction with AGP

The dark current reduction in AGP can be calculated using the following theory. The surface dark current I_d is given as:

$$I_d(nA) = 10^9 q G_{surf} A_{pix} N_{pix} \quad (1)$$

with q the electron charge in [C], G_{surf} the surface dark current generation in [$cm^{-2}s^{-1}$], A_{pix} the pixel area in [cm^2] and N_{pix} the number of pixels.

The bulk generation G_{bulk} in [$cm^{-3}s^{-1}$] is given by the Shockley-Read-Hall equation [7] and corrected for trap-assisted tunneling [8]:

$$G_{bulk} = \frac{n_i^2}{(n_i+p)\tau_n + (n_i+n)\tau_p} (1+\Gamma) \quad (2)$$

with n_i the intrinsic charge density, n the free electron density, p the free hole density, Γ the field effect function, τ_n and τ_p the lifetimes of electrons and holes, respectively. Under the assumption that $n=0$ and $\tau_n=\tau_p=\tau$, eq. (2) results in:

$$G_{bulk} = \frac{n_i^2}{(2n_i+p)\tau} (1+\Gamma) \quad (3)$$

The surface generation G_{surf} [$cm^{-2}s^{-1}$], only valid for $p=0$ and the electrical field component $E=0$, if a constant

density of interface states is assumed throughout the bandgap, results in [9]:

$$G_{surf} = \pi \frac{kT}{q} D_{it} \sigma v_{th} \frac{n_i}{2} \quad (4)$$

D_{it} represents the interface trap density in [$eV^{-1}cm^{-2}$], σ the capture cross-section in [cm^2] and v_{th} the thermal velocity [cm/s]. For $p \neq 0$ and $E \neq 0$, eq. (4) is modified analogous to the bulk generation (eq. (3)). In this approximation, $n_i/2$ is replaced by

$$\frac{n_i^2(1+\Gamma)}{(2n_i+p)} \quad (5)$$

This results in a surface generation of

$$G_{surf} = \pi \frac{kT}{q} D_{it} \sigma v_{th} \frac{n_i^2(1+\Gamma)}{(2n_i+p)} \quad (6)$$

For a sensor with AGP, the surface hole concentration p is higher than without. (6) shows that this lowers G_{surf} : the generation rate is reduced.

It is possible to make an accurate estimate of the surface dark current of the imager, using the output of the 3D electrostatic device simulator PADDY. This was first demonstrated by Toren *et al.* [10] and can also be applied on AGP sensors. PADDY integrates (5) over the complete pixel area. This results in the following factor:

$$F_{PADDY} = \int \frac{n_i^2}{(2n_i+p)} (1+\Gamma) dA \quad (7)$$

For the surface dark-current of the sensor is found:

$$I_d(nA) = 10^9 q N_{pix} \int G_{surf} dA = 10^9 \pi k T D_{it} \sigma v_{th} F_{PADDY} N_{pix} \quad (8)$$

The first two variables are determined from experimental data in different parts of the image pixel [10]. Substitution of these values results in the total dark current of the imager.

Development of the AGP imager

Fig. 1 shows a schematic representation of the imager. The design parameters and technology are summarized in Table 1. The basic image pixel is a four-phase cell constructed of two polysilicon layers, using two short "thick" ($0.3 \mu m$ thick, $25 \Omega/\square$) poly-1 and two long "membrane" ($0.05 \mu m$ thick, $1000 \Omega/\square$) poly-2 electrodes per pixel. A cross-section along the transport direction in the middle of the cell is shown in Fig. 3. A conventional $n-p-N_{sub}$ structure is used for the CCD with vertical anti-blooming. A p^+ channel-stop implant separates the columns. To be able to perform the frame shift in this large imager, the RC -time constants in the CCD electrode network need to be as low as possible. This is achieved by significantly lowering the capacitances by reducing drastically the overlap of the polysilicon electrodes and the resistances of the CCD network by using low-resistance vertical tungsten shunt wiring [11]. Since the $0.9 \mu m$ wide straps lie above the p^+ channel stops which are less light-sensitive, the sensitivity of the imager is almost unaffected.

Because all gates are set to a low voltage for pinning, an additional n -type implant $DN2$, self-aligned on poly-1 under the poly-2 gates, is introduced to obtain a modulation of the channel potential such that charge packets can be kept separated. The resulting potential profiles are shown in Fig. 4. The length of the poly-1 gate and the dose of the $DN2$ enhancement implant are the critical factors for the pixel performance. They determine both the barrier between neighboring pixels and the transport from one poly-2 gate to the next. A limit on the high clock voltage is given by the injection of electrons from the substrate to the CCD channel. The low clock voltage is essentially limited by pinning conditions (Fig. 5a,b).

In a first AGP approach [5], the poly-2 and poly-1 gates were connected and two-phase transport was

achieved. The solid line in Fig. 5b shows the conditions for maximum $DN2$ dose during transport, the dotted line shows the effect of an increase in $DN2$ dose: a barrier will arise at point "A" under poly-1 (high). By combining the $DN2$ implant for AGP with a four-phase transport scheme with built-in voltage offset between the poly-1 and poly-2 gates, a significant increase in maximum charge handling is achieved (Fig. 5c) compared to the two-phase solution. The barrier at point "A" in Fig. 5b is eliminated by a higher voltage on poly-1 (high) and/or a lower voltage on poly-2 (low). The main difference with the two-phase version with respect to the dopants is an increase of the top dope of the enhancement implantation $DN2$ with 30%. The result is a 50% increase in charge-handling capacity. The 2D output of a 3D device simulation (PADDY) of integration in the image pixel is shown in Fig. 6. The maximum charge measured is 60,000 electrons for an overexposure handling of 10^5 . The PADDY output for transport in the image section is shown in Fig. 7. With similar doping profiles, complete charge transport in two-phase mode would be impossible, as shown in the same figure. In order to avoid injection from the substrate to the CCD channel, the total CCD implant ($DN+DN2$) under the poly-2 gate must not exceed a certain maximum. Since the charge capacity is determined to a large extent by $DN2$, the DN dopant could be reduced to avoid injection. However, because of this, a problem with the first doping profiles for AGP was a significant reduction in collection volume of the image pixel (and thus quantum efficiency). This new approach uses optimized doping profiles for both CCD channel and p well to obtain a deep collecting well over the whole area of the pixel and consequently to have collection also in the non- $DN2$ implanted areas. Fig. 8 shows the collection depth (for the generated electrons) in the middle of the pixel.

Results

From this HDTV imager the following results were obtained:

- The compact amplifier design reduces the total amount of noise electrons in the complete video band of 30 MHz from $20e^-$ to $14e^-$ after optimal signal pre-processing and increases the responsivity from 10 to $14 \mu V/e^-$ at the floating diffusion.
- The FPN of the imager is lowered from $40e^-$ to less than $3e^-$ (30 MHz) at $60^\circ C$ (Fig. 2) by suppressing the generation at interface-states by inverting the complete surface during integration.
- The quantum efficiencies for red (610 nm), green (540 nm), and blue (450 nm) are improved from 15%, 19%, and 13% to 20%, 30%, and 23%, resp. with respect to the conventional device [1] because of the membrane polysilicon layers, and the improved collection depth in AGP.

Conclusion

A new 1", 2.2 Mpixel imager is presented. It has an excellent signal-to-noise ratio from an optimized amplifier design and four-phase AGP, and a high sensitivity by the optimization of the AGP method with respect to collection depth and by membrane polysilicon layers. Table 2 summarizes the performance of the device.

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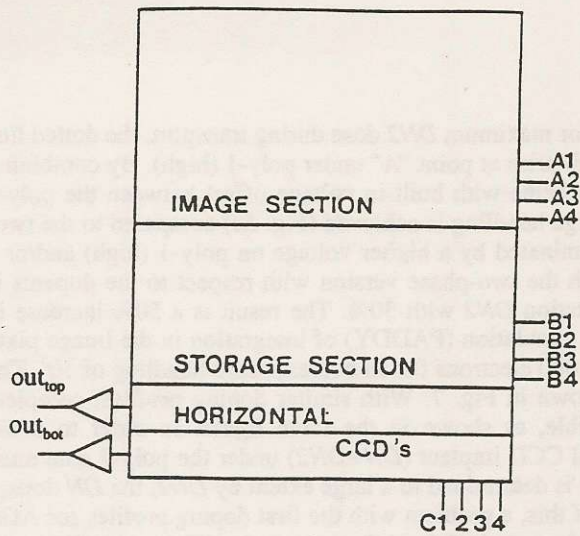


Fig. 1: Device architecture.

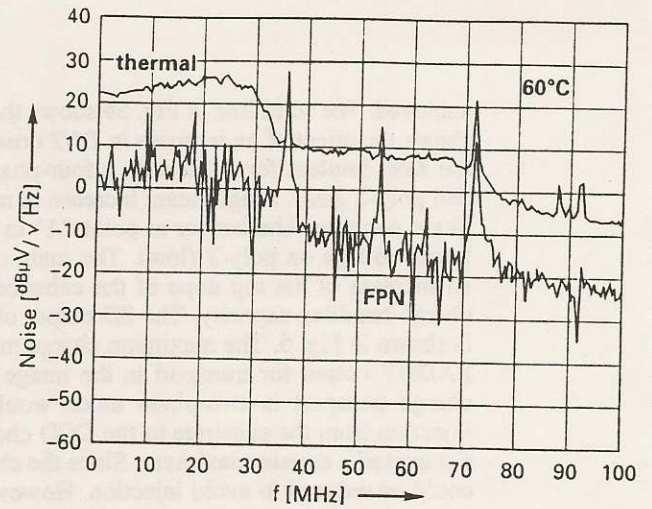


Fig. 2: Thermal noise and FPN versus frequency in HDTV sensor with AGP.

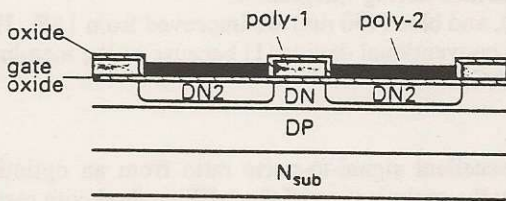


Fig. 3: Cross-section of AGP cell along transport direction.

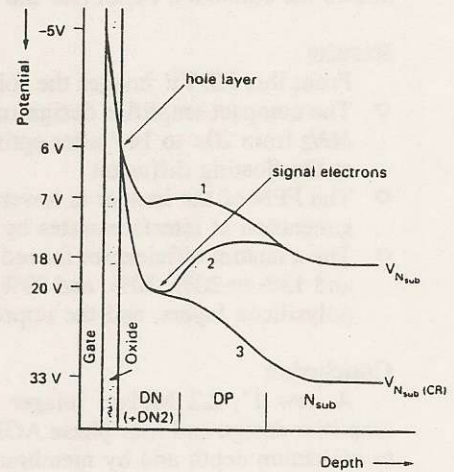


Fig. 4: Potential profiles for AGP. curve 1 shows the potential profile under the short thick gate, curve 2 shows the same under the long thin gate with an additional DN2 channel implant. Since the layer of holes at the interface "pins" the interface voltage, the electronic shutter function by setting all the gate voltages "off" is no longer possible. Now charge reset is obtained by giving a pulse on n substrate (N_{sub}); the resulting potential profile under the poly-2 gate is shown in curve 3.

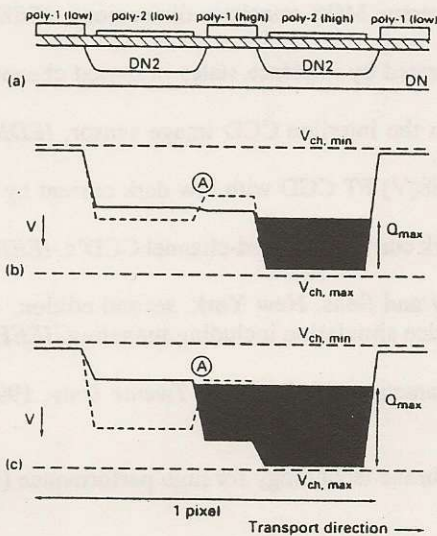


Fig 5: Cross-section pixel in transport direction. (a) electrode and doping structure; (b) potential distribution (maximum DN2) for two-phase operation; (c) the same for four-phase operation.

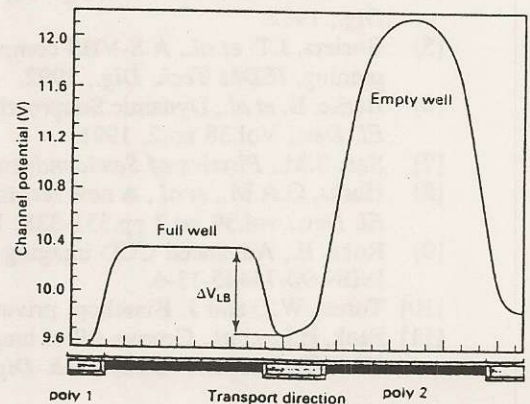


Fig. 6: Output of 3D simulation (PADDY) of integration in the image pixel showing the maximum channel potential in the pixel along transport direction.

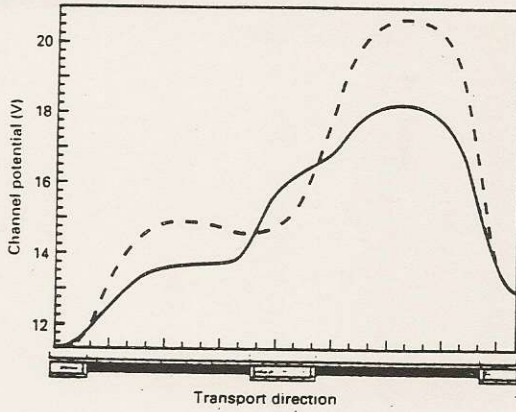


Fig. 7: Output of 3D simulation (PADDY) of transport in the image pixel for four-phase transport (solid line) and two-phase transport (dotted line), for the same DN2 doping profile.

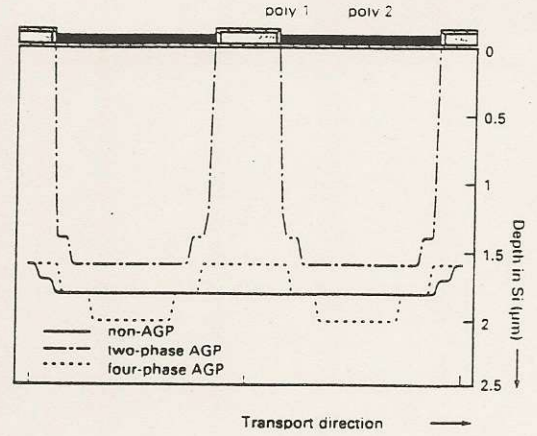


Fig. 8: Collection depth in four-phase AGP pixel compared to the two-phase solution.

CCD type	Frame Transfer, 1"
Number of active lines	1152
Number of pixels/line	1920
Number of fields/sec	50
Interlacing	2:1
Aspect ratio	16:9
Image diagonal	16 mm
Image area	109 mm ²
Pixel size	7.25 μm(H)×13.6μm(V)
Chip area	240 mm ²
Minimum features	0.9 μm

Table 1: Design parameters.

Frame shift frequency	1.125 MHz
Readout frequency	36 MHz
Pixel frequency	72 MHz
Smear (in camera)	none
Overexposure	10 ⁵
Charge-handling capability	60 000 e ⁻
Quantum efficiency:	
red (610 nm)	20%
green (540 nm)	30%
blue (450 nm)	23%
FPN (60°C)	3 e ⁻
Outamp noise	14 e ⁻
Bandwidth output stage	150 MHz

Table 2: Sensor performance.