

REAL-TIME IMAGING WITH MEGA-PIXEL CHARGE-COUPLED DEVICES.

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Abstract.

A technology is described which allows the application of real-time imaging in combination with mega-pixel CCDs. This technology is based on the following characteristics : high-speed transport of the video information through the parallel CCDs in the imaging section, very high-speed transport of the charge packets through the serial section of the devices, and high-speed conversion of the electrons to a measurable voltage by the output amplifier. Key competences to comply these requirements are : low-resistive CCD gates, low-capacitance CCD gates and high bandwidth and low noise floor output stages.

Key words : charge-coupled devices, solid-state imaging, real-time imaging, high-resolution imagers, CCD technology.

Introduction.

Real-time imaging by means of very high-resolution image sensors is an important feature for high-end surveillance applications. In parallel with the introduction of high-speed analog to digital convertors (e.g. 40 MHz) for video signals, high-resolution devices driven in real-time video mode for machine vision, robots or other industrial applications have also become commercially available.

But the CCD technology applied in the classical consumer application area or in the field of scientific imagers is not optimized to fulfill the requirement of delivering 60 or 50 fields per second in combination with mega-pixel resolution. In the consumer field, imagers have up to 500,000 pixels per frame and deliver data rates up to 18 MHz. On the other hand, scientific devices have several million pixels but give only a few frames per second, resulting in a 15 MHz video signal through a single output stage.

To overcome these shortcomings, devices are developed with multiple outputs in such a way that the data available in the CCD is brought in parallel to the outside world through different output stages. By using this technique the overall data rate is increased but real-time imaging at video rates becomes very complicated

because all the video data has to be reshuffled. This paper describes a CCD technology (or a combination of several sub-technologies) which makes it possible to :

- deliver 60 Hz field rate video through a single output stage at a speed of 40 MHz. This allows a 1 Mpixel device running at 60 Hz in an interlaced mode [1],
- deliver 60 Hz field rate video through a double output stage with a special pixel interleaving option which makes the reconstruction of the video information very simple (without external memory). These characteristics are needed to drive a 2.2 Mpixel device at 60 Hz in an interlaced video mode [2],
- deliver 120 Hz field rate video coming from a standard consumer type imager through a single output stage,
- derive a 30 Hz field rate coming from scientific imagers having more than 4M pixels and supplied to the output world through a dual output stage, making use of the former interleaving pixel read-out.

Silicon of the first three device options is commercially available; the fourth option is only a speculation.

Required CCD technologies.

After the integration of the video information in the light-sensitive part of the charge-coupled devices, the charge packets have to be transferred to the outside world. This action takes place in the following sequence :

- shifting the charge packets through the parallel CCD channels in the light-sensitive part of the device (in case of imagers with an on-chip memory, the charge packets also have to be shifted through the CCD channels of the memory zone). This parallel shift takes place at frequencies in the lower MHz or upper kHz range.
- shifting the charge packets through the serial output register of the CCD towards the output amplifier. The speed of this serial transport goes at the same pace as the data rate at the output node of the device. A typical value for the transport clock frequency lies around 40 MHz.
- splitting the horizontal output register into different (e.g. two) parallel registers. In this demultiplexing structure odd numbered pixels can be transported in one channel and the even numbered pixels through a second. Off-chip the signals from the two registers can be demultiplexed again to reconstruct the original video signal. This multiplexing technique can be done in a very simple way without the need for an external memory.
- converting the charge packets to an electrical voltage and buffering this signal to the external world. The conversion of time-discrete CCD signals by means of a floating-diffusion detector puts some extreme demands on the electrical characteristics of the output amplifier : its bandwidth has to be at least three times the pixel rate, and it must have low thermal and $1/f$ noise.

To comply with all these needs, current CCD processes available make use of a combination of set of basic technologies, which are described further in the paper.

Minimum overlap capacitances.

An optimisation in the processing flow-chart is done to lower the overlap capacitances of the CCD gates to an absolute minimum (or no physical overlap at all on the chip itself) [3]. This technique allows for minimum driving capacitances and results in high speed (low RC constants) and/or low power dissipation (low values of $C.V^2.f$).

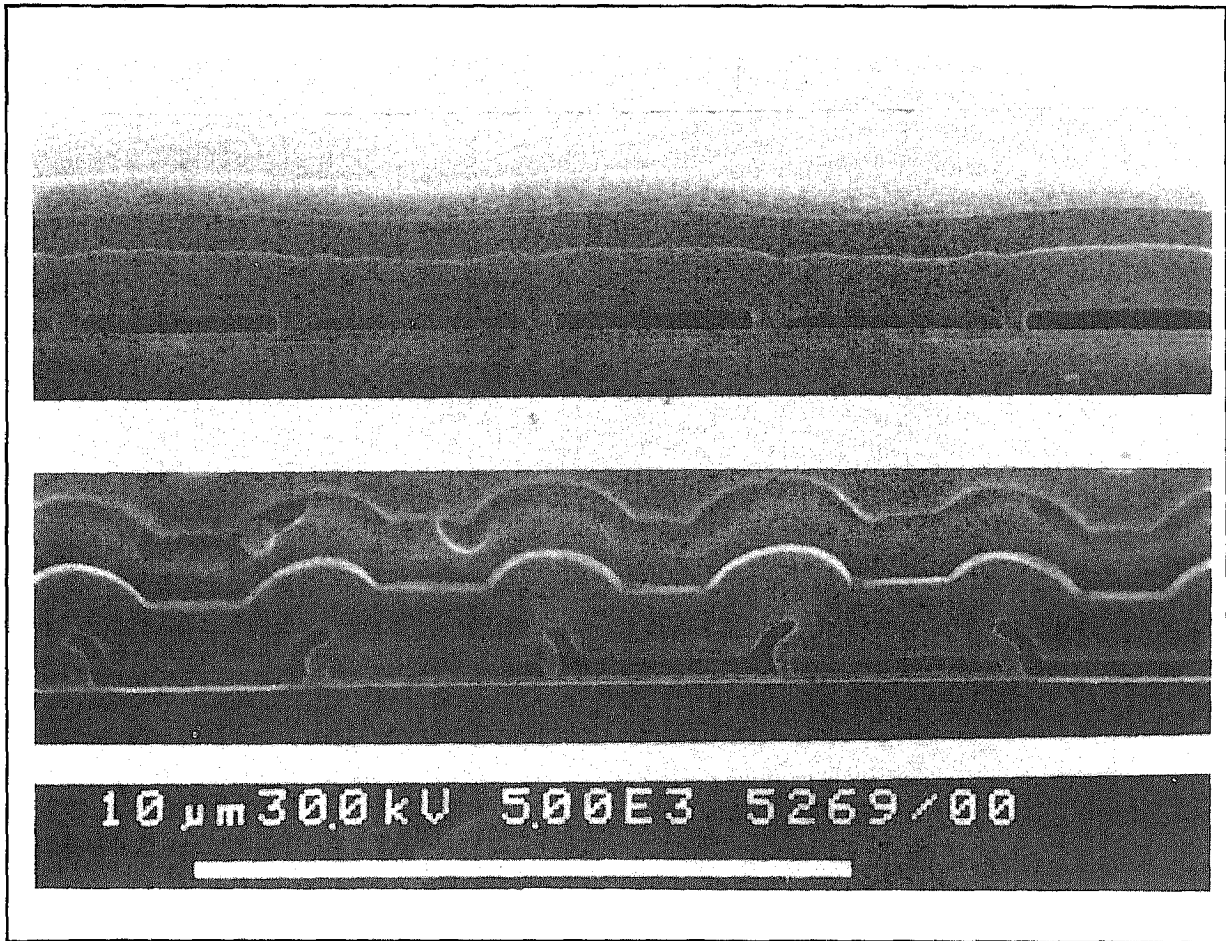


Figure 1. Cross-sections of the CCD-gate structure, taken along the transport channel. Bottom : old situation with overlapping gates, top : new situation with contiguous gates.

Figure 1 shows the results of this new processing technique. Shown are two cross-sections of a CCD channel along the transport direction. The CCD gates can be easily recognized as the black areas adjacent to each other. The previous technology with overlapping CCD gates is shown in the photograph at the bottom; the new situation with contiguous CCD gates is shown in the photograph of the

top. It can be well understood that with the contiguous gate structure the overlap capacitances can be decreased substantially. Yet this does not sacrifice transport efficiency. The inefficiency stays well below 5×10^{-6} /transport.

Strapped CCD gates.

A tungsten-strap technology is introduced in the CCD processing to lower drastically the resistance of the CCD gates in the parallel imaging (and possible storage) zone [2]. Classical CCD gates are made out of poly-crystalline silicon with a sheet resistance of about 30 Ohms/sq. Tungsten straps can be made with a sheet resistance of 0.1 Ohms/sq. This reduction in resistance is immediately translated in to higher speed for the imager (through the RC constants).

The situation before and after the inclusion of the tungsten straps is illustrated in Figure 2. The upper illustration shows the CCD channels covered by the poly-silicon gates. The gates are tied at each side to bus bars surrounding the image section, made out of aluminum. With this construction, in between two metal-poly interconnects, about 2000 pixels/line are defined in an HDTV image sensor. The gate interconnect with tungsten straps is depicted in the lower illustration of Figure 2. The poly-silicon gates are no longer connected directly to the aluminum bus bars, but instead by means of vertically running tungsten straps. A tungsten interconnect line is located above every channel stop implant and it makes the connection between a bus bar and the appropriate poly-silicon gate. Taking again the HDTV imager as an example, with the tungsten interconnect scheme only 4 pixels are located between two contacts. By comparing the two interconnection schemes, without and with tungsten straps, the decrease in RC constant for this example is a factor of 500.

High-speed horizontal clocks.

A totally new interconnection scheme for the high-speed clocks of the serial read-out register is introduced. It makes use of the availability of the second metal-lisation layer : the tungsten interconnect level. All separate CCD gates are "strapped" with a small shunt wire of tungsten. In this way the resistance of the poly-Si gate is made smaller, the RC constant is reduced, and the overall speed and power dissipation of the system is minimized.

Parallel output registers.

If the foregoing measures to speed-up the output data rate are still not satisfactory, additional speed can be gained from a parallel construction of the horizontal output register [2]. In case of the HDTV imager, two parallel horizontal output registers are used to transport all data through two separate output stages. The construction of the two output registers is chosen such that all odd numbered pixels of a video line are transported in the first horizontal register while all even numbered pixels, of the same video line, are transferred through a second horizontal register. Figure 3 schematically shows this situation. The two output registers are driven fully in parallel and the charge packets are fed sequentially to the outputs. Off-chip a very simple demultiplexing structure is used to reconstruct the original stream of

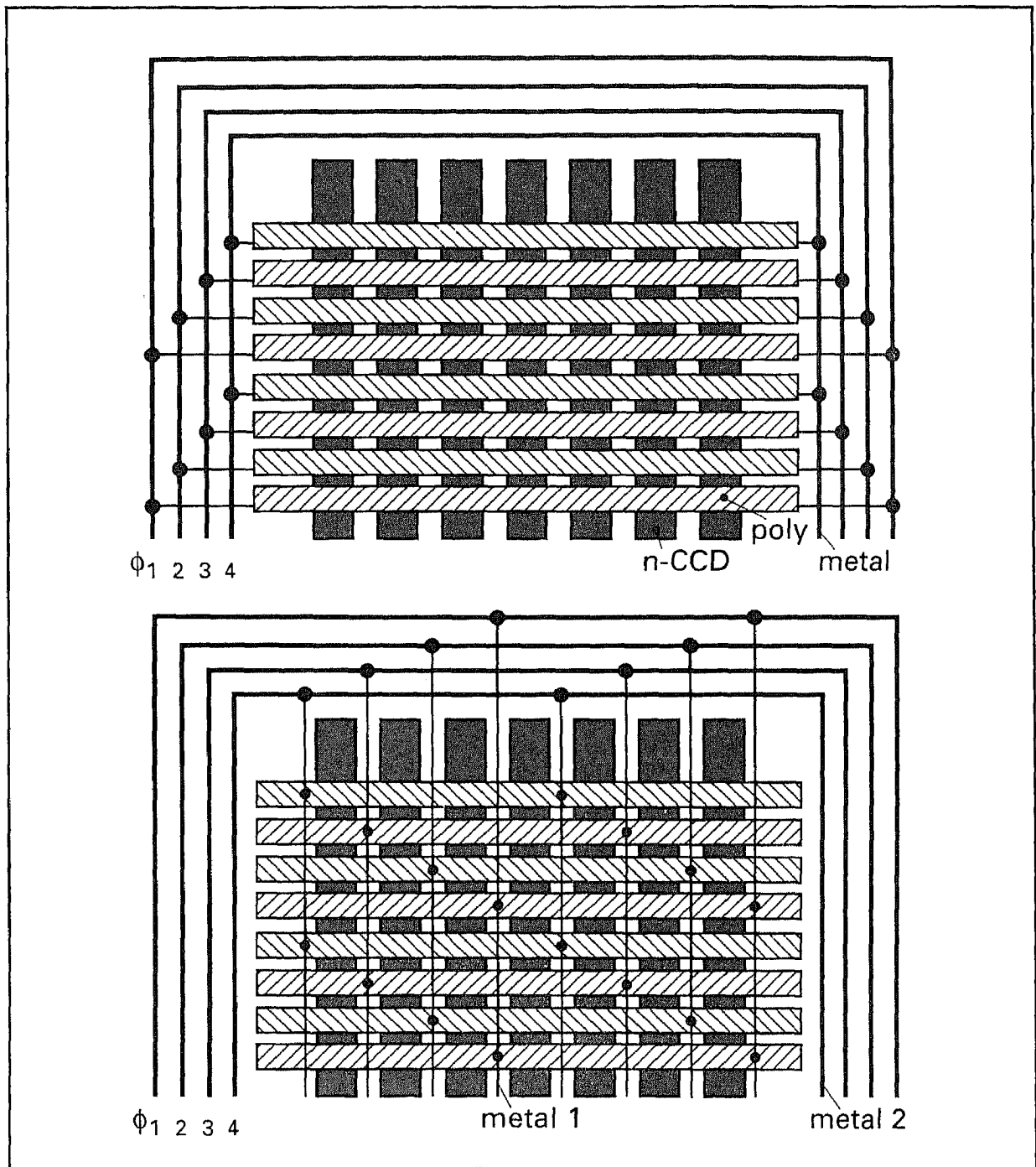


Figure 2. Device architecture without (top) and with (bottom) tungsten straps. The poly-crystalline CCD gates are connected directly or by means of tungsten straps to the aluminum bus bars.

video information. With this architecture of multiple horizontal output registers the clock frequency of the horizontal transport system can be kept low and the power

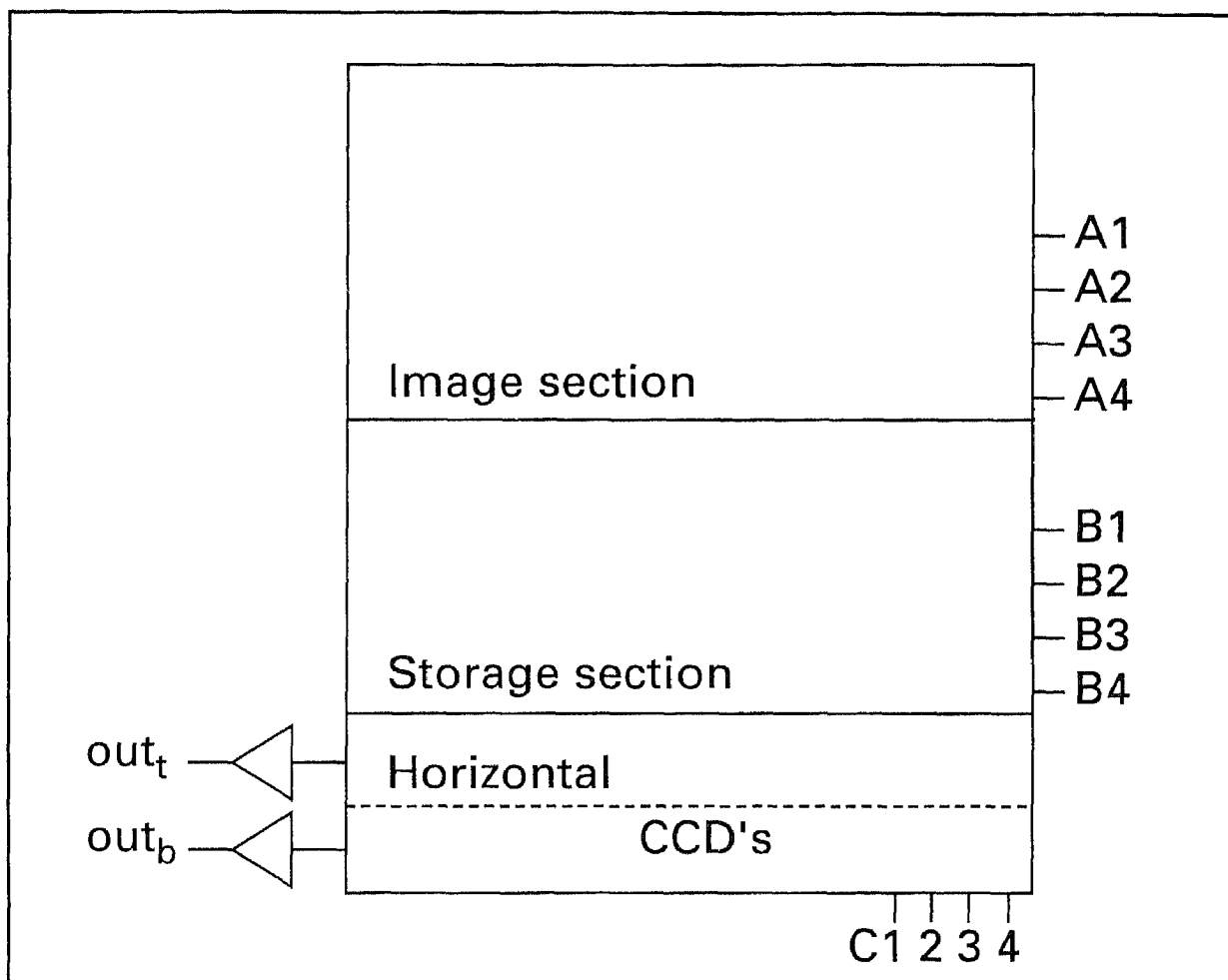


Figure 3. Frame-transfer imager with two horizontal output registers in which the charge packets, coming from the memory zone, are multiplexed. Both registers are read-out fully in parallel.

dissipation on-chip can be minimized [4]. These are two important characteristics which make the application of this method for very high-frequency data rates, as for instance in HDTV imagers, a (very attractive) necessity [6].

The output amplifier.

Figure 4 shows an electrical diagram of the output amplifier which is commonly used in the CCD imaging world : a three-stage source-follower.

With this output stage the small voltage change on the floating-diffusion capacitance is sensed and buffered towards the outside world. The optimisation of the output amplifier is done with respect to :

- the conversion factor, to get as many micro-volts as possible from each electron transported to the floating-diffusion node. This optimisation step is realized by making the capacitance of the floating diffusion as

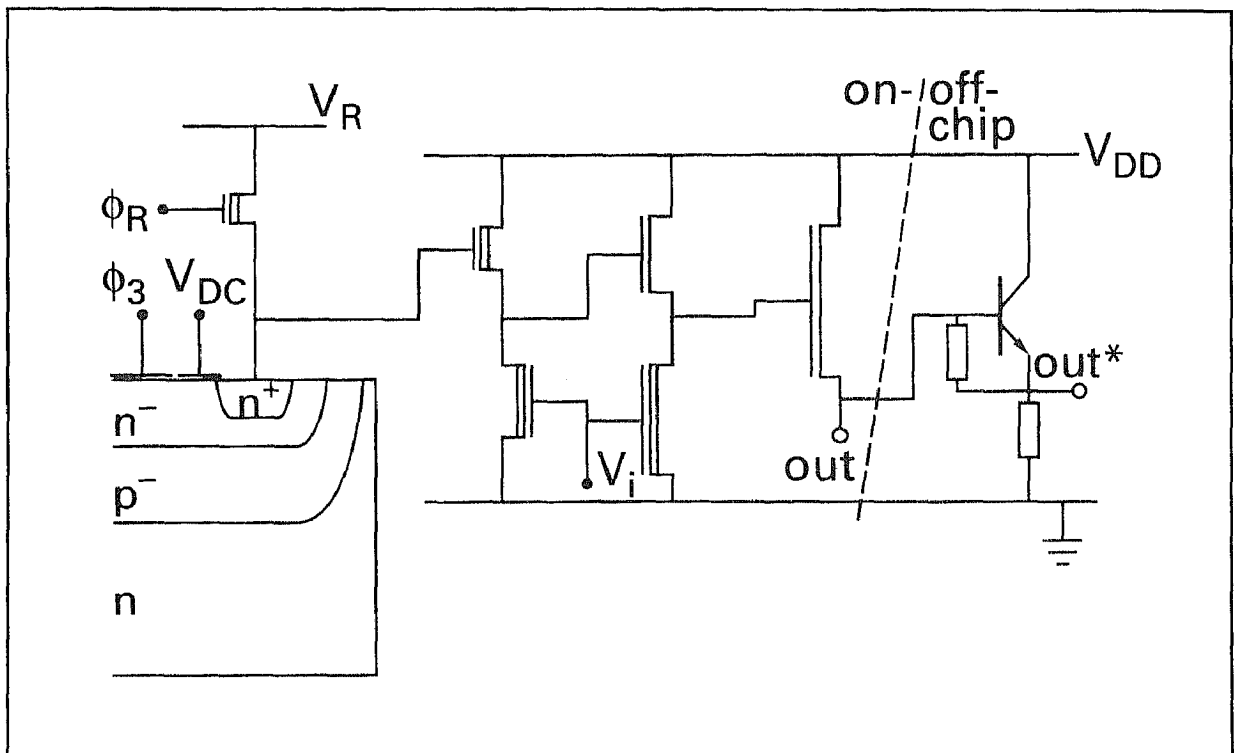


Figure 4. Circuit diagram of the output stage. From left to right : the end of the CCD channel, the floating diffusion with reset transistor and the three-stage source-follower amplifier.

- small as possible through a sophisticated lay-out of the structure.
- the bandwidth of the output stage is made as large as possible, at least three times the output data rate. This can be realized by a very secure adaption of the different stages of the output amplifier to each other.
- the noise performance, as far as $1/f$ noise and thermal noise of the MOS transistors is concerned. Noise is very much dependent on the DC-bias current flowing through the source-follower stages and on the different width versus length ratios of the MOS transistors used in the overall lay-out of the output stage. Both characteristics, the DC-bias current and the physical dimensions of the transistors, are chosen such that both components of the noise, $1/f$ noise and thermal noise, are minimized [5].

Measured results.

The aforementioned CCD technologies are applied in several PHILIPS' products to provide the user with a possibility for real-time imaging with mega-pixel imagers. Two examples are described : the FT8 which is an HDTV-imager with 2.2 Mpixels, and the FT12, which is a device suited for machine-vision applications, with 1

Mpixels. The most important device characteristics and parameters, with respect to the real-time imaging possibility, are listed in the following table.

ITEM	FT8	FT12
Active pixels/line	1920	1024
Active lines/frames	1152	1024
Max. number of fields/sec	60 or 50	60 or 50
Interlacing	2:1	2:1
Vertical frame shift	1.125 MHz	1.5 MHz
Pixel rate	72 MHz	40 MHz
Output conversion factor	6 $\mu\text{V}/e^-$	6 $\mu\text{V}/e^-$
Output bandwidth	160 MHz	120 MHz
Output noise level	19 e^-	16 e^-
Number of parallel CCD	2	1

As can be seen from the data, the devices can run at 60 or 50 fields/sec - real-time video - without sacrificing the resolution of the imager.

Conclusion.

Described are a set of techniques needed to speed-up mega-pixel imagers so that they are able to deliver real-time video. Technologies which are available to fulfill these requirements are :

- minimum capacitances for the CCD-gates,
- minimum resistances for the CCD-gates,
- charge multiplexing methods,
- high bandwidth of the output amplifier,
- low noise floor of the output amplifier.

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