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# CCD IMAGING

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**Abstracts**

A short overview is given about the fundamentals of solid-state imaging. The generation of electrons, through the absorption of photons, the collection of the charges and the read-out of the charge packets are described. Different imager configurations are compared with each other: linear organisations, frame transfer CCD, interline transfer CCD and frame interline transfer CCD.

Keywords: charge-coupled devices, frame interline transfer CCD, frame transfer CCD, interline transfer CCD, solid-state imaging.

## 1. Introduction

During many years the application of imaging for TV purposes was exclusively the application area of imaging tubes, but after the introduction of the first video camera with a solid-state imager as image pick-up element[1]) everything changed very rapidly. At this moment almost the opposite is true: imaging for TV applications is almost exclusively the area of solid-state imagers and in particular charge-coupled devices (CCDs).

From the introduction of CCDs in 1969 until the introduction of the first solid-state camera was quite a long period. The main reason for this is the complexity of the fabrication technology of the imagers. It was not surprising that the first camera was built around an MOS imager, because this device could be fabricated in a somewhat simpler technology which was especially driven by the technology push of the DRAMs. Nevertheless, CCD cameras came soon after cameras with an MOS imager.

The reasons for the change to solid-state imaging from imaging tubes are the many advantages of CCDs over classical imaging devices.

— Compared with tubes, CCDs operate at a much lower supply voltage and consume almost no power.

— Solid-state devices are not sensitive to external electromagnetic fields, whereas tubes with an e-gun inside are.
— Solid-state imagers have a lot of mechanical characteristics more favourable than imaging tubes: they are much smaller in volume and weight; they have a fixed geometry; they are very reliable and robust; they need almost no tuning of voltage settings.
— As far as the optical characteristics of the two challengers are concerned, solid-state devices are almost as sensitive as tubes and show no image lag or burn-in phenomena, but tubes are equal to CCDs when static resolution is compared.
— Last but not least, the cost of solid-state devices has decreased drastically owing to the technology push, and nowadays CCDs are much lower in cost than any tube.

When the CCDs are used in a camera, the camera itself has the advantages of no set-up time, no warming-up time, a very compact camera design, and stable and reproducible performance.

The picture quality of a solid-state imager is superior in all aspects to that of a tube with one exception: the horizontal aliasing effects or moiré effects. These artifacts are generated through the sampling action of a solid-state imager in the horizontal direction. However, tubes have vertical aliasing effects similar to those of CCDs.

All the aforementioned advantages of solid-state devices in general and CCDs in particular have pushed imaging tubes almost completely out of view. Nowadays, only CCDs are used as image sensors for TV applications. In particular, their favourable signal-to-noise ratio compared with those of MOS XY and charge-injection devices makes them attractive for these kinds of applications. For these reasons, attention is paid only to CCDs in this paper.

In Sec. 2 about the basics of solid-state imaging, some elementary aspects about the theory of photon sensing and imager configurations will be explained. This section can be further subdivided into two parts: the photon conversion mechanism and the subsequent electron collection. In Sec. 3, firstly linear devices will be considered, and secondly several possibilities of sensor configurations in the array imaging world will be discussed. At the end of this section an overview will be given of the advantages and disadvantages of the different architectures.

## 2. Photon sensing

Solid-state imaging is based on the physical principle of converting light

(photons) into a measurable electrical quantity (voltage, current). The link between the photons at the input of an imager and the voltages at the output of the device are the electrons. Of great importance in this chain is the capture as well as the transport of these electrons. In this section, attention will be paid to all items involved in the basic operation of solid-state imaging.

### *2.1. Photon conversion*

Energetic particles falling on and penetrating a semiconducting substrate can transfer part of their energy to the substrate. This energy transfer can take place by the generation of electron–hole pairs: if the energy content of the particles is high enough, electrons can be released from the valence band and swept into the conduction band, leaving behind a hole in the valence band. This action reduces the energy of the incoming particle by an amount equal to the energy difference between the conduction and valence bands, i.e. the bandgap. As a consequence, the energy of the particle has to be higher than the bandgap to generate an electron–hole pair.

If this principle is applied to solid-state imaging, photons can create electron–hole pairs in silicon if their energy is higher than 1 eV, or equivalently if their wavelength is shorter than about 1000 nm. After the generation of the charge carriers in the bulk of the semiconductor, the negative electrons have to be separated from the positive holes. The easiest method to achieve this is by the application of an electrical field by which the electrons are caught and the holes are drained to the substrate (or vice versa, depending on the type of substrate).

### *2.2. Charge integration*

However, if the separation is successful, it is almost impossible to transport a single electron or hole to an output stage and to convert it to a measurable quantity: its energy content is much too small. This problem can be circumvented by an integrating action: instead of transferring each single electron or hole, the charge carriers are locally integrated during a certain amount of time into a charge packet. In this way the number of charge carriers in such a packet can be large enough to represent an energy which is easily detectable by the output of the device.

To separate the electrons from the holes and to integrate the charge carriers, a small capacitor is sufficient. Two alternatives are shown in fig. 1: a metallurgical np-junction reverse biased (photodiode) and an externally induced np-junction (MOS capacitor). Both alternatives are based on a p-type silicon substrate. The separation of the electrons and the holes is achieved by the electric field across

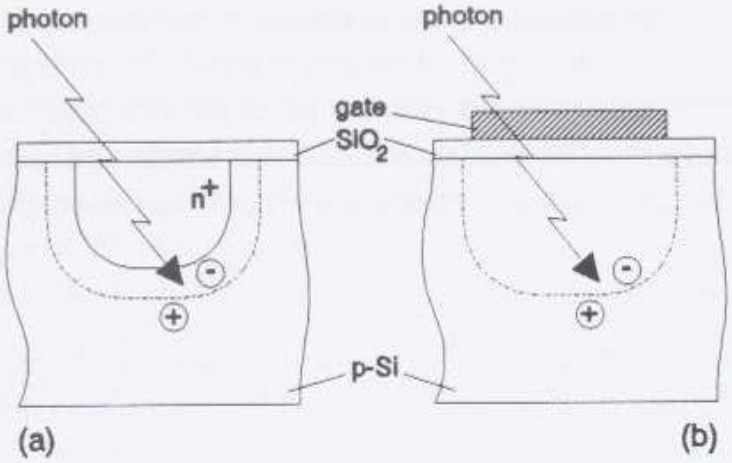


Fig. 1. *a*) A metallurgical np-junction and *b*) a voltage-induced np-junction, both acting as photon-converting sites.

the np-junctions: electrons are caught and holes are drained to the p-type substrate. The integration of the electrons takes place on the reverse-biased and electrically isolated junction capacitances[2]).

In cases in which the voltage across the capacitance decreases, and consequently its depletion region width decreases, the number of electrons integrated or collected will accordingly decrease.

### *2.3. Charge transport*

The next link in the imaging chain is the transport of the charge packets from the integrating sites towards the output of the device. Again two alternatives are shown in fig. 2: an MOS switch with a sense line and a CCD shift register. In both cases the imaging cell or pixel is a photodiode built on a p-type silicon substrate. The choice between the MOS switch combined with the sense line and the CCD shift register is somewhat application dependent because both have their advantages and disadvantages. For the MOS switch with the sense line, the fabrication technology is rather simple, but the MOS switch connects the small capacitance of the pixel to the relative large capacitance of the sense line. That is the reason why the signal-to-noise performance of this construction is rather poor. On the other hand, the technology for the CCD shift register is somewhat more complicated, and the transfer of the charge packet from the pixel towards the output diffusion needs appropriate clocking. However, the charge packet taken from the small pixel capacitance is transferred to the small capacitance of the output diffusion. This can result in a relatively high signal-to-noise performance for the construction of imagers with a CCD shift register as the charge transport medium.

Figure 2 shows only the combination of a metallurgical np-junction with the

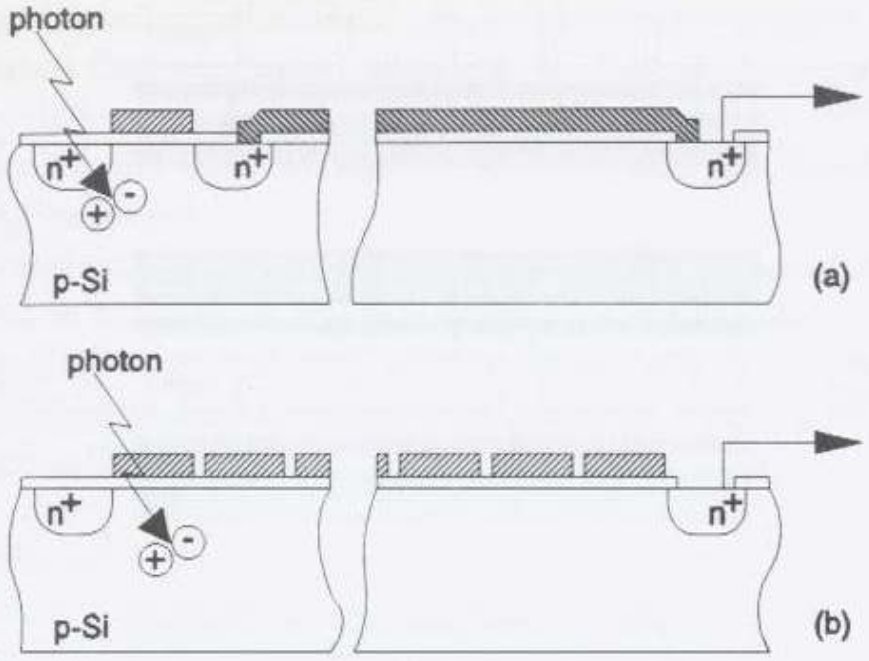


Fig. 2. Read-out structure to connect the photodiode to the outside world: *a*) an MOS switch; *b*) a CCD shift register.

alternative read-out schemes. Of course, an MOS capacitor can also be combined with a CCD shift register.

The conversion from a charge packet to a voltage at the output pin of the imager is done in a classical way: sensing of the voltage changes on a floating $n^+$-region by means of a source-follower. This is also illustrated in fig. 2.

## 3. Imager configurations

In the foregoing section, only the operation of a single imaging cell or pixel is explained. In practical applications, images can be built up in a one-dimensional way (e.g. facsimile) or in a two-dimensional configuration (e.g. home video or camcorders). In this section imager architectures will be discussed ranging for simple linear, bilinear, over quadrilinear to two-dimensional arrays: frame transfer, interline transfer and frame interline transfer.

### *3.1. Linear imagers*

The most simple organisation of pixels is a single line of photosensitive elements, photodiodes or MOS capacitors, as shown in the top illustration of fig. 3. Located next to the row of pixels is a CCD shift register needed for the read-out of the charge packets: the length of a CCD unit cell is equal to the pitch of the pixels. The isolation of the pixels from the CCD is done by means of a transfer gate (e.g. ref. 3). After the integration of charge carriers in the photosensitive elements, the transfer gate is set to a high voltage, the pixels are emptied into the CCD shift register in a way similar to normal parallel–serial

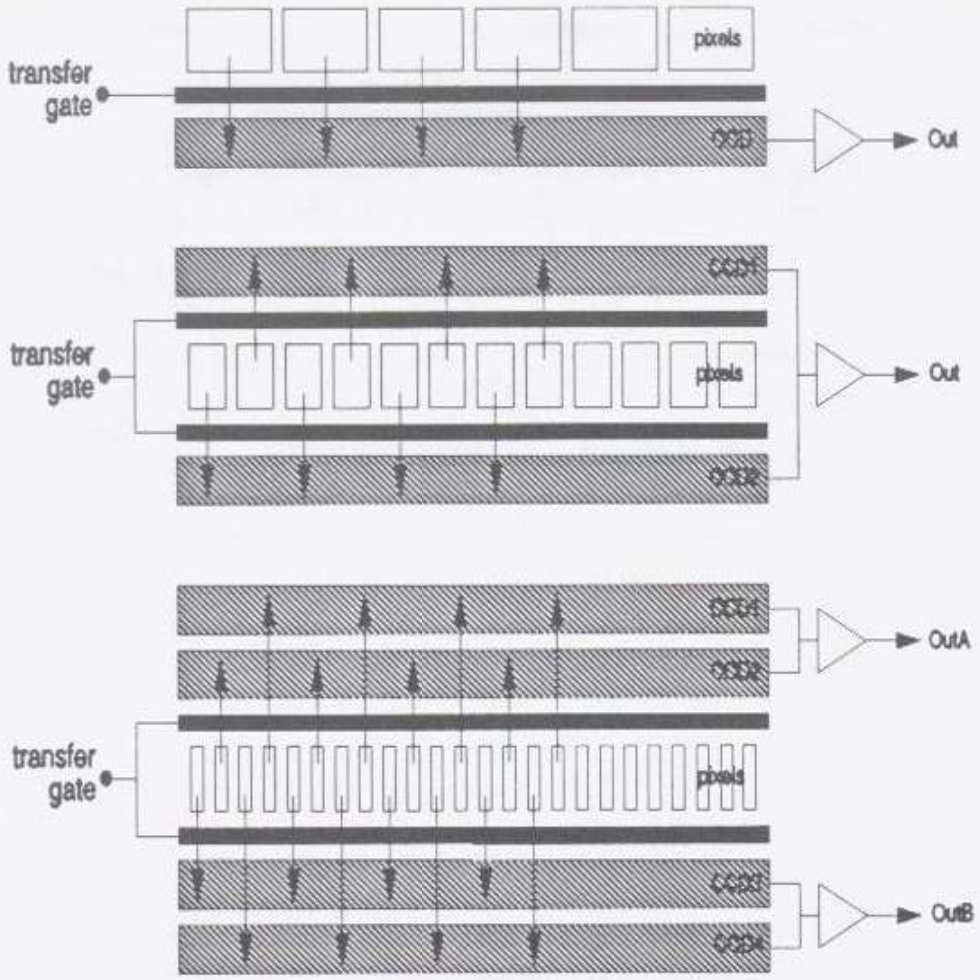


Fig. 3. Device concepts of the different types of linear image sensor: a simple linear structure (top), a bilinear imager (middle) and the quadrilinear concept (bottom).

CCD transport, and the transfer gate is set again to a low voltage. A new integration period can start, and in the meantime the charge packets can be transferred through the CCD shift register towards the output of the device. Note that the CCD shift register is shielded from the incoming light to avoid disturbance in the number of carriers in the charge packets.

If there is a need for a high-resolution imager with a higher number of pixels $mm^{-1}$, the length of the CCD unit cell can be a limitation, because it defines the smallest pixel pitch. In a bilinear imager (e.g. ref. 4) the pixel pitch can be decreased by a factor of 2 compared with a normal linear imager. As shown in the middle of fig. 3, a bilinear device makes use of two CCD shift registers, one on each side of the single row of pixels. The basic operation of a bilinear imager is identical to a simple linear one, except that the charge packets are spread out over two CCD registers after the integration. Odd pixels are, for instance, moved to the bottom CCD line, even pixels to the top CCD line. At the output stage of the device, the charge packets are multiplexed again in

such a way that the information at the output is a successive stream of samples in the same order as they were taken by the photosensitive elements.

Apart from the increased pixel density, the bilinear CCD, compared with its linear counterpart with the same number of pixels, also has the advantage of a lower clocking frequency.

The demultiplexing technique, characteristic of the bilinear imager, can be further applied to make a quadrilinear imager[5–7]); see the bottom illustration of fig. 3. Four CCD shift registers, on both sides of the pixel row, are used to transport the charge packets to a double-output structure (or even a single-output stage). A possible way of splitting the information in four CCDs is indicated in fig. 3 by the arrows. In this quadrilinear imager the pixel pitch is equal to one-quarter of the length of the CCD unit cell. If the partitioning across the different CCD registers is done in a suitable way, this configuration is well suited for high-resolution line-imagers: a total number of more than 5000 pixels on a single line is no longer an exception.

### *3.2. Area imagers*

In the case of two-dimensional solid-state imaging, several device architectures are possible, and not only limited to CCDs: XY-addressed photodiodes (MOS XY) and charge-injection devices can also be used. The CCDs themselves can be further subdivided into frame transfer imagers, interline transfer imagers and frame interline transfer devices. The basics of these different types will be described, and at the end of this section a comparison between the alternatives will be made.

#### *3.2.1. Frame transfer CCD*

Basically all frame transfer devices are built with MOS capacitors as sensing elements. However, all CCD cells are also composed of MOS capacitors, which opens the possibility of combining both functions in one structure: using a string of CCD cells or the CCD shift register as a linear solid-state imager. By placing several of these linear devices near each other, one can build a two-dimensional imaging array, as depicted in fig. 4. Each light-sensitive CCD register is extended by a CCD shift register of the same length. The latter CCD register is shielded from incoming light. These shielded CCD lines can act as a temporary memory for the information which is shifted into it, coming from the top light-sensitive lines.

The complete operation of a frame transfer device can be described as follows: in the light-sensitive top part of the device or image section, all CCD cells are biased in the integrating mode. Part of the CCD phases are connected

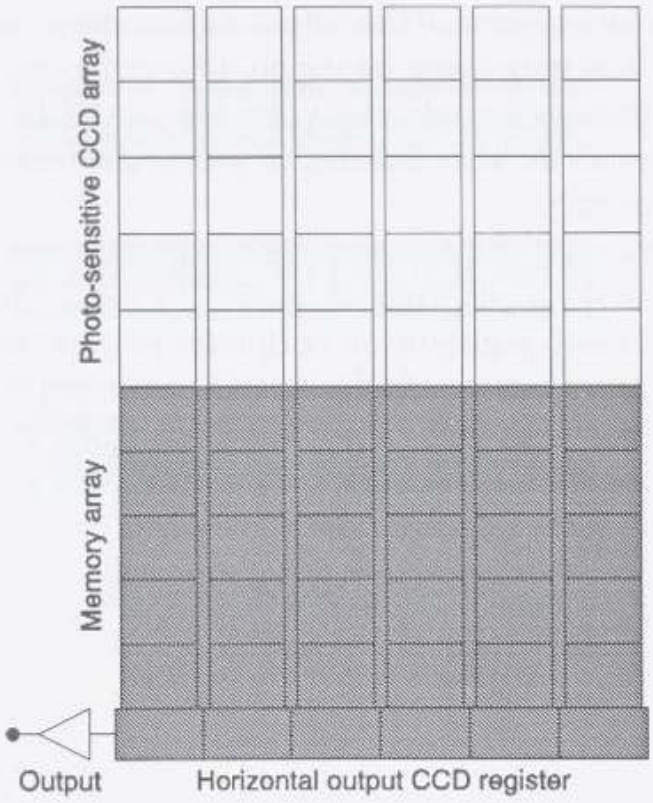


Fig. 4. Device architecture of a frame transfer image sensor.

to a high DC level, part of them to a low DC level. In this situation, charge generated by impinging photons is collected in the induced potential wells. At the end of a defined integration time, the CCD shift registers transfer their charge packets to the corresponding CCD lines in the light-insensitive memory or storage section. This transfer from image to storage area has to be done as quickly as possible to avoid disturbance of the information already available in the CCD shift registers of the imaging section by extra charge generation. Once the complete information of the image section has been transported to the storage section, the transport of the charge packets towards the output structure of the device can start. During this action, the charge packets located on a horizontal line (and belonging in this way to different vertical CCD shift registers) are transferred to a single horizontal output CCD register. This parallel–serial transfer is similar to that described for the linear imagers and used in the bilinear and quadrilinear configurations. Once the charge packets have been shifted in the horizontal output register, the final transfer to the output stage can take place, charge packets can be converted to an electrical voltage and the resulting video signal is available for further processing.

During the transport of all video information from the storage area to the output stage, the CCD cells of the image section are again biased in the integration mode, which allows the next image to be integrated. Note that in this way a

new image is built up in the image section while at the same time the previous one is being read-out from the storage area.

### 3.2.2. Interline transfer CCD

As for the frame transfer device, the two-dimensional interline transfer imager is also built up by placing several linear imagers near to each other. For the interline transfer device, the linear arrays used are of the type shown in fig. 3: the sensitive pixels are located near the shielded CCD transport register. The typical construction of the interline device is shown in fig. 5.

Its basic operation can be as follows: the integration of charge takes place in the pixels, which may be photodiodes or MOS capacitors. At the end of the integration time the charge packets are shifted from the pixels into the vertical CCD shift register near them. These shift registers are shielded from light and act as a memory for the information coming from the pixels.

After this transfer a new integration period can start and also the video information for the image just built up can begin to be shifted out. The vertical shift registers are emptied into the horizontal output register, line by line, in the same way as with the frame transfer device. The serial information in the horizontal output register is transferred to the output and consequently converted into an electrical voltage or current.

Again analogously to the frame transfer device, the interline transfer imager can integrate a new image during the storage of the previous one in its memory part, the vertical CCD shift registers.

### 3.2.3. Frame interline transfer CCD

The marriage between a frame transfer imager and an interline device is the

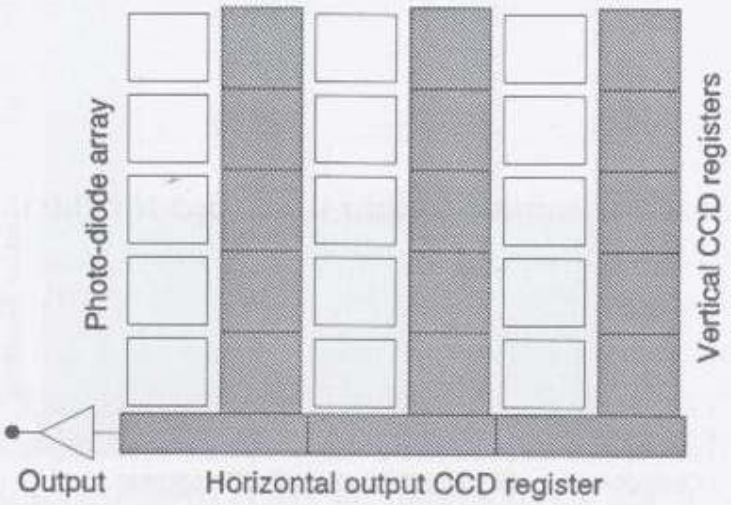


Fig. 5. Device architecture of an interline transfer imager.

frame interline transfer CCD: it has the light-sensitive area of the interline transfer device (photodiodes and vertical shift registers) combined with the storage area of the frame transfer device, as illustrated in fig. 6. Its basic operation is also a combined action of the two previous devices: integration of the charge packets in the pixels, transferring the charge packets in the vertical shift register, and then a fast vertical transport towards the shielded memory part of the imager. This vertical transport is not a line-by-line action, as in the interline transfer structure, but all the charge packets are moved as quickly as possible, as in the frame transfer structure. The vertical shift registers act only as an intermediate memory location and a transport channel between the pixels and the storage area. The conversion of the parallel information in the storage area to the serial information in the horizontal output register is analogous to that already described for the frame transfer and the interline transfer imagers.

### *3.2.4. Overview area imagers*

If different device architectures are compared with each other, it is important to start from a common base which in this section is an equal light-sensitive area[8,9]). Figures 4–6 are drawn in such a way that the imaging area of the frame transfer, interline transfer and frame interline transfer CCDs all have the same size.

Table 1 gives an overview of the pros and cons of the different device structures described.

From the comparison of figs 4 and 5 it is clear that the frame transfer imager

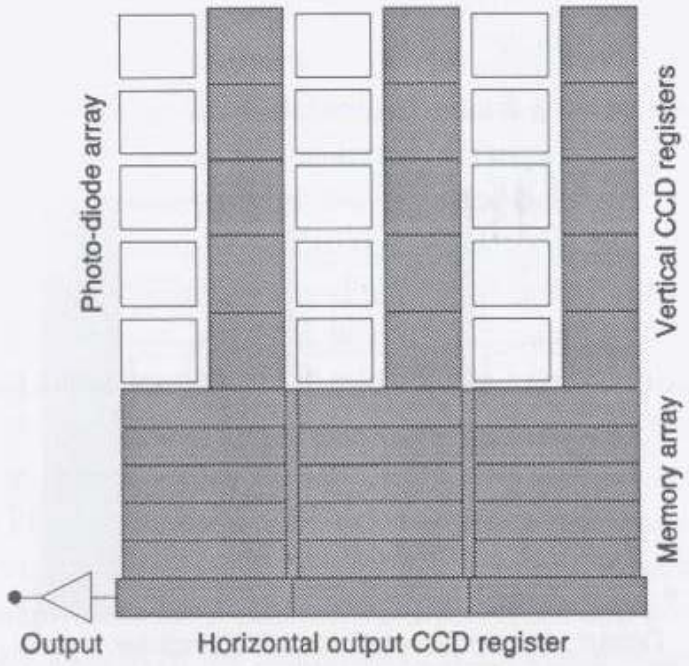


Fig. 6. Device architecture of a frame interline transfer imager.

Table I
Overview of advantages and disadvantages of the different types of two-dimensional imagers under study

| Device | Pros | Cons |
|---|---|---|
| Frame transfer CCD | Horizontal resolution<br>Aperture ratio<br>Shutter possibility<br>Simple technology | Chip size<br>Smear |
| Interline transfer CCD | Chip size<br>Complicated technology | Aperture ratio<br>Smear<br>Limited charge reset |
| Frame interline transfer CCD | Low smear<br>Complicated technology | Chip size<br>Aperture ratio |

has the largest chip size, because apart from its light-sensitive area it also contains a memory part. However, the complete area, which is defined as the imaging part of the frame transfer device, is light sensitive. This is not true for the interline transfer device: the image area also contains the vertical shift registers, which are light insensitive. This effect is translated in the aperture ratio, being the area of light-sensitive silicon divided by the total area of one CCD cell (equal to one pixel plus the area of one stage out of the vertical shift register). The interline transfer CCD has a small chip size but also a small aperture ratio, resulting in a lower optical sensitivity.

Typically for the frame transfer device and the interline transfer sensor there is a relatively high level of smear. To overcome this problem the frame interline transfer CCD was created, but it has the drawbacks of both the interline and the frame transfer devices: a low aperture ratio and a large chip.

## 4. Conclusion

In this article only a few aspect of CCDs and of solid-state imaging with CCDs have been discussed: the basic working principles of the charge-coupled imagers, the different architectures of the imagers, some features of image sensors dedicated to TV applications and some recent developments that increase the device's performance. The expansion of technology and the evolution of device physics have been so fast since the invention of the CCDs, that it has been impossible to cover all details of CCDs in this article. Moreover, research and development work involving CCD imagers is still going

on, and the fact that these efforts result in new ideas, new structures and new patents is shown by the technical and scientific conferences held yearly, e.g. the International Electron Devices Meetings, the International Solid-State Circuits Conferences and the Society of Photographic Institute and Engineers Conferences. More fundamental information concerning the subjects discussed in this article can be found in the proceedings of these meetings and conferences.

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