Groove-fill of tungsten and poly-Si membrane technology for high performance (HDTV) FT-CCD imagers

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Abstract

Key technologies necessary for the manufacturing of a HDTV Frame Transfer CCD sensor [1] are reported:
-a groove-fill titanium-tungsten/tungsten shunt wiring technology, directly resulting in a planar surface;
-non-overlapping poly-Si transfer gate method;
-very thin poly-Si gate-electrodes (membrane poly-gates technology).
With these technologies HDTV FT-CCD an image sensor with a high vertical frame-shift frequency of 2.5 MHz, a low on-chip power dissipation of 560 mW, and a high sensitivity in general (especially in blue), has been fabricated succesfully.

Introduction

In HDTV image sensors fast and optimal charge transport requires CCD gates with sufficiently low RC-values. Decreasing both the R- and C-values is necessary. To obtain small time constants, vertical shunt wiring structures of the poly-Si transfer gates in megapixel image sensors are inevitable. Aluminum and tungsten shunt wiring are already reported in FIT-CCD image sensors [2,3,4,5] using patterning and etching of the metal layers after definition of contact holes. For yield and performance reasons planarisation actions have to preceed the second metallisation.
In this paper a groove-fill with CVD tungsten is described that uses an existing poly-Si layer to act as **a buried etch-stop layer.** The groove etching automatically makes contacts to the transfer gates and diffusion areas. No planarisation is necessary for the second metallisation.
The overlap between the poly-Si transfer gates is traditionally designed to be very safe in order to obtain a good transfer efficiency. In this paper it is shown that considerably **less overlap** is possible by making optimal use of lithographic equipment with very high alignment accuracy. Consequently, much lower RC-values are possible.
In FT image sensors the sensitivity is mainly determined by the relatively thick poly-Si transfer gate and the relatively small uncovered areas (windows). To improve the sensitivity, in this paper a technology is proposed for replacing about 75% of the relatively thick poly-Si by very thin poly-Si **(membrane poly-Si).**

Groove-fill technology

The new filling technology of grooves allows grooves with strongly unequal depths. This in contradiction to the F(illed) I(nterconnect) G(roove) metallisation proposed by Broadbent et al [6], where the depth of the grooves is uniform. An initial planarisation with filled contact structures [7] to access underlying diffusion and poly-Si patterns is required before a planar dielectric layer is deposited. This layer has a thickness equal to that required by the tungsten interconnection.

This paper demonstrates a buried etch-stop layer that determines the bottom of the grooves during etching. Figure 1 shows a schematic cross-section along the length of a W-shunt. The processing sequence of an HDTV FT-CCD image sensor after patterning and oxidizing the first two layers of poly-Si transfer gates (needed for the vertical CCD-channels in the image and storage area) requires the addition of a third poly-Si gate structure in the 4-phase dual horizontal output register. However, in the image and storage area a smart use can be made of this third layer of poly-Si as a stopping layer during the etching of the grooves. By making small holes (1 μm diameter) and gaps (1 μm) in the stopping layer and by continuing the groove etching, the deeper situated poly-Si transfer gates and even mono-Si areas in the output amplifier can be reached and connected with the filling material TiW/W afterwards.
In Figure 2 a top view of the oxidized poly-Si transfer gates is shown in the image (a) and storage (b) section of the HDTV FT-CCD, with oxidized poly-Si stopping strips above the channel stop areas (holes (a) and gaps (b) in the stopping layer are visible). A deposition of a 1 μm thick dielectric, consisting of 0.5 μm TEOS and 0.5 μm BPSG follows. Because of good etch selectivity properties between the dielectric layer and silicon the next groove etching step is not critical. The groove-width is 0.9 μm, and the thickness of the stopping poly-Si layer is 0.3 μm. A sputter deposition

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of TiW and a blanket deposition of W by CVD with subsequent etch-back results in a sunken metallisation with a planar surface [7]. Due to the ultimate flat surface (BPSG flow), deposition and etching of the second metal layer (Al) is straightforward. Figure 3 shows SEM pictures of cross-sections perpendicular to and along the length of the W-shunts. After deprocessing (i.e. after etching oxide), SEM clearly shows the tungsten wires connecting to some lower poly-Si transfer gates and excellent isolation to other crossing gates (see Figure 4).
It should be emphasized, that if a third poly-Si layer is inevitable (due to the inclusion of a dual horizontal output register), only one mask step is needed for both contacting and defining the first metal to silicon (poly and mono). In this process, a 2.2 Mpixel FT-sensor [1] contains 30 m of tungsten wire (2000 lines each 15 mm long and 7.25 μm pitch). The design uses smallest dimensions of only 0.9 μm.

Non-overlapping transfer gates

After oxidation of the first poly-Si pattern, which defines two phases (ϕ1 and ϕ3) of the four-phase transfer system, the other two phases (ϕ2 and ϕ4) are defined by isotropic etching of a second poly-Si layer. Traditionally a clear overlap exists between the two poly-Si patterns. Optimal process control and lithographic steppers (ASML, type PAS2500) with high alignment accuracy allows tight production design rules. In Figure 2 and Figure 5 the non-overlapping of poly-Si transfer gates is shown. A reduction of the overlap capacitance by a factor three is possible. It is obvious that a more optimal topographical flatness is obtained as well.

Membrane poly-Si technology

The sensitivity in FT image sensors is mainly determined by the transparency of the transfer gates, made by relatively thick poly-Si (0.3 - 0.4 μm after oxidation), and the areas not covered by poly-Si (Figure 6a). Because the channel stop areas are barely light sensitive, the buried stopping layer and the groove-filled tungsten wires are situated above these areas.
To improve the sensitivity, the image pixel has been changed as shown in Figure 6b. About 75% of the original thick poly-Si area has been replaced by membrane poly-Si with a 0.05 μm thickness. Together with the definition of ϕ1 and ϕ3 in the first thick poly-Si layer, small square islands (2.0 x 2.0 μm) are defined above the channel stop areas. After oxidation of this poly-Si pattern, the oxide is stripped again from the small square islands to make contact to the second poly-Si layer (membrane poly-Si). To assure no gate-dielectric defects when contacting to membrane poly-Si with titanium-tungsten/tungsten wires, these small square islands of relatively thick poly-Si are necessary. After definition and oxidation of ϕ2 and ϕ4 in the membrane poly-Si, the stopping poly-Si layer structure can be made as described above. Sheet resistance of membrane poly-Si is 1 kΩ/□.
The improvement in sensitivity is considerable, as shown in Table I. Especially in blue the increase in quantum efficiency is almost a factor of 2.
Although the ratio between the sheet resistance of membrane poly-Si and thick poly-Si is about 40, no clock pulse shape distortion between ϕ1 (or ϕ3) and ϕ2 (or ϕ4) is present between two tungsten connection points. Consequently no transfer efficiency problems are observed.

Conclusions

Key technologies for manufacturing of high performance (HDTV) FT-CCD image sensors have been developed.
A high vertical frame-shift frequency of 2.5 MHz and a low on-chip power dissipation of 560 mW were obtained by using:

1) an optimized groove-fill of tungsten technology for shunt-wiring the poly-Si transfer gates. Essential for this is the introduction of a buried etch-stop layer during groove etching.
2) non-overlapping transfer gates, resulting in minimal interpoly capacity, and a smooth topography.

Membrane poly-Si gate layers were also fabricated, resulting in considerable improvement of the overall sensitivity in general and especially for the blue light.

Acknowledgement

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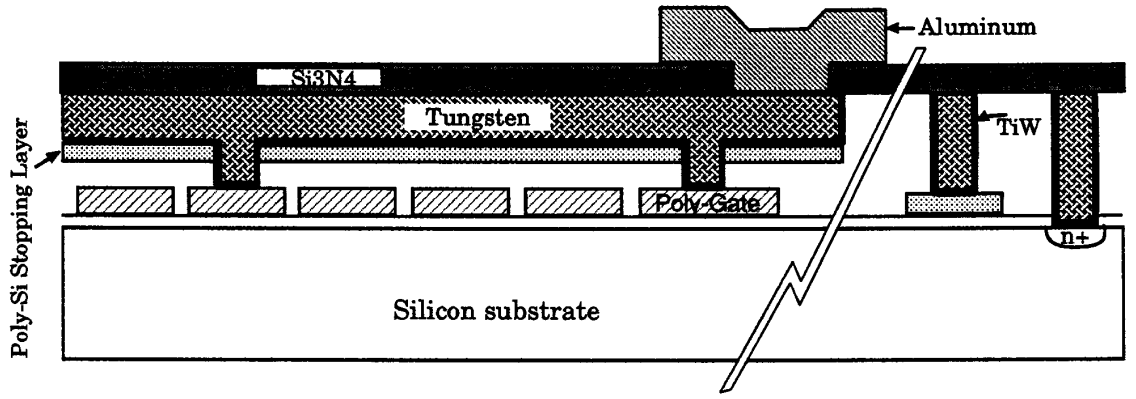

Fig. 1: Cross-sectional view of the groove-fill tungsten technology

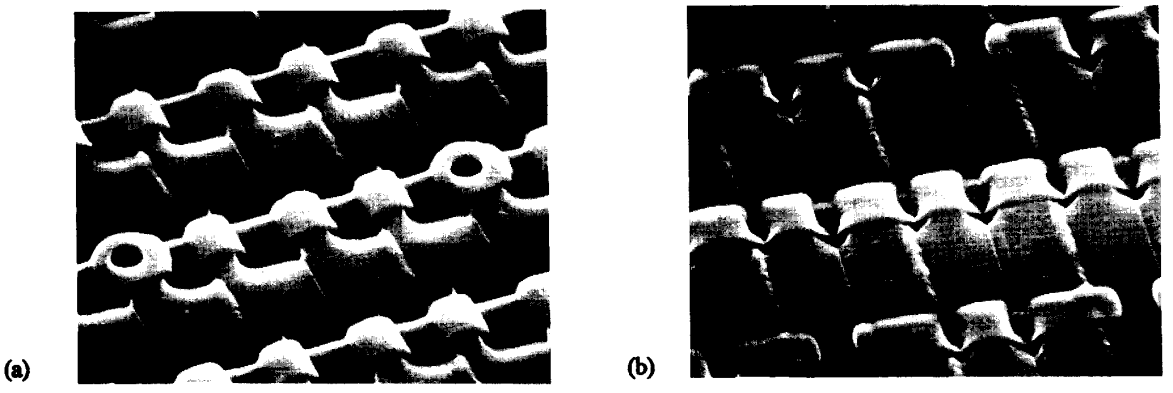

Fig. 2: CCD-channels with stopping layer patterns (third poly-Si layer) in:
a. the image area where contacts are made using holes in the stopping poly-Si
b. the storage area where contacts are made by gaps in the stopping layer

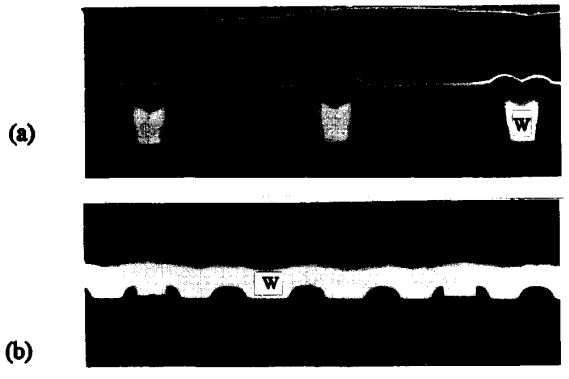

Fig. 3: SEM photographs of cross-sections in the image area
a. perpendicular to the W-shunts
b. along the length through the W-shunts

Fig. 4: SEM photograph of a deprocessed part of the storage area

Fig. 5: Non-overlapping gates in the storage area.

TABLE I
MEASURED QUANTUM EFFICIENCY (QE) WITHOUT AND WITH MEMBRANE POLY-SI

Design	Red (610 nm) QE [%]	Green (540 nm) QE [%]	Blue (450 nm) QE [%]
Conventional [1]	15	19	13
With membrane poly-Si	20	30	23
Ratio	1.36	1.57	1.80

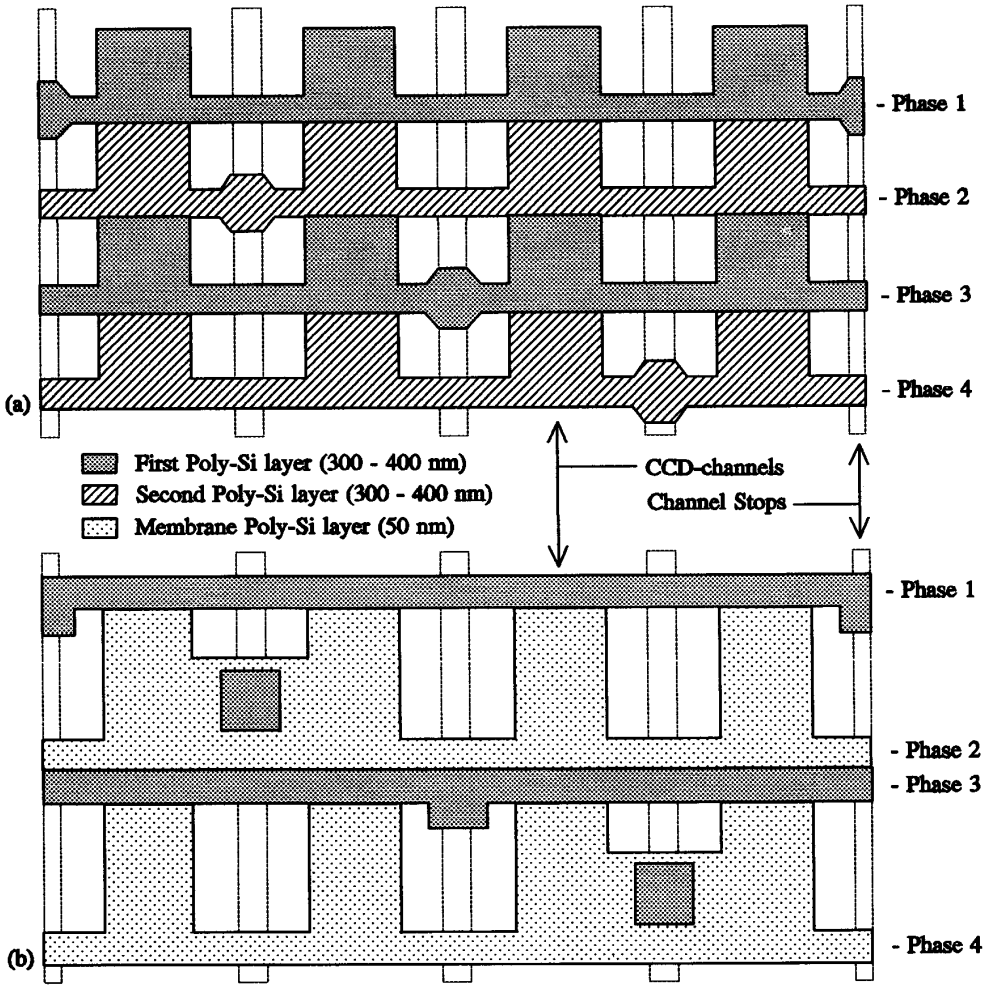

Fig. 6: Topview of 4 image pixels (W-shunt not drawn); pixel dimensions: 13.6 x 7.25 μm
a. Conventional design (ref.1) b. Design with membrane Poly-Si