A 2.2 M Pixel FT-CCD Imager According to the Eureka HDTV Standard

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***Abstract*—A very-high-performance HDTV image sensor is presented. The device tackles successfully a few typical "HDTV challenges": the very high *RC* values of the CCD gates are drastically lowered by means of a new interconnect scheme; a dual horizontal output register is used to lower the output rate; the device is provided with an output amplifier characterized by low noise, high bandwidth, and high conversion efficiency; and finally the imager is designed with a very compact and efficient image cell, providing the functions of photo-conversion, charge transport, highlight handling, charge resetting, and charge pumping.**

Compared to the competition, an imager with a high resolution, no smear when used in a professional camera, no image lag, simple charge-reset method or electronic shutter, and a high pixel uniformity with a fully linear response has been realized.

I. Introduction

IN THE last four years, several papers have been published dealing with HDTV image sensors [1]–[5]. These imagers were designed according to the 1125-line HDTV standard. However, they do not really fulfill completely the requirements put on the new generation of television systems. For instance, the interline HDTV imagers all have problems with smear [1], [5], the very sensitive PSID sensor with an amorphous top layer is characterized by a severe amount of image lag, burn-in effects, and pixel nonuniformity [2], the first FIT reported does not contain the full resolution of 1920 pixels/line [3]. Later FIT's with the full HDTV resolution need microlenses to increase their sensitivity and need a complicated charge-resetting method [4]. Although microlenses are favorable for sensitivity enhancement, they introduce a certain amount of nonlinear response, degrade the resolution of the imager, and cause some extra flare.

This paper describes the structure of the first HDTV imager which fits to the European HDTV standard, and is based on the frame-transfer principle. The device has an optical format of 1 in. If the imager is applied in a camera which is provided with a shutter, the overall system is fully free of smear. There is no need for microlenses. The imager presented has the full HDTV resolution and, as will be shown later, charge resetting can simply be done by biasing all CCD gates at a low voltage. Due to the high transfer efficiency of the vertical and horizontal CCD's of the frame-transfer imager, the video signal provided by this type of image sensor is fully free of lag.

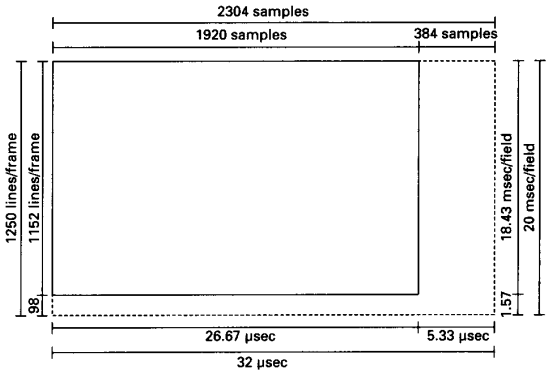

Fig. 1. Schematic illustration of the different parameters defined by the Eureka HDTV standard.

The digital Eureka HDTV standard to which the image sensor fits, is schematically shown in Fig. 1, and can be summarized as follows [6]: 1250 lines complete a frame of two subfields, each subfield has 576 active lines, each line has 1920 samples in an active line time of 26.67 μs. Horizontal and vertical blankings are 5.33 μs and 1.568 ms, respectively. The repetition rate of the subfields is 50 Hz and their aspect ratio is 16:9.

The device architecture of the imager reported here is shown in Fig. 2. The frame-transfer CCD has a four-phase image section, a four-phase storage section, and a four-phase, dual horizontal output register. The two output stages out_b and out_t feed the video information to the outside world.

The next two sections of this paper contain further details on the image cell (Section II) and the interconnect scheme of the CCD gates (Section III). In the definition phase of the HDTV-imager project, much effort was put into the design of the output amplifier. This will be de-

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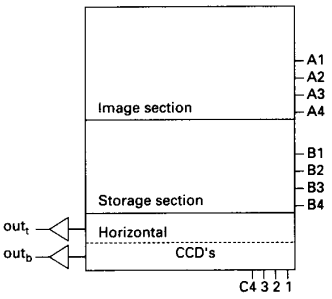

Fig. 2. Device architecture of the HDTV image sensor: a frame-transfer CCD with its image, storage, and horizontal output structure (all have four phases).

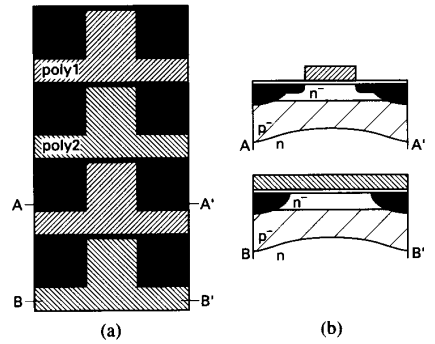

Fig. 3. Basic setup of the image cell. (a) Schematic top view of the image cell. (b) Two cross sections *AA'* and *BB'* (overlaps between the CCD gates are omitted for sake of simplicity).

scribed in Section IV. Some technology highlights will be summarized in Section V. The paper will conclude with the device parameters and characteristics.

II. Construction of the Image Cell

Although a frame-transfer CCD is characterized by a very simple image-cell construction, this cell has to fulfill several completely different functions. First of all, the image cell has to convert the incoming photons into a charge packet, this charge packet has to be transported (through the same image cells) with a very high transfer efficiency. Highlight handling has to be achieved inside the image cell by means of a high-performance anti-blooming construction. This construction can also be used to make the charge-reset action or electronic shutter effective. To lower the dark current in the image section, the doping profiles have to be chosen in such a way that charge pumping is possible. The image cell which has the capabilities to fulfill all the aforementioned functions is illustrated in Fig. 3. In Fig. 3(a), the top view of an image cell is shown; in Fig. 3(b), two cross sections illustrate the effects of the different implants in the silicon bulk.

As depicted in Fig. 3(a), the image cell is constructed by means of four gates, etched in two different polysilicon layers. This "four out of two" choice makes the image cell fully flicker-free from one field to the other if the device is driven in the interlaced mode. Every pixel is defined by a barrier gate made from poly-1 and the integration takes place under alternate poly-1 gate and the two poly-2 gates. This setup holds for both fields and eliminates field flicker. The cross sections show the outdiffusion of the p well into the n-type substrate. The sinusoidal diffusion profile is created by means of a lateral outdiffusion of two implants on both sides of the cell. The p^+ regions act as channel stoppers. Note that this channel stopper is extended to the polysilicon gates by means of self-aligned implant.

A. Optical Response

The main function of the image cell is to convert the incoming photons into electrons in an effective way. The frame-transfer pixel has a high aperture ratio, compared to IL or FIT pixel structures. This property is due to the "absence" of the opaque vertical shift registers which are inherent to the IL or FIT designs. But to optimize the optical response of the described image sensor even further, the following techniques are applied.

- The different thicknesses of the layers belonging to the multilayer stack above the silicon (scratch protection, isolation, poly-layer, gate dielectric) are chosen according to the optical rules for maximum transmission of the overall pixel structure.
- The gates have open windows [as can be seen from Fig. 3(a)], to make the sensor also very sensitive for blue light, otherwise the "blue photons" would be absorbed in the poly-Si gates.
- The voltage bias of the barrier gates (put to a low gate voltage during the integration of charges) is set to such a voltage that electrons generated by light below these gates do not drain to the n-type substrate.

Fig. 4 explains this last characteristic. It shows the simulated electrostatic potential diagram through the center of the pixel and in the direction perpendicular to the Si–SiO_2 interface into the bulk of the silicon. In the simulations the n-type substrate is biased to 15 V and the p well to 5 V. Curves 1 and 4 illustrate to the following situations.

- Curve 1 represents an empty well under a positive-biased gate during integration (V_G = 10 V). Electrons generated within the first 2.25 μm of the silicon will be collected in the potential well, charge generated deeper will disappear into the n-type substrate. All holes generated are drained by the p well and the p^+ stopper implants. Observe that the potential well is more positive than the n-type substrate bias, but the potential barrier in the p well avoids electron injection from the bulk into the channel.
- The barrier gates during the integration are biased at 2 V, as depicted by curve 4. Observe the small potential well underneath this gate, which is responsible for an active barrier gate: electrons generated underneath the barrier gate will be collected into neighboring potential wells. The small barrier towards the substrate prevents draining of these electrons. On the other hand, its collecting depth is reduced to 1.5 μm.

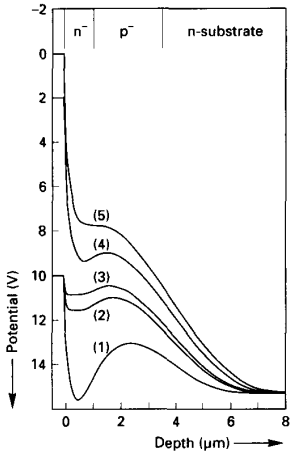

Fig. 4. Shown is the simulated electrostatic-potential diagram through the center of the pixel from Fig. 3 and in the direction perpendicular to the Si–SiO_2 interface into the bulk of the silicon (the different curves are explained in the text).

B. Vertical Anti-Blooming

The ability to handle highlights above the saturation level of the imager is incorporated in the vertical direction: into the bulk of the silicon. The vertical n-p-n structure goes into punchthrough at the moment the charge packet contains a full well of electrons. The same vertical n-p-n structure is used to drain all charges at the moment of charge reset. In Fig. 4, the vertical anti-blooming action is shown by curves 2 and 3.

- Curve 2 depicts the situation underneath the same gate as that for curve 1, but in this case the well is filled with electrons up to the level that the remaining barrier between the channel potential and the minimum potential in the p well is 0.6 V. This point is being defined as full well capacity. For the image cell under study [7.25 μm (H) × 13.6 μm (V)], the static full-well capacity under integrating conditions with three gates biased to 10 V is 220 000 electrons. Its dynamic storage capacity, during the transport underneath two gates, is limited to about 100 000 electrons (at a p-well bias of 5 V).
- In case the potential barrier between the CCD channel and the substrate reduces to 0.4 V, as shown by curve 3, the electron transport across this barrier has a value which corresponds to the overexposure conditions.

Notice that in all cases, there is at least a potential difference of 0.25 V between the channel potential and the potential at the Si–SiO_2 interface. With this restriction, the electrons from the charge packet will not interact with the interface states, and the CCD will maintain its high transport efficiency.

A barrier to neighboring pixels of at least 1.25 V is maintained to isolate two different charge packets from each other in the CCD channel. This barrier is defined as being the potential difference between the channel potential at full well and the potential underneath a negatively biased barrier gate.

C. Charge Reset

If all gates of the image cell are biased to 0 V, there will be no longer any potential well in the silicon, and no electrons can be stored. This situation, shown by curve 5 of Fig. 4, is created in the frame-transfer imager during charge reset, which is accomplished simply by biasing all gates of the image section to an extra low voltage, without any pulse on the n substrate or the p well.

D. Charge Pumping

In case the gates are biased to 0 V, as is the case during the charge-reset action, the surface potential is pinned to the p-well voltage. An inversion layer of holes, supplied by the channel implants, is created underneath the low-biased gates. These holes fill the surface states and reduce the dark-current generation. The conventional clock waveform diagram, needed to drive the frame-transfer imager, is completed with extra pulses to incorporate the charge-pumping option. During the horizontal-blanking period, all gates of the image section are one by one switched to 0 V and back to their original integration voltage. The occupancy state of the surface states is "refreshed with holes" during 1 μs. In the next active line period of 32 μs, the holes are released with a large time constant, keeping the surface states mainly filled. This charge pumping action reduces the dark current by 30%.

E. Transport Efficiency

The vertical and horizontal CCD's are all of the buried-channel type [see cross sections in Fig. 3(b)]. Special care has been taken to reduce the *RC* values of the CCD gates (see the next section).

III. Gate Interconnect

As already mentioned in the discussion of the image-cell configuration, a fast and optimal CCD transport needs CCD gates with a sufficiently low *RC* value. The classical interconnect scheme for the CCD gates of a two-dimensional imager is shown in Fig. 5(a). The vertical n-CCD channels are covered by means of horizontal polysilicon CCD gates. These CCD gates are connected to a four-phase bus-bar system defined around the image section, and made from a single, aluminum metallization level. Each single poly-Si gate has two connections, one at its left side and one at its right side. If this interconnect scheme is applied to the 1-in frame-transfer imager, the maximum frame-shift speed is limited to about 300 kHz. On the other hand, to fulfill the frame shift within the vertical-blanking period, a minimum vertical-transport speed of 700 kHz is required.

To overcome this problem, the HDTV image sensor has to be built in a new technological metallization concept to decrease the *RC* values of the CCD gates. This new concept is found in a new interconnect scheme, which is depicted in Fig. 5(b): the same CCD channels with the same CCD gates are still in place. This holds also for the

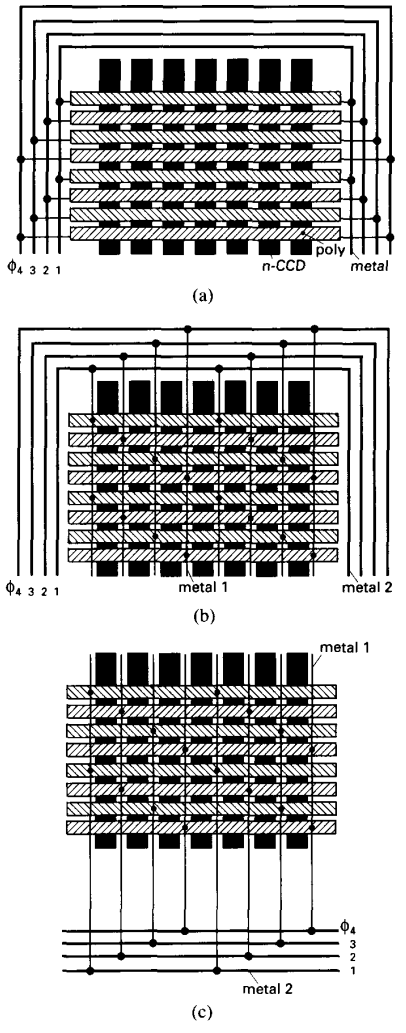

Fig. 5. Different interconnect schemes for the image section of a two-dimensional image sensor. (a) Conventional setup. (b) Lowering the *RC* values of the CCD gates by means of an additional metal layer. (c) Architecture used in the imager reported here.

metal bus-bars, only the interconnect between the polysilicon gates and the metal bus-bars has been changed. In the new concept, an additional (defined as metal 1) interconnect layer is used to bridge the large resistive values of the CCD gates. This metal 1 is defined in very small straps on top of the (light-insensitive) channel stopper implants. They contact every fourth gate, and strap all gates of the same phase. In the original architecture, 1920 pixels are defined between two polysilicon metal contacts; in the new architecture, only four pixels are between two contact points.

This idea can be exploited even further. The metal-1 straps are no longer connected to the bus-bars on top of the image section, but are fed into the storage section and are locally connected to the broad aluminum bus-bars. This ultimate construction is shown in Fig. 5(c). The net result is an imager with bus-bars, very short in length, far

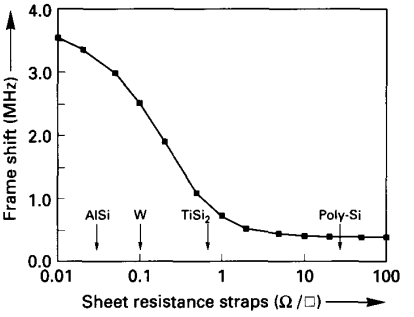

Fig. 6. Simulated frame-shift frequency as a function of the sheet resistance of the strapping material. (Straps of 0.9-μm width are simulated.)

away from the image section. In this way, unwanted reflections on the aluminum bus-bars, acting as mirrors (with 90% reflection) in case of Fig. 5(a) and (b), and resulting in artifacts in the displayed image, can be avoided.

The remaining question with respect to this new interconnect concept is the nature of the additional interconnect layer. The answer is shown in Fig. 6. Illustrated is the maximum frame-shift frequency (without degradation of the maximum charge-handling capability) as a function of the sheet resistance of the strapping material. With the lower limit of the vertical transport speed at 700 kHz, the use of $TiSi_2$ is at the limit, but W or AlSi are attractive alternatives. The implementation of an additional polysilicon level makes no sense with respect to lowering the *RC* value of the CCD gates. In the design of the image sensor described in this paper, the choice is made for straps of tungsten with a width of 0.9 μm. The upper limit of the 2.5-MHz vertical-transport speed suggested in Fig. 6 is experimentally verified. The saturation in the frame-shift frequency improvement for even lower sheet resistances is due to the resistance of the aluminum bus-bars.

The technology applied for this additional strapping step is summarized in Section V.

IV. Output Amplifier

The requirements put on the output stage are quite severe: high bandwidth, low noise, high conversion factor. This all is needed to provide the outside world with video information at a 72-MHz pixel rate. To bring this operating frequency to a lower value, the horizontal output register of the imager is designed as a dual horizontal structure. This technique is well known for HDTV imagers, but special attention has to be paid to the layout of the dual register and their "mutual interconnect" to avoid transport inefficiency between the two horizontal registers. The optimizing process used in the 1-in frame-transfer device is the same as described in [8].

The two horizontal output registers are each provided with a high-sensitivity, low-noise, and high-bandwidth output amplifier [9], built around a triple source-follower stage. Such an output-node construction is shown in Fig.

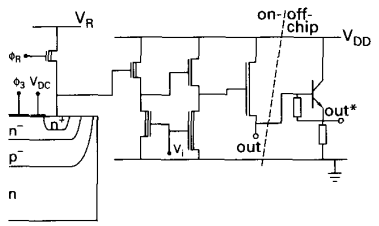

Fig. 7. Construction of the charge-sense node. From left to right: the floating diffusion of the CCD (n^+) with its reset transistor, the triple source-follower amplifier, and the external load (designed as a current source).

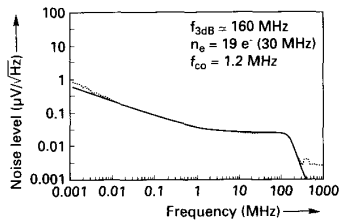

Fig. 8. Measured (points) noise performance of the output amplifier as a function of signal frequency. The line represents a model calculation.

7. Included is the floating diffusion of a horizontal output register (n^+), diffused near the dc-biased output gate (V_{DC}) and the last clocking gate (Φ_3). Resetting is done by means of a deep-depletion MOS transistor, diffused in the same n channel as the buried CCD channels. The triple source-follower stages have two on-chip loads. Only the first driver is a deep-depletion MOS transistor to lower the $1/f$ noise of the overall output stage. The two other drivers are of the enhancement type. To keep the power dissipation as low as possible, the load of the last stage is defined off-chip. All depletion-type MOS transistors have non-self-aligned source and drain implants. This provides the transistors with a kind of graded-drain construction. In the meantime, overlap capacitances are reduced as far as possible. The enhancement-type MOS transistors all have self-aligned sources and drains. Any offset between these implants and the gates will result in a high series resistance (of the p-type region) on the source and drain sides.

Noise figures measured on an output amplifier of the type as described here are shown in Fig. 8: noise levels versus frequency. From these measurements the following numbers can be deduced: bandwidth is about 160 MHz, the equivalent number of noise electrons rms is 19 in a 30 MHz band after signal processing, and the cross-over frequency f_{co} between $1/f$ noise and thermal noise is 1.2 MHz. These numbers prove the applicability of this amplifier concept and layout to a HDTV imager.

An interesting optimizing problem can be defined around the floating-diffusion node. To make the floating-diffusion capacitance as small as possible (to increase the conversion efficiency) a layout concept, as shown in Fig. 9(a), is used: the very small area of the floating diffusion is surrounded at three sides by the output gate. This two-dimensional layout—where electrons come from three sides to the floating diffusion—is reshaped to a one-dimensional horizontal output register—where electrons are transported in only one direction—in a few steps in the design of the last gates of the horizontal CCD register. With this concept the layout can be made as compact as possible, but on the other hand there is a lower limit for the area of each gate. The last Φ_3 gate has to store a full packet, but also has to transport a full packet. The requirement of storing gives a minimum length of the gate, the requirement of transporting defines the maximum length of the same gate. To overcome this problem, a two-

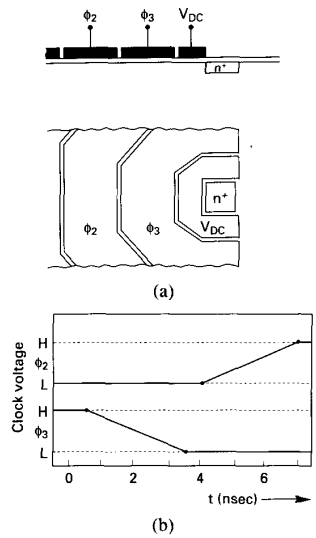

Fig. 9. Layout concept (a) and timing diagram (b) during the charge transport from the last clocking Φ_3 across the output gate towards the floating diffusion (overlaps between the CCD gates are omitted for sake of simplicity).

dimensional dynamic device simulator CURRY [10] which has been developed in-house, is applied to the output-node configuration. The charge transport is simulated at the moment a full well is transferred from the Φ_3 gate across the output gate towards the floating diffusion. The timing corresponding to this situation is shown in Fig. 9(b).

The results from these dynamic simulations are illustrated in Fig. 10(a) and (b). Fig. 10(a) contains the situation in which the length of the Φ_3 is 8 μm, which will lead to an incomplete charge transfer. In the starting situation, the full-well charge packet is stored underneath Φ_3, and, as can be deduced from the timing diagram in Fig. 9, the gate Φ_2 is biased low. At $t = 0.5$ ns, Φ_3 starts going low, and this point is the onset of the transport of the charge packet. At $t = 1$ ns, the first electrons are attracted by the floating diffusion. Observe that the transfer itself takes place through the bulk of the silicon. At $t = 1.5$ ns, the first charges reach the floating-diffusion node. During the further timing points, the transport continues, but at time $t = 3.5$ ns Φ_3 is low, and at $t = 4$ ns Φ_2 starts increasing. At this moment ($t = 4$ ns), the next charge packet is coming towards Φ_2, and at the same time, Φ_2 is

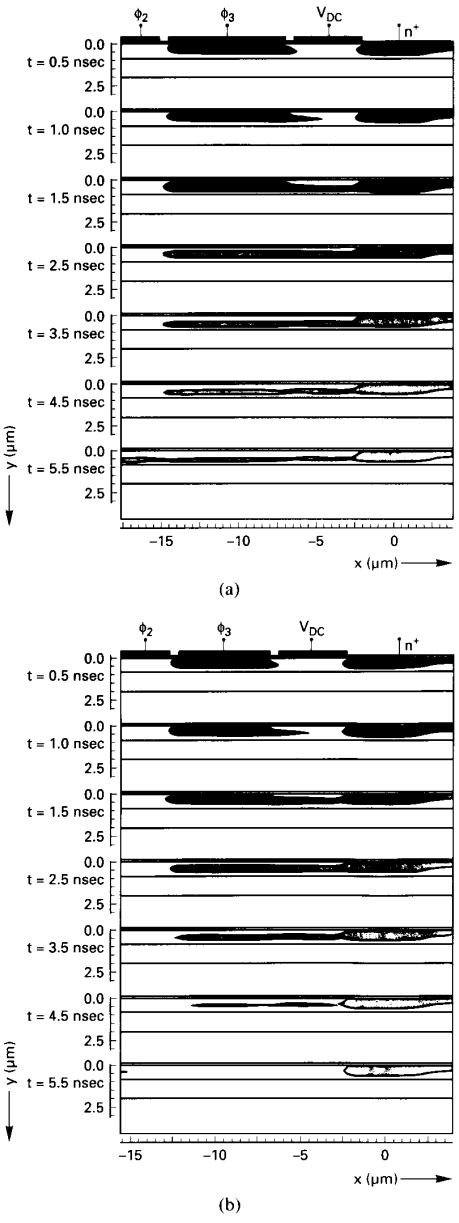

Fig. 10. Results of the dynamic two-dimensional device simulations of the transport of a full-well charge packet towards the floating diffusion. The gate length of the Φ_3-gate is (a) 8 μm in the first simulation results and (b) 6 μm in the second.

attracting remaining electrons from Φ_3. This can be seen at time point $t = 5.5$ ns: there is a continuous electron flow from Φ_2 towards the floating-diffusion node. Charge packets are mixing up, a[illegible] the transport deteriorates the resolution of the devic

In the case the gate length of Φ_3 is 6 μm, shown in Fig. 10(b), and under the same timing conditions, the result is much better. Though the transport is not fully completed at $t = 4.5$ ns, the amount of charges flowing back under Φ_2 is relatively small: less than 0.3%. This transfer inefficiency is tolerable due to the fact that it affects the charge packets only once in its complete transfer trajectory. From this conclusion and from Fig. 10(a) the gate lengths of Φ_3 and Φ_2 are chosen to be, respectively, 6 and 8 μm.

The simulations of the charge transport through the horizontal output registers are all done with clock amplitudes of 5 V. Limiting the voltage swing to this voltage is attractive from the point of view of power dissipation and of driver design. Direct coupling of the horizontal CCD register to CMOS drivers connected to a low-voltage power supply is preferable.

V. Technology

The device technology used to fabricate the HDTV image sensors is based on the technology already described in [12] and [13]. Summarized: n-type buried CCD channels are defined in a single implanted p well. As already stated, the sinusoidal shape of the profile is defined by an appropriate outdiffusion of the B implant. The gate dielectric is a sandwich of SiO_2 (62 nm) and Si_3N_4 (78 nm), three layers of polysilicon define the CCD gates (two layers in the image and storage section, three layers in the horizontal output registers). After the gate definition, all remaining implantations are done and isolation layers are deposited. The tungsten interconnect, the aluminum metallization, and the scratch protection complete the fabrication process. The minimum dimensions used in the layout are 0.9 μm, and the total number of masks needed is 13.

Compared to the "standard" processing as described in [12] and [13], the tungsten interconnect is added. To minimize the negative influence on the light sensitivity from the W straps, the width of the W straps should be as small as possible. This requirement can be achieved by a groove-fill technique [14]. The processing sequence of the W process is illustrated in Fig. 11: after the processing of the polysilicon layers, a planar dielectric is deposited, with a thickness of about 1 μm. The W-interconnect pattern is defined in this dielectric in the form of grooves. The grooves are 0.9 μm wide. Next is a blanket tungsten deposition, followed by a very well controlled tungsten etchback. The net result is an interconnect network of grooves filled by tungsten. This processing method allows to keep the W straps quite small compared to the stopper implantation width after outdiffusion. In other words, the incorporation of the straps has very little effect on the light sensitivity of the imager.

VI. Device Parameters and Characteristics

In Table I, the device parameters and device characteristics are summarized. A microphotograph of the chip is shown in Fig. 12. This device is the key component of a three-chip professional HDTV camera. A monitor photograph of a picture taken by the HDTV camera is shown

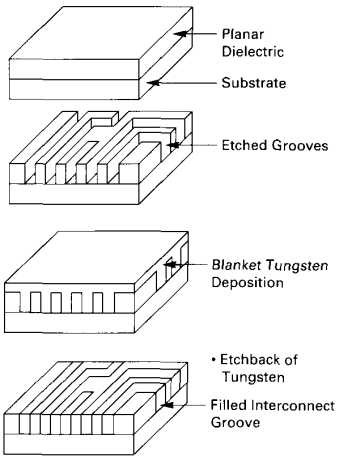

Fig. 11. Processing sequence of the W interconnect: from top to bottom, the dielectric deposition, the groove definition, the W deposition, and finally the W etchback.

TABLE I
DEVICE PARAMETERS AND CHARACTERISTICS MEASURED WITH THE p-WELL BIASED AT 5 V

Parameter	Value
HDTV standard	Eureka
Aspect ratio	16:9
Interlacing	2:1
Fields/s	50
CCD type	frame transfer
Optical format	1 in
Image diagonal	16 mm
Image section (H × V)	13.92 mm × 7.83 mm
Number of active lines	1152
Number of active pixels/line	1920
Pixel dimensions (H × V)	7.25 μm × 13.6 μm
Chip dimensions (H × V)	15.37 mm × 15.57 mm
Chip area	239 mm^2
Number of output registers	2
Pixel output rate	72 MHz
Frequency of horizontal clocks	36 MHz
Horizontal clock swing	5 V
Frequency of vertical clocks	1.125 MHz
Vertical clock swing	8 V
Sensitivity at output pin	6.5 μV/e$^-$
Amplifier gain	0.6
Number of noise electrons	19
Bandwidth of output stage	160 MHz
Quantum efficiency	20%
Overexposure capacity	10^4 ×
Full well capacity	10^5 e$^-$
Dynamic range	74 dB
Horizontal resolution	1000 TV lines
Image lag	none
Smear (in the camera)	none

in Fig. 13. The HDTV camera has a shutter included in its optical system. This shutter cuts the light path during the vertical frame shift of the frame-transfer CCD. In this way, the application of the HDTV imagers is made fully smear-free.

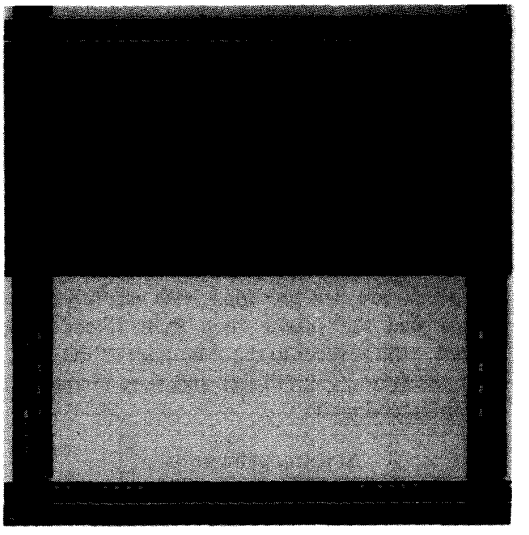

Fig. 12. Microphotograph of the HDTV imager.

Fig. 13. Monitor photograph of a picture taken with a professional HDTV camera including three HDTV image sensors.

VII. CONCLUSIONS

The 2.2 M pixel frame-transfer CCD described in this paper has successfully tackled the following challenges:

- the *RC* values of the CCD gates are lowered considerably by means of the new interconnect scheme making use of the incorporated W technology;
- the high output rate is halved by using a dual horizontal output register;
- the device is provided with an output stage characterized by low noise, a high bandwidth, and a high conversion factor;
- the imager has a compact and efficient image cell functioning as photo-convertor, transporting cell, highlight handler, charge-resetting, and charge-pumping site.

The imager presented combines a few attractive elements which are additionally compared to the competition:

- 1920 pixels/line give the device the full HDTV resolution of 1000 TV lines;
- in the application, the device is running fully smear-free;
- due to its architecture and its technology, the imager is fully image-lag- and burn-in-free, the pixels are characterized by high uniformity;
- charge reset to shorten the integration time can be applied very easily: simply biasing all gates of the image section to a low potential;
- the pixels are not provided with microlenses (this means that the pixels keep their linear photoresponse, with respect to the F number of the lens, and their resolution capabilities and flare characteristics remain unchanged).

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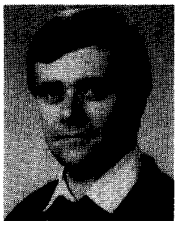
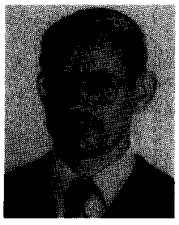


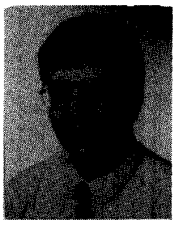
Albert J. P. Theuwissen (S'80–M'83) was born in Maaseik, Belgium, on December 20, 1954. He received the degree in electrical engineering from the Catholic University of Leuven, Belgium, in 1977, and the Ph.D. degree in electrical engineering from the ESAT Laboratory of the Catholic University of Leuven.

From 1977 to 1983, his work at the ESAT Laboratory focused on transparent conductive-gate electrode technology for linear CCD image sensors. In 1983, he joined the Micro-Circuits Division of the Philips Research Laboratories in Eindhoven, The Netherlands, as a member of the scientific staff. His work involved the design and development of new device structures and concepts for solid-state image sensors. In 1988 he became Project Leader of the HDTV-image-sensor project, and since 1991 he has been managing the Micro-Circuits Division, including the solid-state imager activities.



Herman L. Peek was born in Haalderen, The Netherlands, on June 25, 1942. He received the Ingenieur diploma degree in physics from Eindhoven Technical College, Eindhoven, The Netherlands, in 1969.

He joined the Semiconductor Research Group of Philips Research Laboratories, Eindhoven, in 1964, where he worked on MOS technology, silicon epitaxy, and silicon vidicon devices. Since 1973, he has been working in the CCD research group, where he has been responsible for the development of the frame-transfer solid-state image-sensor technology. From 1979 to 1983, he also worked on the development of EEPROM technology.



Martien J. H. van de Steeg was born in Wanroij, The Netherlands, on December 27, 1952. He received the M.S. and Ph.D. degrees in 1976 and 1982, respectively, from the University of Nijmegen, The Netherlands. His doctoral work concerned Fourier transform spectroscopy and its application to electrons and holes in high-purity germanium.

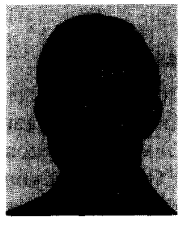
In 1982, he joined the Micro-Circuits Division of the Philips Research Laboratories, Eindhoven, The Netherlands, as a member of the scientific staff. He was involved in the design, electrical and theoretical characterization of solid-state image sensors. From 1988 till 1991 he worked at Philips RHW, Hamburg, Germany, as Manager of the product and test development in the pilot factory of solid-state image sensors. In 1991 he returned to the Micro-Circuits Division in Eindhoven as Project Leader of CCD imagers for HDTV applications.

Rob M. G. Boesten was born in Nuth, The Netherlands, in 1961. He received the B.Sc. degree in physics in 1984 from the Technical College of Eindhoven.

He joined the Technical University of Delft in 1985 where he worked on the magnetoresistance effect of small aluminum structures at superconducting temperatures. In 1986 he joined the Philips Research Laboratories, Eindhoven, where he initially worked in the field of very high-speed CCD's. In 1987 he started working on device simulations of CCD's for image-sensor applications. Now he is also working on quality and reliability of image sensors.

Peter B. Hartog was born in Arnhem, The Netherlands, on November 17, 1958. He received the Ingenieur Diploma degree in chemistry from Technical College, Hengelo, The Netherlands, in 1982.

After military service, he joined the Philips CMOS Research Group of Philips Research Laboratories, Eindhoven, in 1984, where he worked on CCD video memories and submicrometer lithography. Since 1988, he has been working on yield of solid-state image sensors.

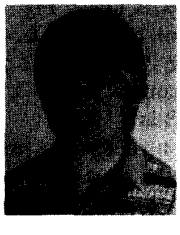


Andre L. Kokshoorn was born in Den Haag, The Netherlands, on September 22, 1961.

In 1984, he joined the Micro-Circuits Division at Philips Research Laboratories, Eindhoven, The Netherlands, where he is currently working on the development of solid-state image-sensor technology.

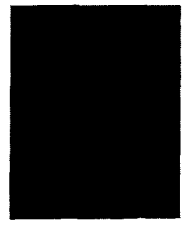
Eelco A. de Koning was born in Geldrop, The Netherlands, on August 22, 1961. He received the Ingenieur Diploma degree in electronics from 's Hertogenbosch Technical College, 's Hertogenbosch, The Netherlands, in 1986.

He joined the Philips Research Laboratories in Eindhoven, The Netherlands, in 1986, in the Automation Department. In 1989, he joined the Institute for Perception Research IPO (a cooperation of Philips Research and the Technical University of Eindhoven). Since 1990, he has worked in the CCD research group, where he is currently working on image sensors for HDTV.



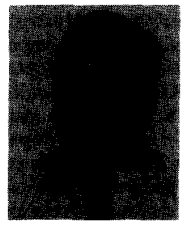
Jac M. A. M. Oppers was born in Oirschot, The Netherlands, on June 7, 1958. He received the Ingenieur Diploma degree in electronics from Eindhoven Technical College, Eindhoven, The Netherlands, in 1980.

After military service, he joined the Micro-Circuits Group at Philips Research Laboratories, Eindhoven, in 1981, where he is currently working on computer-aided testing of solid-state image sensors of the Philips Imaging Technology and the CCD Research Group.



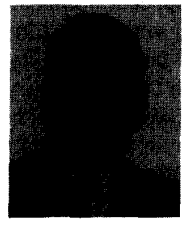
Frans F. Vledder was born in The Netherlands on September 5, 1964. In 1987 he received the B.Sc. degree in electronics from the Technical College in Leeuwarden, The Netherlands.

After serving in the Royal Dutch Navy, in 1989, he joined the Philips Research Laboratories in Eindhoven, The Netherlands, where he has been working in the CCD research group. In the first year he investigated an electronic smear compensation. Since 1990 he has been working on image sensors for HDTV, where he is responsible for the camera electronics.



Peter G. M. Centen was born in Goirle, The Netherlands, on October 19, 1952. He received the Masters degree (cum laude) in electronics from the Technical University of Eindhoven (TUE), The Netherlands.

At the end of 1983 he became an Assistant Researcher at the TUE and worked on a Variational Principle for the Equilibrium Conditions for a Magneto-Hydro-Dynamic Plasma. Late in 1984 he joined Broadcast Television Systems (BTS) a joint company of Philips and Bosch in Breda, The Netherlands. He carried out research on optimal signal processing for CCD sensors. After some time he became Guest Researcher at the Philips Research Laboratories in Eindhoven, where he devoted his attention to noise reduction of the CCD image-sensor output circuitry. His current interest includes a broad-band low-noise on-chip amplifier for High-Definition Television CCD image sensors.



Henk Blom was born in The Netherlands on September 22, 1936. He received the degree in electronics from the Delft Technical University in 1966.

He joined the Philips development department of professional audio recording and switched, in 1968, to the development department of broadcast video processing and transmission circuits and evaluation of pick-up tube performance. Since 1986 he has been with Broadcast Television Systems, a joint company of Philips and Bosch, Breda, The Netherlands, responsible for solid-state image-sensor applications in broadcast and HDTV color cameras.

Wim Haar was born in Hoogeveen, The Netherlands, in 1966. He received the B.C. degree in electrical engineering from the Technical College in Hilversum in 1989.

In 1990 he worked for four months at the University of Amsterdam. In June 1990 he joined the Broadcast Television Systems, Breda, The Netherlands, research and development department, where he is working on CCD's.