**HDTV IMAGE SENSOR : the pixel structure.**

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## ABSTRACT.

A very high performance HDTV image sensor is presented. The device tackles successfully a few typical "HDTV-challenges" : the very high RC-values of the CCD-gates is drastically reduced by means of a new interconnect scheme, a dual horizontal output register is used to lower the output rate, the device is provided with an output amplifier characterised by low noise, high bandwidth and high conversion efficiency, and finally the imager is designed with a very compact and efficient image cell, providing the functions of photo-conversion, charge transport, highlight handling and charge reset site.

Compared to the competition, an imager with a high resolution, no smear when used in the appropriate application, no image lag, simple charge reset method and a high pixel uniformity with a fully linear response is realised.

## 1. INTRODUCTION.

In the last four years, several papers were published dealing with HDTV image sensors [1-5]. All came from Japan, and all data described was applicable to devices suited for the 1125-lines standard. On the other hand, the imagers from these references do not really fulfil completely the requirements put on the new generation of television systems. For instance, the interline HDTV-imagers all have problems with smear [1] [5], the very sensitive PSID-sensor with an amorphous top-layer is characterised by a severe amount of image lag and pixel non-uniformity [2], the first FIT reported does not contain the full resolution of 1920 pixels/line. Later FIT's with the full HDTV-resolution need micro-lenses to increase their sensitivity and need a complicated charge resetting method [4].

This paper describes the pixel structure of the first HDTV-imager which fits to the European HDTV-standard, and is based on the frame transfer principle. The device has an optical format of 1". If the imager is applied in its appropriate application, the overall system can be made fully smear free. There is no need for micro-lenses, so there will be no deterioration of linearity and resolution due to these micro-lenses. The imager presented has the full HDTV-resolution and as will be shown later, charge resetting can be done in a very simple way. As known for the frame transfer CCD, its video performance is completely lag free.

The TV-standard to which the image sensor fits can be summarised as follows : 1250 lines complete a frame of 2 sub-fields, each sub-field has 576 active lines, each line has 1920 pixels in an active line time of 26.67 $\mu$sec. Horizontal and vertical blankings are 5.33 $\mu$sec and 0.785 msec respectively. The repetition rate of the different sub-fields is 50 Hz and their aspect ratio 16:9.

The device architecture of the imager reported here is shown in Figure 1. The frame transfer CCD has a 4 phase image area, a 4 phase storage area and a 4 phase, dual horizontal output register. The two output stages $out_b$ and $out_t$ feed the video information to the outside world [6].

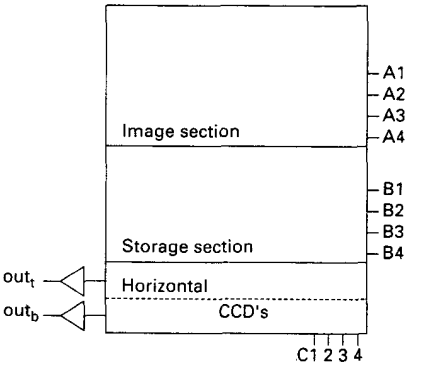


Figure 1 : Device architecture of the HDTV image sensor : a frame transfer CCD with its image, storage and horizontal output structure, all 4 phases.

## 2. IMAGE CELL CONSTRUCTION.

Although a frame transfer CCD is characterised by a very simple image cell construction, the unit cell has to fulfil several completely different functions. First of all the image cell has to convert the incoming photons into a charge packet, this charge packet has to be transported (through the same image cells) with a very high transport efficiency. Highlight handling has to take place inside the image cell by means of a proper anti-blooming construction. This construction can also be used to make the charge reset action effective. The image cell which has the capabilities to fulfil all the aforementioned functions is illustrated in Figure 2. In Figure 2a a top view of a unit cell is shown, in Figure 2b two cross sections illustrate the effects of the different implants in the silicon bulk.

As depicted in Figure 2a, the image cell is constructed by means of 4 gates, etched in two different poly-silicon layers. This "4 out of 2" choice makes the unit cell fully flicker free from one field to the other. Every pixel is defined by a barrier gate made from poly 1 and the integration takes place under the remaining gate from poly 1 and the 2 gates from poly 2. This set-up holds for both fields and eliminates field flicker. The cross-sections show the way the p-well out-diffuses into the n-type substrate. The sinusoidal diffusion profile is created by means of a lateral out-diffusion of two implants on both sides of the cell. The $p^+$-regions act as channel stoppers. Remark that this channel stopper is extended to the poly-silicon gates by means of a self-aligned implant.

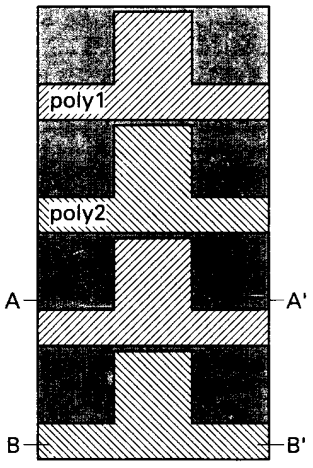


Figure 2a : Basic set-up of the image cell : top view of the unit cell.

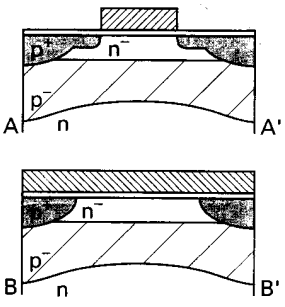


Figure 2b : Basic set-up of the image cell : cross sections AA' and BB' corresponding to Figure 2a.

The first function of the image cell is to convert the incoming photons into electrons in an effective way. The frame transfer pixel has an high aperture ratio, compared to IL or FIT pixel structures, due to the "absence" of the vertical shift registers. To further optimize the optical response,

- the multi-layer stack (scratch protection, isolation, poly-layer, gate dielectric) is chosen according the optical characteristics of the device,
- the gates have open windows (as can be seen from Figure 2a) to make the sensor as sensitive as possible also to blue light, otherwise the "blue photons" will be absorbed in the poly-Si gates,
- the voltage bias of the barrier gates (put to a low gate voltage during the integration of charges) is set to such a voltage that also these barrier gates are active during the charge integration periods.

As far as the charge transport through the image cells is concerned, the transport channels are all of the buried type (see cross sections on Figure 2b). Besides this, special care is taken to reduce the RC-values of the CCD-gates (see next section).

The ability for highlight handling is incorporated in the vertical direction : into the bulk of the silicon. The vertical npn-structure goes into punch-through at the moment the charge packet contains a full well of electrons. The same vertical npn-structure is used to drain all charges at the moment of charge reset. To explain this action, Figure 3 is included. It shows the simulated electrostatic potential diagram through the center of the pixel and in the direction perpendicular to the Si-$SiO_2$ interface into the bulk of the silicon. In the simulations the n-type substrate is biased to 15 V and the p-well to 5 V. The different curves belong to the following situations :

- curve (1) represents an empty well under a positively biased gate during integration ($V_G$ = 10 V). Electrons generated in the first 2.25 $\mu$m of the silicon will be collected in the potential well, charge generated deeper will disappear into the n-type substrate. All holes generated are drained by the p-well and the $p_+$-stopper implants. Remark that the potential well is "deeper" than the n-substrate bias, but the potential barrier in the p-well avoids electron injection from the bulk into the channel.
- curve (2) is the situation underneath the same gate as for curve (1), but in this case the well is filled with electrons up to the level that the remaining barrier between the channel potential and the minimum potential in the p-well is 0.6 V. This point is being defined as full well capacity. For the image cell under study (7.25 $\mu$m (H) x 13.6 $\mu$m (V)), the static full well capacity under integrating conditions with 3 gates biased to 10 V is 220,000 electrons. Its dynamic storage capacity, during the transport underneath 2 gates, is limited to about 100,000 electrons, depending on the bias of the p-well.

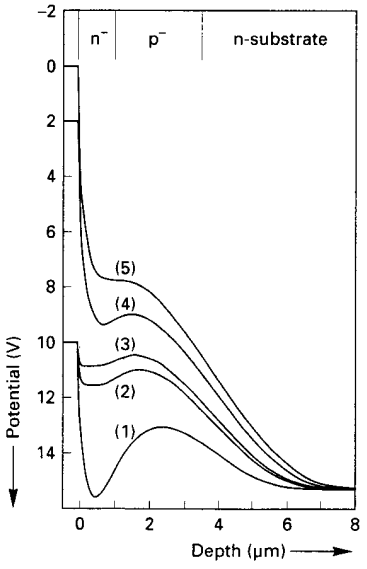


Figure 3 : Shown are the simulated electrostatic potential diagram through the center of the pixel from Figure 2 and in the direction perpendicular to the Si-$SiO_2$ interface into the bulk of the silicon. (The different curves are explained in the text.)

- in case the potential barrier between the CCD-channel and the substrate reduces to 0.4 V, as shown by curve (3), the electron transport across this barrier is of a value which corresponds to the overexposure conditions.
  Remark that in all cases, there is at least a potential difference of 0.25 V between the channel potential and the potential at the Si-$SiO_2$ interface. With this restriction, the electrons from the charge packet will not interfere with the interface states, and the CCD will keep its high transport efficiency.
- during integration, the barrier gates are biased at 2 V, as depicted by curve (4). Notice the small potential well underneath this gate, which is responsible for an active barrier gate : electrons generated underneath the barrier gate will be collected into neighbouring potential wells. The small barrier towards the substrate prevents draining of these electrons. On the other hand its collecting depth is reduced to 1.5 $\mu$m.
- if all gates of the image cell are biased to 0 V, there will be no longer any potential well in the silicon, and no electrons can be stored. This situation, shown by curve (5), is created in the frame transfer imager during charge reset, which is accomplished simply by biasing all gates from the image area to an extra low voltage, without any pulse on the n-substrate or on the p-well.

## 3. GATE INTERCONNECT.

As already mentioned in the discussion around the image cell configuration, a fast and optimal CCD-transport needs CCD-gates with a sufficiently low RC-value. A classical interconnect scheme for the CCD-gates of a two-dimensional imager is shown in Figure 4a. The vertically running n-CCD channels are covered by means of horizontally running poly-silicon CCD-gates. These CCD-gates are connected to a four phase bus-bar system defined around the image area, and made from the metallisation level. Every gate is connected from two sides. If this interconnect scheme is applied to the 1" frame transfer imager, the maximum frame shift speed is limited to about 30 kHz. On the other hand to fulfil the frame shift within the vertical field blanking period, a minimum vertical transport frequency of 700 kHz is required.

To overcome this problem, the HDTV image sensor has to be built in a new technological metallisation concept to decrease the RC values of the CCD gates. This new concept is found in a new interconnect scheme, depicted in Figure 4b : the same CCD-channels with the same CCD-gates are still in place. This holds also for the metal bus-bars, only the interconnect between the poly-silicon gates and the metal bus bars is changed. In the new concept, an additional (defined as metal1) interconnect layer is used to bridge the large resistive values of the CCD-gates. This metal-1 is defined in very small straps on top of the (light insensitive) channel stopper implants. They contact every fourth gate, and strap all gates of the same phase. In the original architecture, 1920 pixels are defined between two poly-silicon metal contacts, in the new architecture, only 4 pixels are between two contact points.

This idea can even further explored. The metal-1 straps are no longer connected to the bus-bars on top of the image section, but are fed into the storage area and are locally connected to the aluminum bus-bars. This ultimate construction is shown in Figure 4c. The net result is an imager with bus-bars very short in length, far away from the image area. In this way, unwanted reflections on the aluminum mirrors in case of Figures 4a and 4b, which are responsible for artifacts in the image section, can be easily avoided.

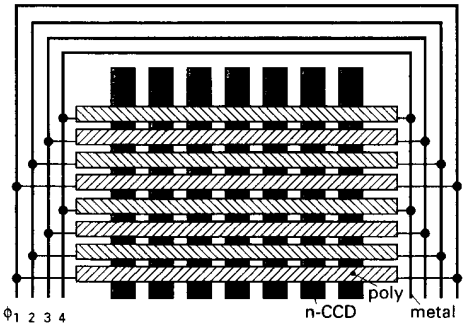


Figure 4a : Conventional interconnect scheme for the image section of a 2-dimensional image sensor.

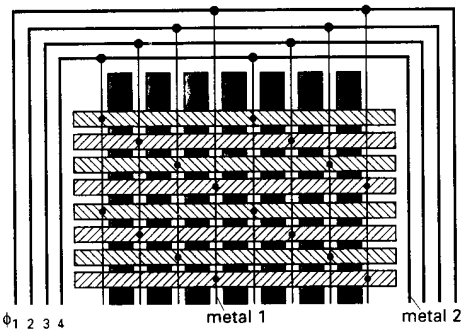


Figure 4b : Lowering the RC-values of the CCD-gates by means of an additional metal layer.

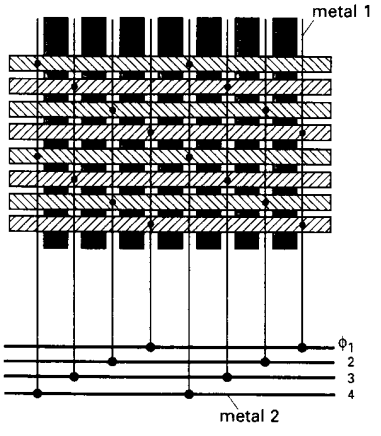


Figure 4c : Interconnect architecture used in the imager reported in this paper.

## 4. DEVICE PARAMETERS AND CHARACTERISTICS.

In table 1, the device parameters and device characteristics are summarised. This sensor is the key component of a 3-chips professional HDTV-camera. The HDTV-camera has a shutter included in its optical system. This shutter cuts the light way during the vertical frame shift of the frame transfer CCD. In this way the application of the HDTV-imagers is made fully smear-free.

| Parameter | Value |
|---|---|
| HDTV-standard | Eureka |
| Aspect ratio | 16:9 |
| Interlacing | 2:1 |
| Fields/sec | 50 |
| CCD-type | FT |
| Optical format | 1 inch |
| Image diagonal | 16 mm |
| Image area width | 13.92 mm |
| Image area height | 7.83 mm |
| Number of lines | 1152 |
| Pixels/line | 1920 |
| Pixel width | 7.25 $\mu$m |
| Pixel height | 13.6 $\mu$m |
| Chip width | 15.37 mm |
| Chip height | 15.57 mm |
| Chip area | 239 mm$^2$ |
| Output registers | 2 |
| Pixel output rate | 72 MHz |
| Frequency H-clocks | 36 MHz |
| Swing H-clock | 5 V |
| Frequency V-clocks | 1.125 MHz |
| Swing V-clock | 8 V |
| Sensitivity output | 13 $\mu$V/e$^-$ |
| Amplifier gain | 0.6 |
| Noise electrons | 19 e$^-$ |
| Bandwidth output | 160 MHz |
| Quantum efficiency | 20 % |
| Overexposure capacity | $10^5$ x |
| Full well capacity | $10^5$ e$^-$ |
| Dynamic range | 74 dB |
| Resolution | 1000 TV-lines |
| Image lag | none |
| Smear (incl. camera) | none |

Table 1 : Device parameters and characteristics.

## 5. CONCLUSIONS.

The 2.2 Mpixel frame transfer CCD described in this paper has successfully tackled the following challenges :
- the RC-values of the CCD-gates are lowered considerably by means of the new interconnect scheme,
- the high output rate is halved by using a double horizontal output register,
- the device is provided with an output stage characterised by low noise, a high bandwidth and a high conversion factor [6],
- the imager has a compact and efficient image cell functioning as photo convertor, transporting cell, highlight handler and charge resetting site.

The imager presented combines a few attractive elements which are additional when compared to the competition :
- 1920 pixels/line give the device the full HDTV-resolution of 1000 TV-lines,
- in the application, the device is running fully smear free,
- due to its architecture and its technology, the imager is fully image-lag free and the pixels are characterised by a high uniformity,
- charge reset to shorten the integration time can be applied very easily : simply biasing all image area gates to a low potential,
- the pixels are not provided with micro-lenses. This means that the pixels keep their linear photo-response, with respect to the F-number of the lens, and their resolution capabilities remain unchanged.

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