A 2.2 Mpixel FT-CCD imager, according to the Eureka HDTV-standard.

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ABSTRACT.

The first frame transfer CCD imager with 2.2 Mpixel, developed for use in HDTV applications according to the Eureka HDTV standard is reported: 1250 lines/frame, 1920 pixels/ line, 50 fields/sec, aspect ratio 16:9, 2:1 interlacing. The image section of the CCD fits to an optical system of 1 inch, corresponding to a diagonal of 16 mm. The total chip area is 240 mm².
This huge HDTV sensor has tackled successfully some typical technological challenges:
- too high RC-value of the poly-silicon CCD gates,
- the high pixel count resulting in an output rate of 72 MHz,
- providing the device with a high sensitive, low noise and high bandwidth output amplifier,
- a compact and efficient CCD cell combining the photo conversion, CCD transport, vertical anti-blooming and electronic charge reset.

INTRODUCTION.

During the last few years, several HDTV imagers are announced. But all devices reported suffer from one or another shortcoming not acceptable for HDTV-imagers. Image lag is a typical problem for the devices overlaid with amorphous silicon [1], interline and frame interline imagers deal with smear artifacts [2] and imagers with micro-lenses [3] show non-linearity effects. All data published up to now describes CCD imagers applicable to the 1125:60:2 standard.
In this paper, an imaging system fully free of image lag and of smear, with a fully linear spectral response and according to the European 1250:50:2 standard is described. The device architecture is shown in Fig. 1: a frame transfer type CCD with a dual horizontal output register. All section are 4 phase driven, buried channel CCD's, processed in a triple poly, double metal technology.

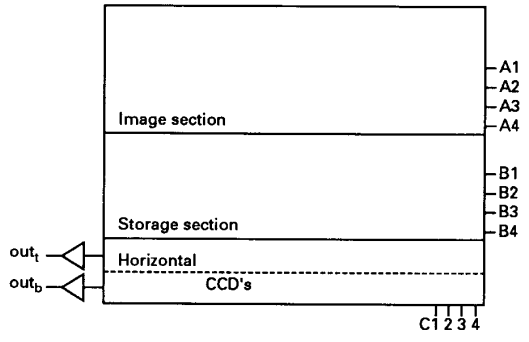


Fig. 1. Architecture of the HDTV frame transfer image sensor.

GATE INTERCONNECT SCHEME.

The image area, with a 16 mm image diagonal is constructed with horizontal running poly-silicon gates. The gate structure is schematicly illustrated in top part of Fig. 2: (vertical) n-type buried channel CCD's covered with (horizontal) poly-Si gates, arranged in a 4-phase configuration with aluminum bus bars. The gates have dimensions of 1.2 µm in height and 14 mm in width. With this set-up, the maximum transport speed is limited, and the transport time does not fit in the vertical blanking of the Eureka standard.
To increase the transport speed considerably, the poly-Si gates are

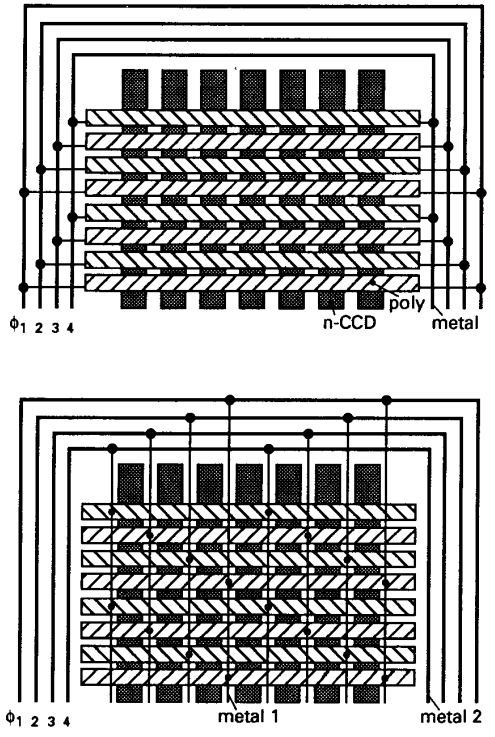


Fig. 2. Interconnect scheme of a conventional FT-imager with a single metal layer (top) and of the new HDTV sensor with an additional metal layer (bottom).

shunted by a second layer of metal. The new situation is illustrated in the bottom part of Fig. 2: the same poly-Si gates on the same CCD channels, shunted by means of an additional metal layer. The 4-phase driving option is maintained, and the complete imager can be operated with a vertical transport speed of at least 1.25 MHz, without any loss in charge handling capability.
Fig. 3 shows an SEM-photograph of a partially processed image cell: the horizontally running gates with their vertical shunts.

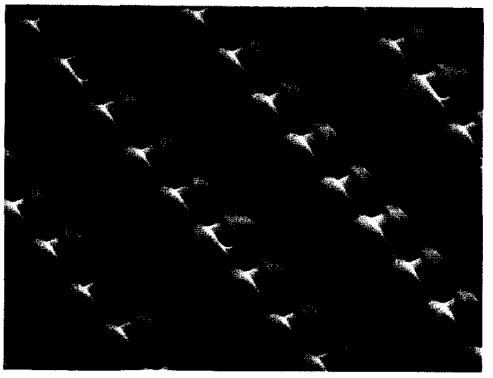


Fig. 3. SEM-photograph of a partially processed image cell.

OUTPUT REGISTER AND OUTPUT STAGE.

The high pixel count of the HDTV imager results in an output rate of 72 MHz. This puts severe constraints to the driving electronics and the off-chip video pre-processing. To simplify the construction of these off-chip circuits, the horizontal output register of the device is split into two parallel, 4-phase CCD lines (see Fig. 1). The clock frequency of the horizontal CCD's can be reduced to 36 MHz, and the bandwidth of video pre-processors can be limited too.
The design of a highly sensitive, low noise and high bandwidth output amplifier has to satisfy manu conflicting needs. Special care has been taken to the design and the lay-out of the 2 triple source follower

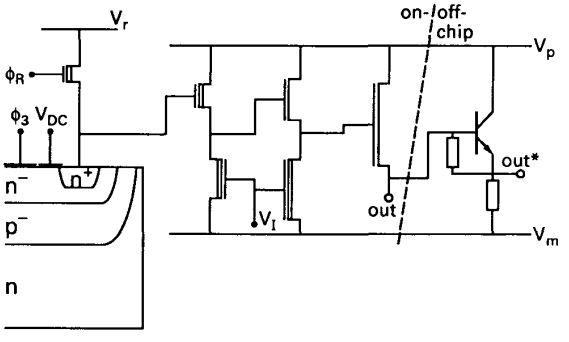


Fig. 4. Concept of the triple source follower output stage of the HDTV imager, with the emitter follower off-chip.

output stages. Their concept is shown in Fig. 4. The enhancement MOS-transistors have self-aligned sources and drains, the depletion MOS-transistors and the output diffusion have non self-aligned n^+-diffusions. This construction reduces overlap capacitances and introduces a kind of LDD structure, thereby lowering the noise. A compromise has to be made for the last clocking gate of the horizontal registers: they have to be as short as possible to allow a fast transport across the DC output gate towards the floating diffusion but they have to contain also the full well packet of 200,000 electrons for which the horizontal structures are designed. Extensive simulations under steady state and non-steady state [4] resulted in a gate length of 6 μm. Some of the results obtained by means of the dynamic simulations are shown in Fig. 5a and 5b. Shown is the transport of the electrons, at different time instants, from the last clocking gate (ϕ_3 on Fig. 4) of the horizontal register across the DC-output gate (V_{DC} on Fig. 4) towards the floating diffusion, in case of a 6 μm long ϕ_3-gate in Fig. 5a, in case of a 8 μm long ϕ_3-gate in Fig. 5b:
(See next page)

- charge transport can start at time t = 0 nsec, when ϕ_3 goes low,
- the first small enlargement of the charge packet can be seen at t = 0.5 nsec, when the charge is spread out underneath the output gate,
- the first electrons arrive at the floating diffusion at t = 1.5 nsec,
- the theoretical end of the charge transport is at t = 4.5 nsec,
- the end result at t = 5.5 nsec, shows the electrons left behind and shifted backwards to the next coming charge packet: about 3 electrons in case of 6 μm gate length and about 800 electrons in case of 8 μm gate length.

The main electrical parameters of the output amplifier can be seen on Fig. 6 which illustrates the noise behaviour as a function of frequency.

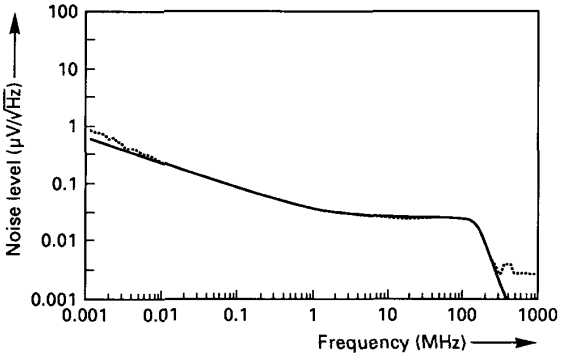
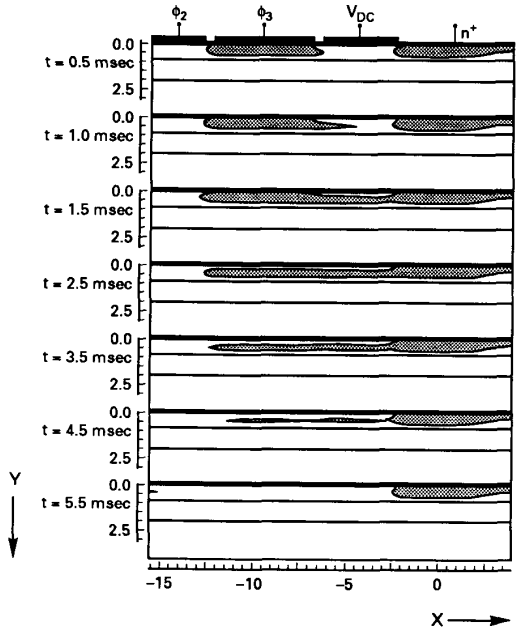


Fig. 6. Noise measurement of the output stage as a function of the frequency: dots are measurments, solid line is a fit.

From this figure the following parameters can be deduced: bandwidth of the amplifier 157.8 MHz, cross-over frequency (from 1/f to thermal noise): 1.2 MHz, noise equivalent electrons: 2.5 e-/√MHz, resulting in a noise floor for the output stage after signal processing in 19 e- (bandwidth 30 MHz).

IMAGE CELL.

The HDTV imager is provided with a compact and efficient image cell which combines the following functions into each pixel: photo conversion, CCD transport with a high efficiency, vertical anti-blooming and electronic charge reset to shorten the integration time. A top view and a cross section of such a pixel is shown in Fig. 7. Extensive 2D and 3D electrostatic potential simulations are used



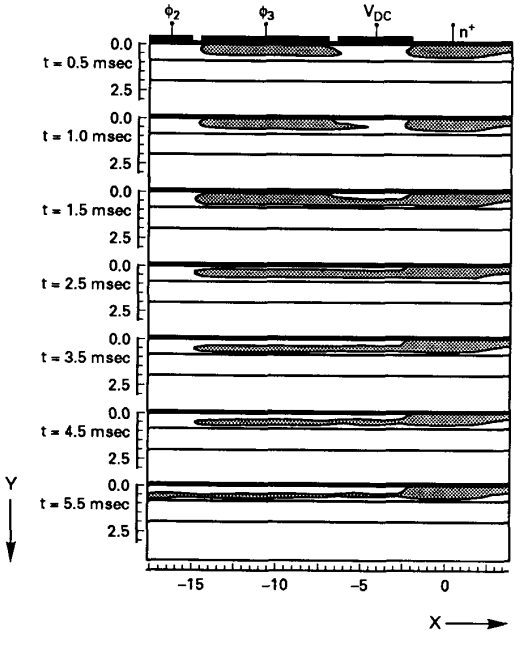


Fig. 5. Dynamic simulation of the charge transport from ϕ_3, across V_{DC} towards the floating diffusion. Top : ϕ_3 has a length of 6 µm, bottom ϕ_3 has a length of 8 µm (all numbers are µm).

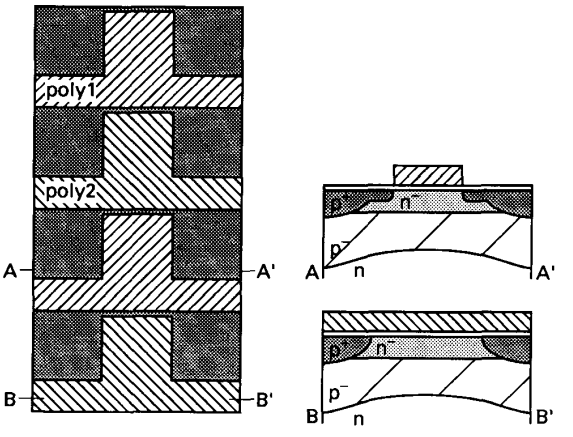


Fig. 7. Lay-out of the image cell: top view and corresponding cross sections.

to optimize not only the image cell lay-out but also the charge transport from the storage region into the dual horizontal output registers. The results of these potential calculations for the image cell, (through the centre of the pixel as shown in Fig. 7) are illustrated in Fig. 8: for an empty well, a full well with 100,000 electrons, a 100x overexposed well, a barrier gate and a gate at charge reset potential.

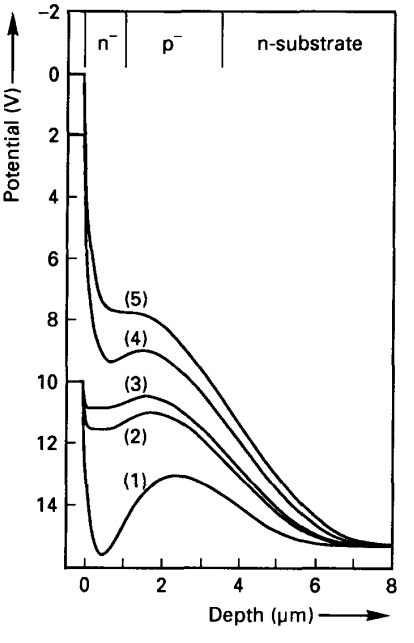


Fig. 8. Potential curves through the center of the image cell: (1) VG = 10 V, empty well; (2) V_G = 10 V, full well; (3) V_G = 10 V, full well, 100x overexposure, (4) V_G = 2 V, barrier gate, (5) V_G = 0 V, charge reset mode.

CONCLUSION.

Some device parameters and characteristics are summarized in Table 1.

Table 1. Device parameters.

ITEM	VALUE
Number of active lines	1152
Number of pixels/line	1920
Number of field/sec	50
Interlacing	2 : 1
Aspect ratio	16 : 9
Image diagonal	16 mm
Image area	109 mm^2
Pixel width	7.25 µm
Pixel heigth	13.6 µm
Chip Area	240 mm^2
Frame shift frequency	1.125 MHz
Horizontal clock freq.	36 MHz
Pixel frequency	72 MHz
Clockswing	10 V
Overexposure	10^5
Output sensitivity	11 µV/ e^-
Bandwidth output stage	>150 MHz
Quantum eff. (500 nm)	20 %
Noise floor	<20 e^- rms
Smear (with shutter)	none
Image lag	none
Charge reset	yes

A photograph of the image sensor is shown in Fig. 9, a representation of an image obtained with the device is shown in Fig. 10.

In conclusion, the first fully functional HDTV image sensor is presented which can be operated according to the Eureka HDTV standard. The concept of the device is an FT CCD, with a new double metal interconnect scheme, a dual horizontal output register, a high performance output stage and a compact and efficient image cell.

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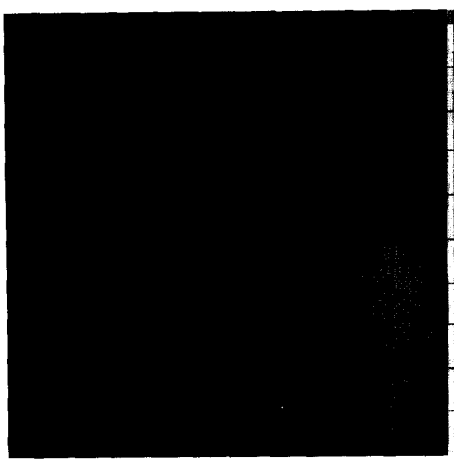

Fig. 9. Photograph of the 2.2 Mpixel frame transfer HDTV imager.

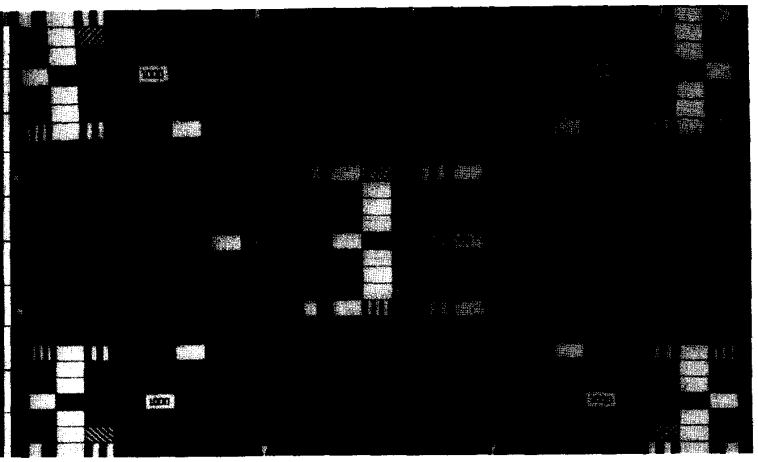

Fig. 10. Image taken by the 2.2 Mpixel frame transfer HDTV imager.